Implementation of *Initial-On* ESD Protection Concept With PMOS-Triggered SCR Devices in Deep-Submicron CMOS Technology

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***Abstract*—In order to enhance the applications of SCR devices for deep-submicron CMOS technology, a novel SCR design with "*initial-on*" function is proposed to achieve the lowest trigger voltage and the highest turn-on efficiency of SCR device for effective on-chip ESD protection. Without using the special native device (NMOS with almost zero or even negative threshold voltage) or any process modification, this initial-on SCR design is implemented by PMOS-triggered SCR device, which can be realized in general CMOS processes. This initial-on SCR design has a high enough holding voltage to avoid latchup issues in a VDD operation voltage of 2.5 V. The new proposed initial-on ESD protection design with PMOS-triggered SCR device has been successfully verified in a fully-silicided 0.25-μm CMOS process.**

***Index Terms*—Electrostatic discharges (ESD), silicon controlled rectifier (SCR), turn-on efficiency, holding voltage.**

I. Introduction

ELECTROSTATIC DISCHARGE (ESD) damage has become one of the main reliability concerns for CMOS IC products fabricated in the deep-submicron CMOS processes. On-chip ESD protection devices must be added into CMOS chips to achieve the required ESD robustness. In the past, the traditional ESD protection devices are initially kept off in CMOS ICs, as illustrated in Fig. 1. When the pad is zapped with ESD pulse, the ESD clamp device is triggered on by the ESD stress voltage to conduct ESD current from the pad to ground. However, when the core circuits are realized with a much thinner gate oxide in a deep-submicron CMOS technology, the traditional ESD protection design cannot be able to effectively protect the core circuits with thinner gate oxide. To effectively protect the core circuits with much thinner gate oxide in the deep-submicron CMOS technology, a new on-chip ESD protection concept with the initial-on ESD protection device is shown in Fig. 2. The ESD clamp device is kept off, when the IC is in the normal circuit operation conditions. But, the ESD clamp device is initially on, when the IC is floating without any power bias. When the pad is zapped by ESD, the ESD clamp device standing in the already-on status can quickly discharge ESD current from the pad to ground. Therefore, this new ESD protection concept can effectively protect the internal circuits in a deep-submicron CMOS technology [1].

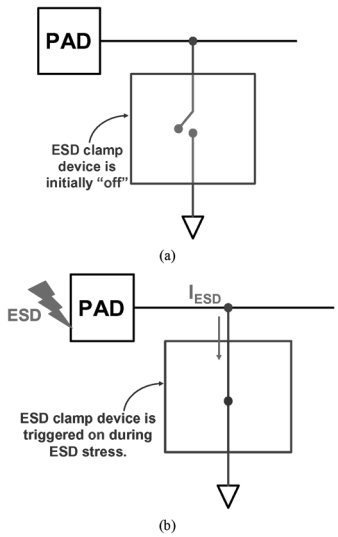

Fig. 1. The traditional ESD protection design with the initial-off ESD protection device. (a) The ESD clamp device was kept off in normal circuit operation conditions. (b) During ESD stress, the ESD clamp device was triggered on to discharge ESD current.

In Fig. 3, the optimum ESD protection design window is restricted within the range between VDD operation voltage and the gate oxide breakdown voltage. The ESD protection circuits should be triggered on to discharge the ESD currents, and to protect the internal circuits without gate oxide damage. Therefore, the trigger voltage of the ESD protection circuit must be lower than the breakdown voltage of the internal circuits. In addition, the holding voltage and on resistance $(\mathrm{R_{on}})$ of ESD protection circuit will significantly influence the ESD robustness of CMOS IC product. The lower holding voltage and smaller on resistance $(\mathrm{R_{on}})$ can provide more efficient ESD protection. However, the holding voltage of ESD protection devices must be higher than the VDD operation voltage to prevent the latchup under normal circuit operation condition [2].

In IC products, the on-chip ESD protection designs are required to provide higher ESD robustness with smaller layout area to save the chip area. Silicon controlled rectifiers (SCRs) have been used as on-chip ESD protection devices, because of their superior area-efficient ESD robustness [3]. However, SCR

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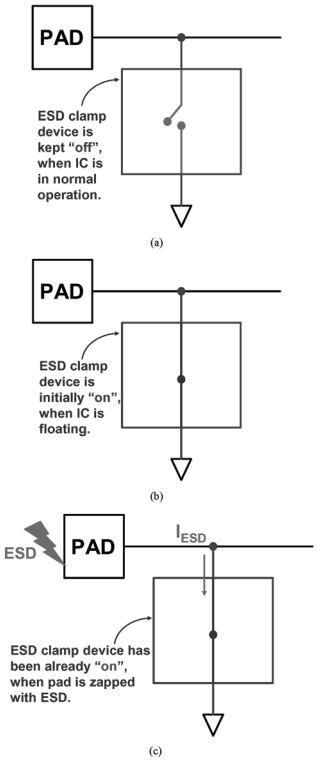

Fig. 2. The new ESD protection concept with the initial-on ESD protection device. (a) The ESD clamp device was kept off in normal circuit operation conditions. (b) The ESD clamp device was initially on when IC was floating. (c) The already-on ESD clamp device can rapidly discharge ESD current during ESD stress.

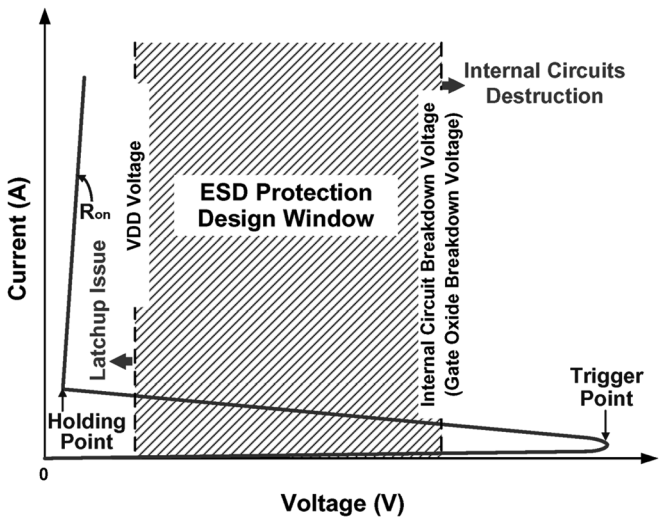

Fig. 3. The design window for ESD protection. The traditional *I–V* characteristic of SCR device can not meet to this ESD protection design window.

has some drawbacks, such as higher trigger voltage (Vt1), lower turn-on efficiency, and even latchup danger. The traditional *I–V* characteristic of the SCR device is shown in Fig. 3. The higher trigger voltage and lower turn-on efficiency would not efficiently protect the internal circuits in deep-submicron or nanoscale CMOS technology. Therefore, the low-voltage-triggered SCR (LVTSCR) was invented to reduce the trigger voltage of SCR device [4]. Moreover, some advanced circuit techniques (the gate-coupled [5], substrate-triggered [6], and GGNMOS-triggered [7] techniques) were also reported to enhance the turn-on efficiency of SCR devices. However, those modified SCR designs [4]–[7] still function as the initial-off ESD devices. Recently, in order to further enhance the turn-on speed, the native-NMOS-triggered SCR (NANSCR) has been reported to achieve more efficient ESD protection for CMOS ICs in a 0.13-μm CMOS technology [8]. In this NANSCR, it uses the special native device to achieve the "*initial-on*" function. The native device is the nMOS transistor with the almost zero threshold voltage (about 0.1 V). It is directly built in a lightly-doped p-substrate, whereas the normal nMOS is in a heavily-doped p-well in p-substrate CMOS technology. Besides, to keep such NANSCR in off state when the IC is in normal operation, it needs the on-chip negative-bias generator [9]. Such extra efforts to realize the NANSCR with negative gate bias for on-chip ESD protection design would cause some limitation in practical applications of general CMOS ICs.

On the other hand, the lower holding voltages (lower than VDD operation voltage) could cause latchup triggering by external noise pulses during normal circuit operation conditions. Several previous studies had been presented to increase the holding voltage during normal circuit operation conditions, such as dynamic holding voltage SCR (DHVSCR) [10], SCR devices with stacked diode string [6], and stacked SCR devices [11]. In addition, the high-current-triggered SCR devices had been proposed to safely protect the internal circuits without being accidentally triggered on by the electrical noisy pulse during normal circuit operation conditions [12].

In this work, a novel initial-on SCR design is proposed to achieve the lowest trigger voltage and the highest turn-on efficiency of SCR device for effective on-chip ESD protection. Without using the special native device or any process modification, this initial-on SCR design is realized by circuit skill with the pMOS transistor in general CMOS processes [13]. This initial-on SCR design also presents a high enough holding voltage in a fully-silicided 0.25-μm CMOS process to avoid latchup issues in normal circuit operation conditions.

II. Realization of the Initial-On SCR Design

A. Implementation of the Initial-On ESD Protection Circuit

The new proposed initial-on ESD protection design, which consists of the SCR device with PMOS-triggered technique and the *RC*-based ESD transient detection circuit, is shown in Fig. 4. A pMOS transistor is directly embedded into the SCR structure to achieve the initial-on function for ESD protection. The source and drain terminals of the pMOS transistor are connected to the additional N+ diffusion and P+ diffusion of the SCR structure, respectively, as illustrated in Fig. 4. These additional P+ diffusion and N+ diffusion are the p-triggered and n-triggered nodes in p-substrate and n-well of this SCR structure, respectively, to enhance the turn-on efficiency of SCR during ESD stress. The gate terminal of the embedded pMOS is controlled by a

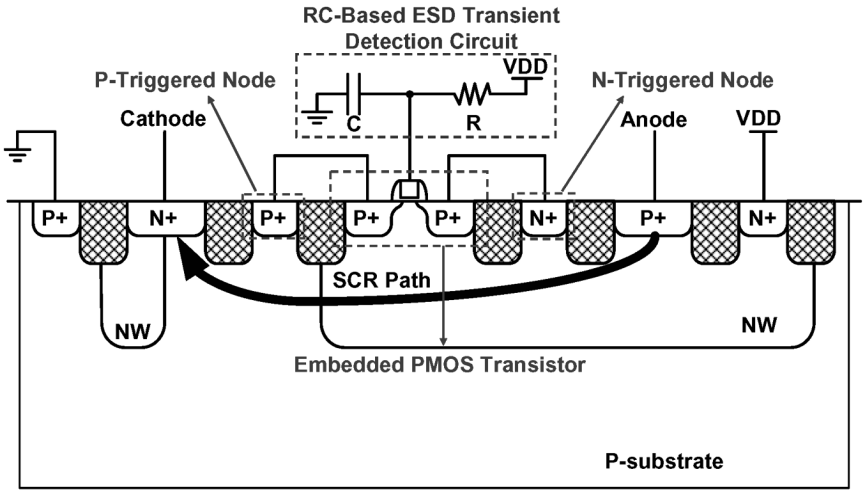

Fig. 4. Cross-sectional view of the initial-on SCR design with PMOS-triggered technique.

RC-based ESD transient detection circuit, which is used to distinguish the ESD-stress conditions from the normal circuit operation conditions.

B. Operation Principles

Under positive VDD-to-VSS ESD-stress condition, the gate voltage of embedded pMOS is initially kept at zero in the power-rail ESD clamp circuit, as shown in Fig. 5(a). With an initial gate voltage of 0 V, the pMOS transistor is initially on to conduct the ESD current from the anode P+ of SCR or pickup N+ of n-well, and then inject into the p-well/p-substrate of SCR device, as the dashed lines illustrated in Fig. 5(a). With the both trigger currents in the n-well and p-well/p-substrate synchronously, the SCR can be fired on quickly. Finally, the ESD current is mainly discharged from the anode to the cathode of SCR device. The equivalent circuit of the initial-on SCR design is shown in Fig. 5(b). The initial-on pMOS transistor provides the conduction paths to generate the voltage bias between emitters and bases, which in turns induce base currents of the parasitic vertical pnp bipolar transistor (Qpnp) and lateral npn bipolar transistor (Qnpn) to trigger on the SCR device to discharge ESD current.

Due to the difference in the rise time between the ESD pulse and the VDD power-on voltage, the *RC* time constant of the ESD-transient detection circuit is designed about 0.1–1 μs to distinguish the ESD-stress condition from the normal circuit operation condition [14], [15]. To achieve the desired operation, the *RC* time constant of the ESD-transient detection circuit in Fig. 5(a) and (b) is designed around 1 μs in this work. During normal circuit operation condition with the normal VDD and VSS power supplies, the gate of embedded pMOS is biased at VDD to keep itself off. Therefore, the PMOS-triggered SCR device is always kept off during the normal circuit operation condition.

C. Layout Structure for Initial-On SCR Device

To investigate the turn-on phenomena and circuit characteristics, two types of layout implementations (structure-1 and structure-2) for the proposed initial-on SCR device are verified in

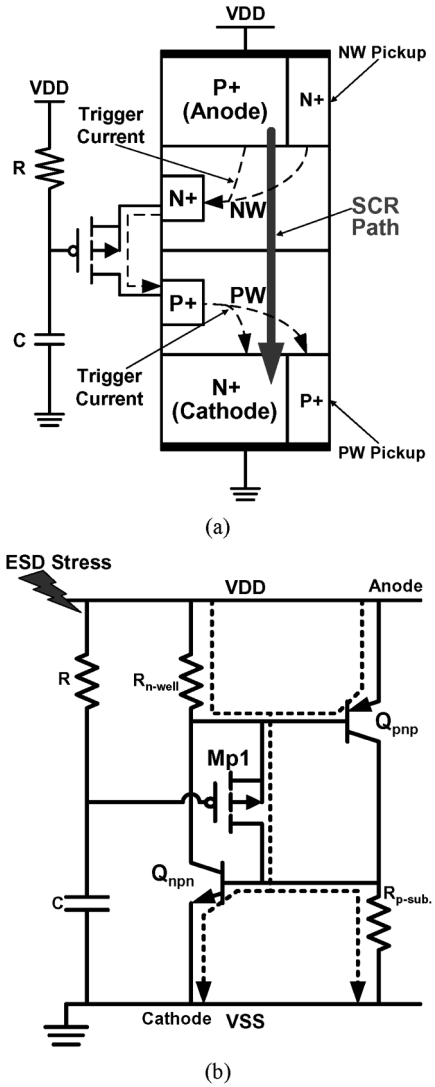

Fig. 5. (a) The operation of the initial-on SCR design for power-rail ESD clamp circuit. (b) The equivalent circuit of the initial-on SCR design. The embedded pMOS transistor generates the trigger current to initiate the turn-on of SCR during ESD stress.

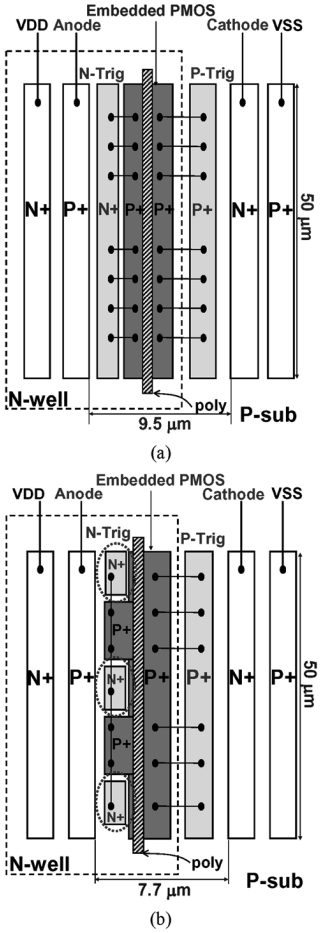

Fig. 6. Top views of initial-on SCR devices with (a) structure-1 and (b) structure-2 layout styles realized in a 0.25-μm CMOS process.

this work, as shown in Figs. 6(a) and 6(b). The SCR structure is consisted of P+ diffusion of anode, the n-well, the p-substrate (p-well), and the N+ diffusion of cathode in each test structure. The embedded pMOS transistors of structure-1 and structure-2 are different in the layout of the n-triggered node and the anode-to-cathode spacing. Because the n-triggered node has been merged into the source terminal of pMOS transistor, the anode-to-cathode spacing of structure-2 is reduced to 7.7 μm, whereas the anode-to-cathode spacing of structure-1 is 9.5 μm in a 0.25-μm CMOS process. The device characteristics, such as holding voltage, on resistance $(\mathrm{R_{on}})$, and ESD robustness, of the PMOS-triggered SCR device can be adjusted by its anode-to-cathode spacing.

III. Experimental Results

The initial-on SCR devices, in Fig. 6(a) and (b), have been fabricated in a 0.25-μm salicided CMOS process without using the silicide-blocking mask. The active width of each SCR device is drawn with 50 μm in the test chip.

A. DC Characteristics for the Initial-On SCR Devices

According to the measured device DC characteristics, the breakdown voltages of the P+ drain diffusion/n-well junction in pMOS and N+ drain diffusion/p-well junction in nMOS are, respectively, 7 V and 6.5 V in the 0.25-μm CMOS process. The n-well/p-well junction breakdown voltage is higher than 15 V in the same CMOS process. If the ESD protection devices are triggered on by junction-breakdown mechanisms, such as gate-grounded nMOS (GGNMOS), gate-VDD pMOS (GDPMOS), and LVTSCR, the junction-breakdown mechanisms often have higher trigger voltages which could not efficiently protect the internal circuits with thinner gate oxide in the deep-submicron or nanoscale CMOS technologies. Therefore, the initial-on ESD protection concept realized with PMOS-triggered SCR device is proposed in this work to achieve the lower trigger voltage and the higher turn-on efficiency.

In order to observe the influence of embedded pMOS gate bias on the trigger voltage of SCR devices, the gate-biased voltages (V_G) of 0, 1, 2, and 3 V were applied to the gate terminal of the embedded pMOS transistor. The measurement setup is shown in Fig. 7(a). The measured DC *I–V* curves of the initial-on SCR devices with structure-1 and structure-2 layout styles under different gate-biased voltages are shown in Fig. 7(b) and (c), respectively. The trigger voltage (Vt1) of PMOS-triggered SCR device is reduced with the decrease of the gate-biased voltage. When the gate voltage of the embedded pMOS is decreased from 3 V to 0 V, the Vt1 of PMOS-triggered SCR device is decreased from $\sim$ 6.6 V to $\sim$ 4 V and from $\sim$ 5.75 V to $\sim$ 3.3 V in structure-1 and structure-2, respectively. These results have proven that the Vt1 of SCR device can be significantly reduced by the proposed PMOS-triggered technique.

The holding voltage of the PMOS-triggered SCR device is slightly increased when the gate voltage of embedded pMOS is increased, as shown in Fig. 7(b) and (c). With an initial gate voltage of 0 V, the SCR device has the lowest holding voltage to effectively clamp the over-stress ESD pulse. In addition, another issue of using SCR device as the ESD protection device is the latchup concern under normal circuit operation condition. The gate terminal of the embedded pMOS transistor was biased at VDD through the resistor in the ESD-transient detection circuit during normal circuit operation conditions. To avoid latchup issue, the holding voltage of SCR devices must be designed greater than the maximum voltage of VDD. Under the temperatures of 25 °C, 75 °C, and 125 °C, the holding voltages of PMOS-triggered SCR devices in the layout styles of structure-1 and structure-2 with gate bias at VDD were shown in Fig. 8(a) and (b), respectively. The dependence of SCR holding voltages in structure-1 and structure-2 layout styles on the operating temperature is shown in Fig. 8(c). The holding voltages of the PMOS-triggered SCR device in structure-1 layout style are about $\sim$ 3.15 V to $\sim$ 2.65 V, which is higher than the 2.5-V VDD voltage, under operating temperatures of 25 °C to 125 °C. The holding voltages of the PMOS-triggered SCR device in structure-2 layout style are about $\sim$2.78 V to $\sim$2.45 V under operating temperatures of 25 °C to 125 °C. A diode can be added in series with the PMOS-triggered SCR device of structure-2 to further increase the total holding voltage for latchup-free applications in the CMOS ICs with VDD of 2.5 V.

B. Turn-on Verification

To observe the turn-on efficiency of the initial-on SCR device, 6-V ESD-like voltage pulses with different rise times were applied on the anodes of PMOS-triggered SCR with structure-1,

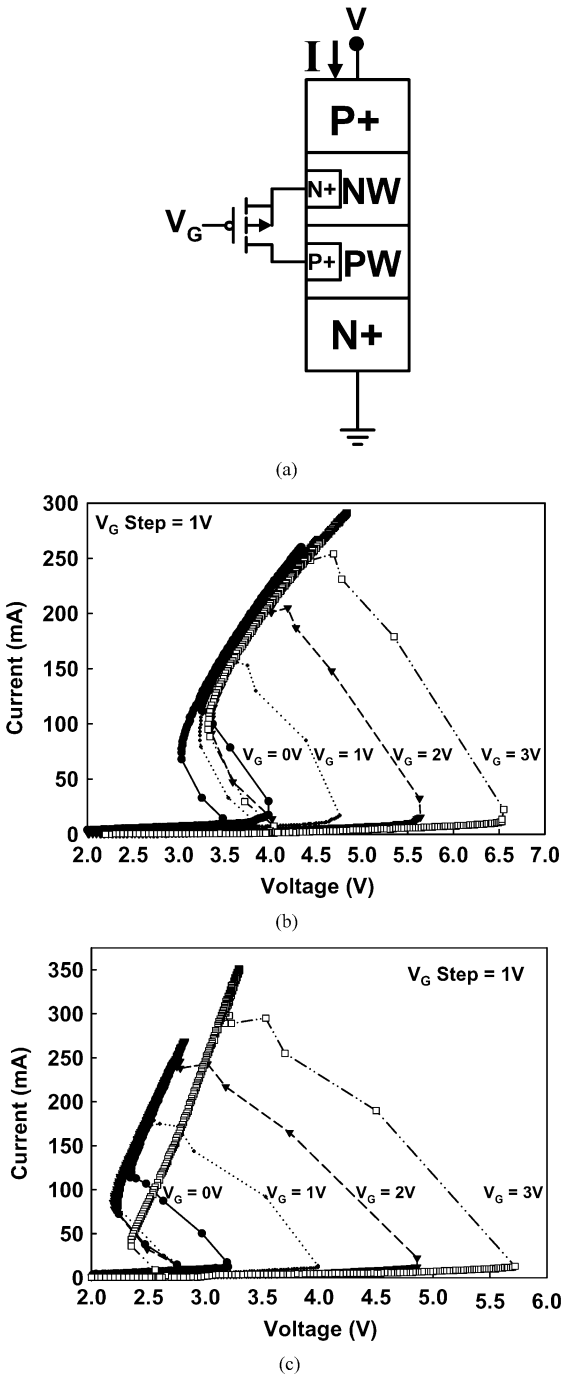

Fig. 7. (a) The different gate-biased voltages were applied to the gate terminal of the embedded pMOS transistor in the SCR structure. The measured DC *I–V* curves of the initial-on SCR devices with the layout styles of (b) structure-1, and (c) structure-2, under different gate-biased voltages.

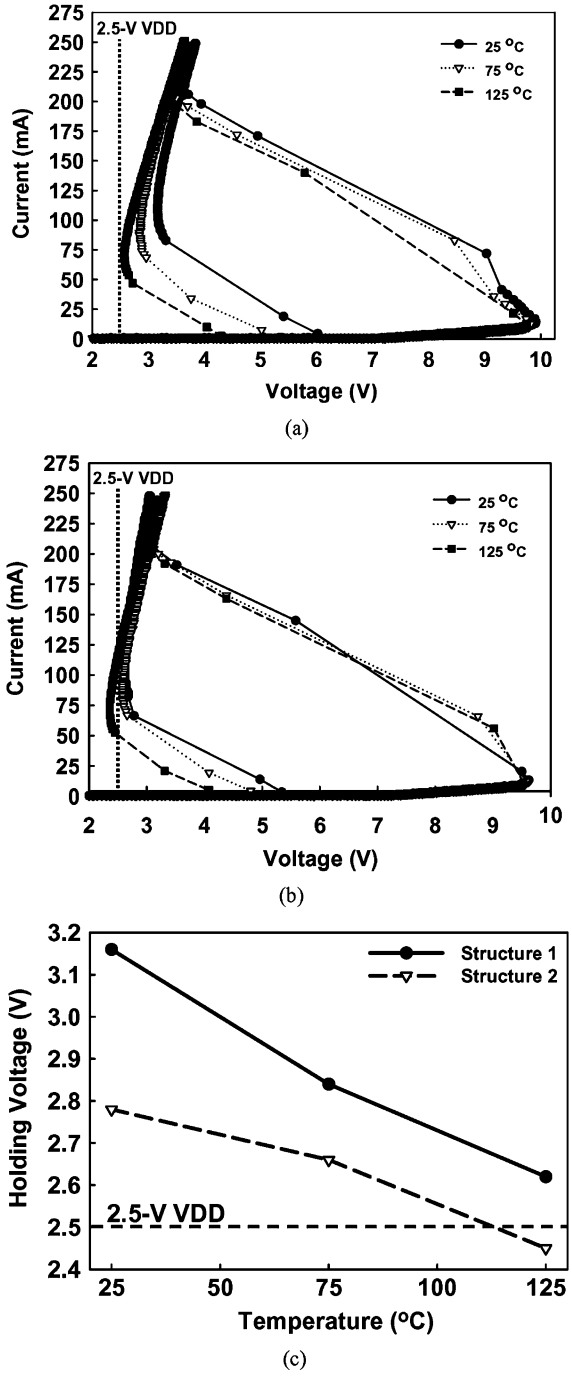

Fig. 8. The DC *I–V* curves of the initial-on SCR devices with the layout styles of (a) structure-1, and (b) structure-2, under different temperatures. (c) The dependence of SCR holding voltage on the temperature.

structure-2, and the traditional LVTSCR [4]. The measurement setup for investigating the turn-on efficiency of the initial-on SCR device is illustrated in Fig. 9(a). The rise time of Human Body Model (HBM) ESD event is about 2 ns to 10 ns [16]. The clamped voltage waveforms by different SCR devices are compared in Fig. 9(b) and (c) under the rise times of 10 ns and 1.8 ns, respectively. In Fig. 9(b), the applied 6-V ESD-like voltage pulse with a rise time of 10 ns is clamped by the PMOS-triggered SCR devices to a lower voltage level (below 4 V). In Fig. 9(c) with a rise time of as short as 1.8 ns which is faster than the typical rise time of HBM ESD event, the PMOS-triggered SCR devices performed a lower trigger voltage and higher turn-on efficiency than LVTSCR did. Because the LVTSCR device was triggered by junction breakdown occurring between p-well and the N+ drain diffusion of the embedded GGNMOS transistor, the trigger voltage of LVTSCR was much higher than that of the proposed PMOS-triggered SCR device. When the 6-V ESD-like voltage pulses with the rise time of 10 ns or 1.8 ns were applied on the PMOS-triggered SCR devices, the main

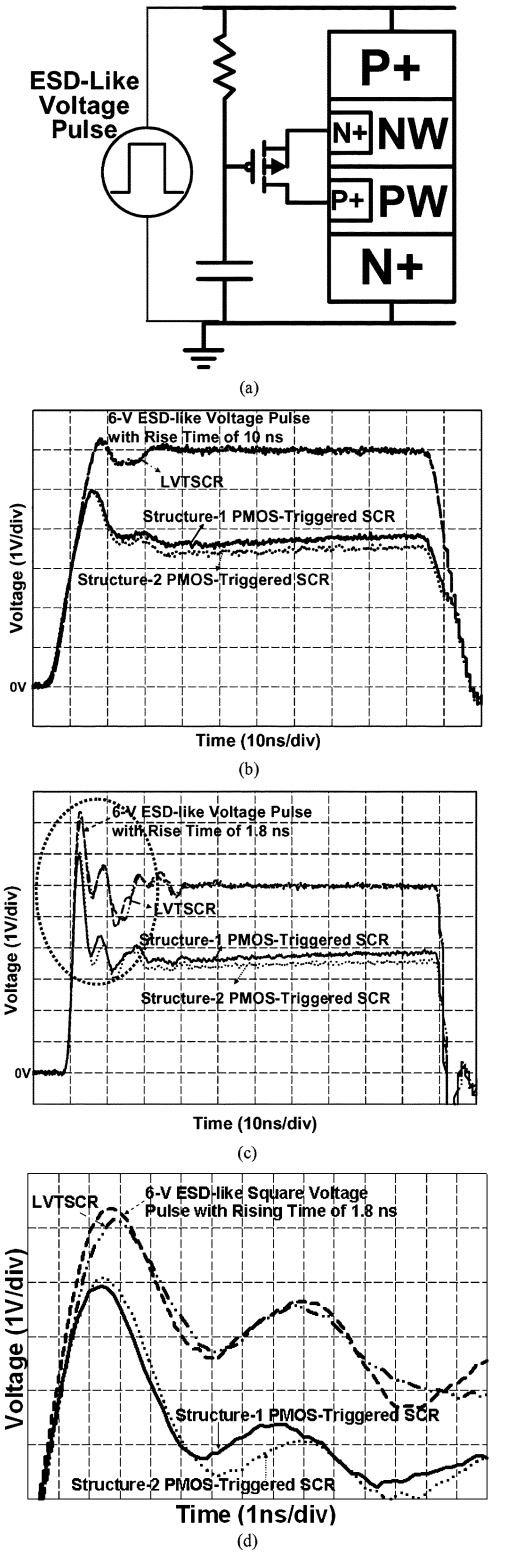

Fig. 9. (a) The measurement setup with ESD-like voltage pulse to investigate the turn-on efficiency of the LVTSCR and the PMOS-triggered SCR in structure-1 and structure-2 layout styles. The 6-V ESD-like voltage pulses were applied to the anodes of SCR devices with the rise time of (b) 10 ns and (c) 1.8 ns. (d) The zoomed-in view on the clamped voltage waveform of (c) around the rising edge.

SCR structures were rapidly turned on by the PMOS-generated trigger current. However, the LVTSCR device can not be turned on to clamp the overshooting ESD voltage pulses when

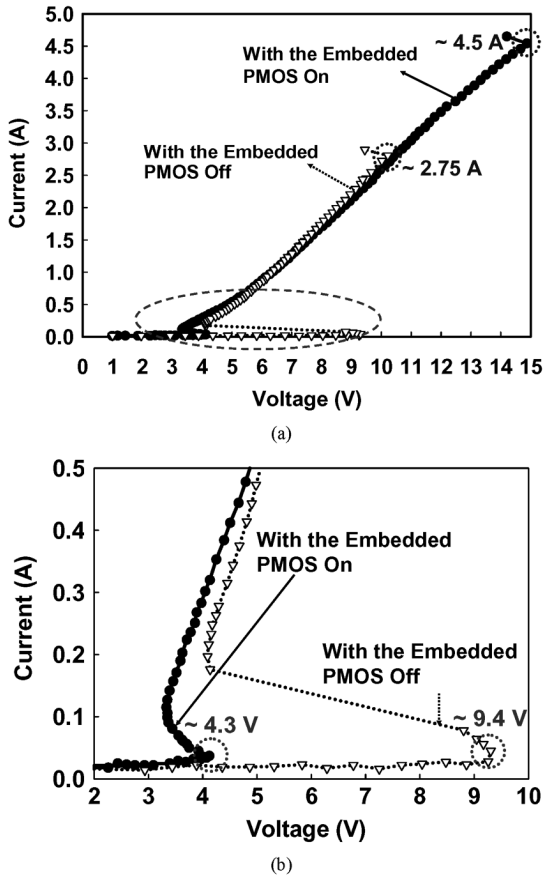

Fig. 10. (a) The TLP-measured *I–V* curves of the PMOS-triggered SCR device with structure-1 layout style under the embedded pMOS on or off. (b) The zoomed-in view of (a) around the low-current region.

the 6-V ESD-like voltage pulses were applied. According to the measurement results in Fig. 9(b) and (c), the PMOS-triggered SCR devices can be firstly turned on at a lower applied voltage pulse to efficiently clamp the overshooting ESD voltage pulse to a lower voltage level (below 4 V) at the short period. The rising edges of the voltage waveforms clearly prove the higher turn-on efficiency of the new proposed initial-on SCR devices under both structure-1 and structure-2 layout styles, as the zoomed-in waveforms shown in Fig. 9(d). With lower trigger voltage and higher turn-on efficiency, the PMOS-triggered SCR devices can rapidly clamp the overshooting ESD voltage pulse to a lower voltage level. With a duration of less than 10 ns, the overshooting ESD voltage pulse can be rapidly clamped to avoid the damage occurrence in internal circuits. Thus, the internal circuits with thinner gate oxide can be well protected by the new proposed initial-on SCR devices.

C. TLP Characteristics

The Transmission Line Pulse (TLP) measured *I–V* characteristics of the new proposed initial-on SCR devices with the structure-1 and structure-2 layout styles are shown in Figs. 10(a), (b) and 11(a), (b), respectively. The PMOS-triggered SCR devices were measured by the TLP system with a 100-ns pulsewidth and a 2-ns to 10-ns rise time. The trigger voltages of the PMOS-triggered SCR devices in structure-1

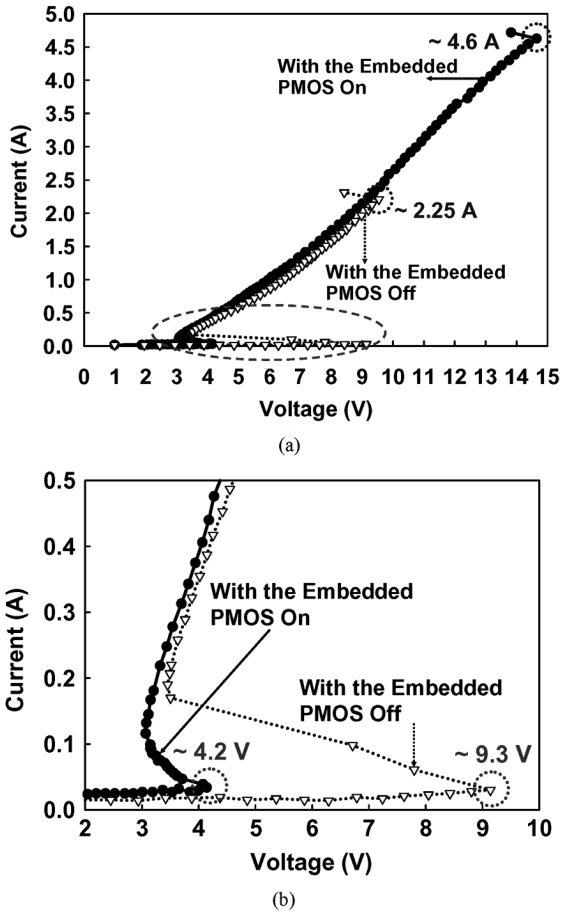

Fig. 11. (a) The TLP-measured *I–V* curves of the PMOS-triggered SCR device with structure-2 layout style under the embedded pMOS on or off. (b) The zoomed-in view of (a) in the low-current region.

and structure-2 can be significantly reduced from ∼9.4 V to ∼4.3 V and from ∼9.3 V to ∼4.2 V, respectively, as shown in Figs. 10(b) and 11(b). If the gate of embedded pMOS transistor is connected to the anode of SCR (to keep the pMOS off), the SCR devices have trigger voltages of ∼9.4 V and ∼9.3 V in structure-1 and structure-2, respectively. The second breakdown currents (It2) of the PMOS-triggered SCR devices are also obviously improved, when the embedded pMOS transistor is turned on, as shown in Figs. 10(a) and 11(a). The PMOS-triggered SCR devices with the embedded pMOS off were triggered by the junction breakdown between the n-well and the P+ drain diffusion of the embedded pMOS transistor. The trigger voltages of the PMOS-triggered SCR devices with the embedded pMOS off are much higher than that with the embedded pMOS on. In addition, because the junction breakdown occurred between the n-well and the P+ drain diffusion of the embedded pMOS transistor, the breakdown mechanism caused the local joule heats at this junction. When the higher TLP energy pulses were applied to the PMOS-triggered SCR devices with the embedded pMOS off, some junction location was produced with high enough joule heats to destroy the contacts. However, the PMOS-triggered SCR devices with the embedded pMOS on were triggered on by the trigger current generated from the pMOS transistor. The higher TLP energy pulses can be effectively discharged by the SCR structures without junction breakdown to avoid the local joule heat occurrence. Therefore, the It2 values of PMOS-triggered SCR devices with the embedded pMOS on are much higher than that with the embedded pMOS off, as shown in Figs. 10(a) and 11(a). The It2 of the proposed PMOS-triggered SCR device is about 4.5 A (4.6 A) with the layout style of structure-1 (structure-2), whereas the widths of SCR devices are only 50 μm. Moreover, for the PMOS-triggered SCR devices, a It2 of 3.5 A can be achieved before the gate-oxide breakdown of 12 V in the given 0.25-μm CMOS technology with a 5-nm gate-oxide thickness.

D. ESD Robustness

The HBM ESD robustness of the initial-on SCR devices was measured by the *ZapMaster* ESD simulator. The failure criterion is defined as 30% voltage shifting from its original *I–V* curve at 1-μA bias. With a device width of 50 μm in the given 0.25-μm fully-silicided CMOS process, the HBM ESD levels of the initial-on SCR devices with structure-1 and structure-2 layout styles are 5.5 kV and 6.0 kV, respectively. Due to the smaller distance between anode and cathode of the SCR device with the structure-2 layout style which has a lower holding voltage, the ESD robustness of PMOS-triggered SCR in structure-2 is higher than that in structure-1.

IV. Applications for On-Chip ESD Protection

A. Whole-Chip ESD Protection Scheme

The on-chip ESD protection designs for input, output, and power-rail ESD clamp circuits with the proposed PMOS-triggered SCR devices and the corresponding ESD-transient detection circuits are shown in Fig. 12(a). The initial-on SCR device with the lowest Vt1 and the highest turn-on efficiency, as compared to the other SCR devices [3], can effectively protect the internal circuits against ESD damage. Application for power-rail ESD clamp circuit, the initial-on SCR device with the gate bias of VDD on the embedded pMOS has a high enough holding voltage to prevent the latchup issue under the normal circuit operation condition. In addition, the *RC*-based ESD transient detection circuits among the I/O cells can share the same R and C to save chip area, as that (R1 and C1) shown in Fig. 12(a). The initial-on SCR device can provide bi-direction low-impedance discharging paths, which include the turn-on path of the SCR structure and the parasitic diode between n-well and p-well (p-substrate), as shown in Fig. 12(b). The initial-on SCR device is placed from each pad to VSS to provide ESD protection for the input or output circuits.

The ESD current discharging paths under different ESD-stress conditions, which are positive-to-VSS (PS) mode, negative-to-VSS (NS) mode, positive-to-VDD (PD) mode, and negative-to-VDD (ND) mode, are shown in Figs. 13(a)–(d), respectively. In Fig. 13(a) and (b) during PS-mode and NS-mode ESD stresses, the ESD currents are discharged by the initially turned-on PMOS-triggered SCR device and the parasitic diode in the SCR structure, respectively. In Fig. 13(c) during PD-mode ESD stress, the ESD current is discharged by the initially turned-on PMOS-triggered SCR device from the pad to the VSS metal line, and then from VSS to the grounded VDD through the parasitic diode of another PMOS-triggered

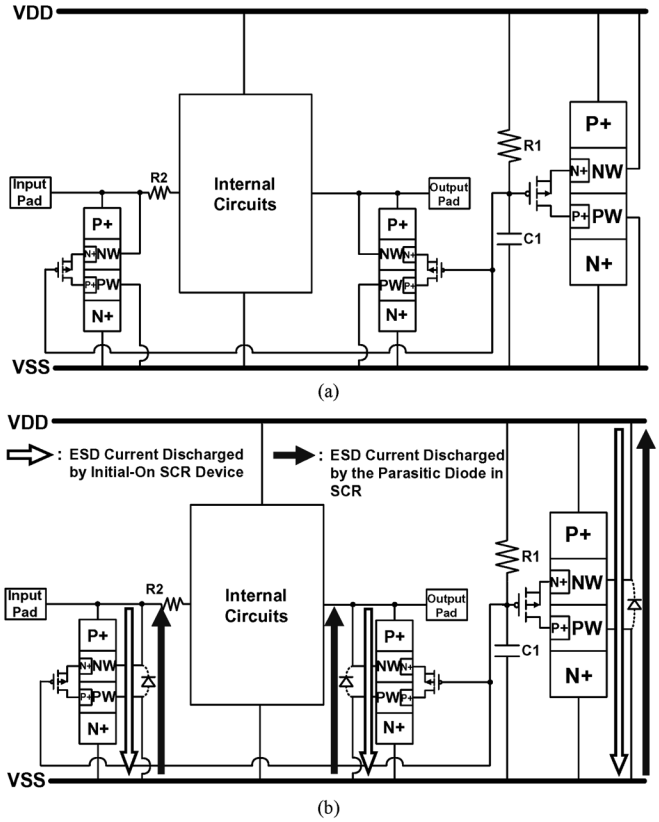

Fig. 12. (a) The on-chip ESD protection design for input, output, and power-rail ESD clamp circuits with the initial-on SCR devices. (b) The initial-on SCR device can provide the low-impedance bi-direction discharging paths to discharge ESD currents during different ESD stress conditions.

SCR device in the power-rail ESD clamp circuit. In Fig. 13(d) during ND-mode ESD stress, the negative ESD current is discharged by the parasitic diode of the SCR device from the pad to the VSS metal line, and then through the initially turned-on PMOS-triggered SCR device in the power-rail ESD clamp circuit to the grounded VDD pin.

B. ESD Protection for IC With Multi-Power Domains

The interface circuits in CMOS ICs with separated power domains are often damaged by ESD stress, especially during the I/O pin to I/O pin ESD test. For the chip with separated power domains, the whole-chip ESD protection scheme realized with the proposed initial-on SCR devices and ESD buses is shown in Fig. 14. In the same power domain, the anodes of the PMOS-triggered SCR devices are connected to the pads (including I/O, VDD, and VSS pads), and their cathodes are connected to the common ESD bus. The ESD bus can be realized by the wide metal line in the chip to efficiently conduct ESD current of several amperes during ESD stresses. To further save layout area, such ESD bus can be co-designed with the seal ring of the chip [17]. Between the ESD buses, the initial-on SCR devices are also used to connect the separated ESD buses to avoid ESD damage on the interface circuits between the separated power domains. During ESD stresses, the PMOS-triggered SCR devices with the initial-on function in the whole-chip ESD protection scheme can be quickly triggered on to efficiently protect the internal circuits. The proposed initial-on SCR devices can achieve the same turn-on efficiency of the already-on (native) device for ESD protection, but neither the extra on-chip negative voltage generator nor the native device is needed to realize with this initial-on ESD protection concept with the PMOS-triggered SCR device.

C. Discussion

The PMOS-triggered SCR devices have also been implemented in more advanced CMOS technologies, such as 0.18-μm CMOS technology and 90-nm CMOS technology. According to the measured results of PMOS-triggered SCR devices in 0.18-μm CMOS technology, the PMOS-triggered SCR devices have the lower trigger voltage (below 3.6 V) and higher second breakdown current (over 4 A) to efficiently protect the internal circuits in deep-submicron CMOS technologies. In addition, the lower holding voltage and smaller layout area of the SCR devices always are the advantageous to others devices, such as GGNMOS and parasitic lateral NPN bipolar transistor. According to the TLP *I–V* characteristics of the PMOS-triggered SCR devices, the holding voltages of the PMOS-triggered SCR devices are about 3 V (2.8 V) in 0.25-μm (0.18-μm) CMOS technology. The holding voltages of parasitic diodes in SCR structures are about 0.85 V in 0.25-μm and 0.18-μm CMOS technologies. Due to these excellent ESD protection characteristics, which are lower trigger voltage and lower holding voltage, and higher ESD robustness with smaller layout area, the proposed initial-on ESD protection design with PMOS-triggered SCR device is suitable to apply in nanoscale CMOS technology.

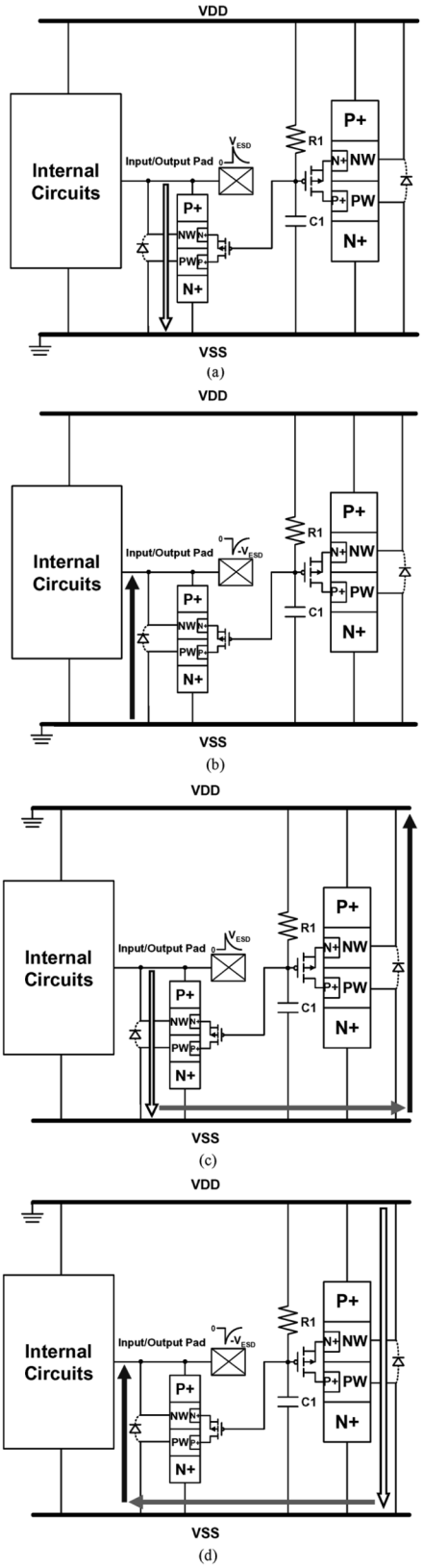

Fig. 13. The ESD discharging paths during the ESD stresses of (a) positive-to-VSS (PS) mode, (b) negative-to-VSS (NS) mode, (c) positive-to-VDD (PD) mode, and (d) negative-to-VDD (ND) mode.

In deep-submicron CMOS technology, to decrease the voltage across the ultrathin gate oxide of the internal circuits is

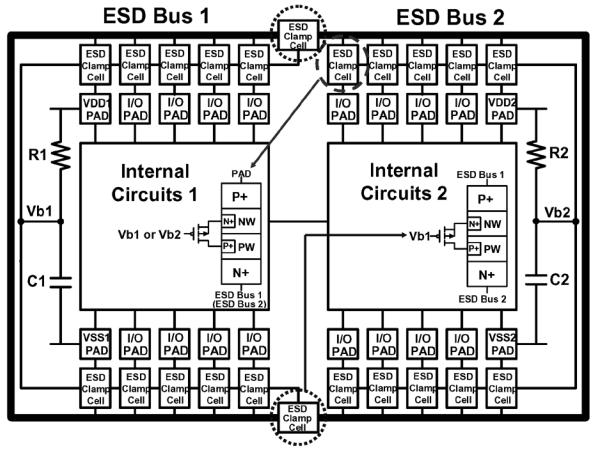

Fig. 14. The ESD protection scheme realized with the initial-on SCR devices and ESD buses for the chip with separated power domains.

the main challenge of ESD protection designs. The overstress voltages across the ultrathin gate oxide will induce the oxide breakdown to cause internal circuit damages. During the ESD stresses, the huge ESD voltages must be firstly clamp to avoid the damages of internal circuits. However, when the ESD currents discharged through the arranged ESD protection circuits, such as pad-to-VDD ESD clamp devices, pad-to-VSS ESD clamp devices, power-rail ESD clamp devices, VDD metal lines, or VSS metal lines, the voltage across the gate oxide were still raised by the holding voltages and IR drops of the ESD clamp devices, and IR drops of the VDD or VSS metal lines. The raised voltages across the gate oxide could cause the damages on the gate oxide of the internal circuits.

For the whole-chip ESD protection design scheme with PMOS-triggered SCR devices, the ESD currents can be discharged by the initially turned-on PMOS-triggered SCR device or parasitic diode in the SCR structure from the pad to the VSS, and then from VSS to VDD through the parasitic diode of another PMOS-triggered SCR device or the other initially turned-on PMOS-triggered SCR device in the power-rail ESD clamp circuit under different ESD-stress conditions. The detail ESD-current discharging paths were illustrated in Fig. 13(a)–(d). The discharging paths of PD-mode and ND-mode are longer than that of PS-mode and NS-mode. Therefore, when the ESD stress applied on an input pin, the raised voltage across the gate oxide of the pMOS transistor under PD-mode and ND-mode ESD stresses are higher than that of the nMOS transistor under PS-mode and NS-mode ESD stresses. Under PD-mode or ND-mode ESD stress, raised voltage $(\mathrm{V_{oxide}})$ across the gate oxide of the pMOS transistor can be simply evaluated by the holding voltages (V_h) of a PMOS-triggered SCR device and a parasitic diode, the IR drops of the ESD current $(\mathrm{I_{ESD}})$ discharging through the on resistances $(\mathrm{R_{on}})$ of a PMOS-triggered SCR device and a parasitic diode, and the IR drops of the ESD current $(\mathrm{I_{ESD}})$ discharging through the resistance $(\mathrm{R_M})$ of VSS metal line. The related equation of the raised voltage is shown as following. The raised voltages across the gate oxide of the pMOS transistor under PD-mode and ND-mode ESD stresses are shown in (1). Equations (2) and (3) are shown the raised voltages

across the gate oxide of the nMOS transistor under PS-mode and NS-mode ESD stresses, respectively.

$$V_{\text{oxide}} = V_{h,\text{SCR}} + V_{h,\text{diode}} + I_{\text{ESD}} \times (R_{\text{on,SCR}} + R_{\text{on,diode}} + R_{\text{M}}) \quad (1)$$

$$V_{\text{oxide}} = V_{h,\text{SCR}} + I_{\text{ESD}} \times R_{\text{on,SCR}} \quad (2)$$

$$V_{\text{oxide}} = V_{h,\text{diode}} + I_{\text{ESD}} \times R_{\text{on,diode}}. \quad (3)$$

The holding voltages of the PMOS-triggered SCR devices are about 3 V in 0.25-μm CMOS technology. The holding voltages of parasitic diodes in SCR structures are about 0.85 V in 0.25-μm CMOS technologies. The on resistances $(\mathrm{R_{on}})$ of a PMOS-triggered SCR device and a parasitic diode in the SCR structure with the 50-μm device sizes are respectively about 2.5 Ω and 1.25 Ω. Generally, the resistances of the VSS metal lines or VDD metal lines are about several tens of milliOhms in deep-submicron CMOS technology. Before the gate-oxide breakdown of 12 V in the given 0.25-μm CMOS technology, the $\mathrm{I_{ESD}}$ can achieve over 2 A (about HBM ESD robustness of 3 kV) under the PD-mode or ND-mode ESD stress in the whole PMOS-triggered SCR devices with the device sizes of 50 μm. On the other hand, the $\mathrm{I_{ESD}}$ of the NS-mode or PS-mode ESD stress was higher than that of the PD-mode or ND-mode, because the whole-chip ESD protection design scheme with PMOS-triggered SCR devices had the shorter ESD discharging paths in NS-mode or PS-mode ESD stress.

For more advanced CMOS technology applications with the ultra-thin gate oxide, the holding voltage and the on resistance $(\mathrm{R_{on}})$ of the PMOS-triggered SCR devices needs to be further decreased to reduce the raised voltage across the ultra-thin gate oxide of the internal circuits. However, the holding voltages of the SCR devices are dependent on the anode-to-cathode spacing of the SCR structures. The anode-to-cathode spacing of the PMOS-triggered SCR devices can be adjusted by the layout modifications of the embedded pMOS transistor, n-triggered node, and p-triggered node, such as the PMOS-triggered SCR devices with different layout styles of structure-1 and structure-2. The holding voltages of the PMOS-triggered SCR devices can be adjusted by different layout styles with different anode-to-cathode distances to reduce for more advanced CMOS technology applications. The holding voltages would be reduced below 2 V in the SCR devices with the shortest anode-to-cathode spacing. In addition, the on resistances $(\mathrm{R_{on}})$ of the PMOS-triggered SCR devices can be significantly reduced by increasing the device widths. The on resistances $(\mathrm{R_{on}})$ of the PMOS-triggered SCR devices are directly proportional to the device widths. The ESD robustness also can be obviously improved in the increments of the device widths. Therefore, the PMOS-triggered SCR devices with the shorter anode-to-cathode spacing and large device width can efficiently reduce the raised voltage across the ultra-thin gate oxide of the internal circuits for ESD protection applications in nanoscale CMOS technology.

V. Conclusion

The "*initial-on*" ESD protection concept realized by the PMOS-triggered SCR device with *RC*-based ESD-transient detection circuit has been successfully designed and verified in a 0.25-μm salicided CMOS process. Compared to the LVTSCR, the lowest trigger voltage and the highest turn-on efficiency of SCR device can be achieved by the proposed PMOS-triggered technique for effective on-chip ESD protection. Such PMOS-triggered SCR also presents a high enough holding voltage to overcome the latchup issue under the normal circuit operation condition. The ESD robustness of the PMOS-triggered SCR can be higher than 5.5 kV with a device width of as small as 50 μm. Therefore, such initial-on SCR devices can achieve the whole-chip ESD protection scheme for input, output, power-rail ESD clamp circuit, and the ESD clamp cells between the separated power domains.

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