A Reliability Model for Low-Temperature Polycrystalline Silicon Thin-Film Transistors

Chih-Yang Chen, Jam-Wem Lee, Po-Hao Lee, Wei-Cheng Chen, Hsiao-Yi Lin, Kuan-Lin Yeh, Ming-Wen Ma, Shen-De Wang, and Tan-Fu Lei

***Abstract*—We proposed here a reliability model that successfully introduces both the physical mechanisms of negative bias temperature instability (NBTI) and hot carrier stress (HCS) for p-channel low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs). The proposed model is highly matched with the experimental results, in which the NBTI dominates the device reliability at small negative drain bias while the HCS dominates the degradation at large negative drain bias. In summary, the proposed model provides a comprehensive way to predict the lifetime of the p-channel LTPS TFTs, which is especially necessary for the system-on-panel circuitry design.**

***Index Terms*—Hot carrier stress (HCS), low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs), negative bias temperature instability (NBTI), reliability.**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon thin-film transistors (LTPS TFTs) are known as attractive candidates for system-on-panel applications. In comparing with the requirement arisen from the pixels, the driving circuits have to control their output current precisely, which require devices with good electrical stability [1]. Hot carrier stress (HCS) has been widely studied and commonly used for reliability assurance [2]–[4]. However, because the LTPS TFT driving circuit is designed using the CMOSFET structure, the HCS becomes a transient phenomenon that mixes with the effects of negative bias temperature instability (NBTI) and positive bias temperature instability [5].

NBTI has been introduced into the reliability insurance process for the very large scale integration circuit, and the related model has been comprehensively developed [6]–[8]. Unfortunately, the mixed effects of NBTI and HCS are rarely explored for the LTPS TFTs. Therefore, we demonstrated here a reliability model for p-channel LTPS TFTs that considers both the effects of NBTI and HCS. From the experimental results and the model we proposed, the combined NBTI and HCS effects can be clearly identified.

Manuscript received January 3, 2007; revised February 12, 2007. This work was supported by the National Science Council, Taiwan, R.O.C., under Contract NSC95-2221-E-009-279. The review of this letter was arranged by Editor J. Sin.

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Digital Object Identifier 10.1109/LED.2007.895454

II. Experimental

P-channel LTPS TFTs fabricated on glass substrates were used in this letter. A 400-Å amorphous silicon layer was deposited by PECVD and crystallized into a polycrystalline silicon film through excimer laser annealing. After defining the active region, 1000-Å PECVD SiO_2 and 3000-Å sputtered Mo were deposited and patterned as the gate. The source and drain were then doped through plasma doping. The hydrogenation was performed soon after the formation of source and drain by NH_3 plasma treatment at 300 °C for 10 min. Following that, 5000-Å SiO_2 was deposited and densified as the interlayer dielectric. Finally, 5000-Å Al was deposited and patterned as the interconnection metal. The devices were fabricated with channel width (W) of 20 μm and channel length (L) of 20 or 10 μm. The constant current method is used for threshold voltage $(V_{\rm th})$ extraction, where the $V_{\rm th}$ is defined as the bias of gate voltage that forces drain current to $(W/L) \times 10$ nA at $V_{\rm DS} = -0.1$ V. Under the extraction method, the initial threshold voltages of all the devices were about -1 V at room temperature. We used HP 4156B for both the NBTI and HCS measurements. The stress was performed at various stress temperatures with gate voltage $(V_{\rm GS})$ of -20 V and drain voltage $(V_{\rm DS})$ ranging from 0 to -20 V to study the combined NBTI and HCS effects.

III. Results and Discussion

Figs. 1 and 2 show the threshold voltage shift $(\Delta V_{\rm th})$ of the devices stressed at 100 °C and 25 °C, respectively. The stress was performed with a fixed $V_{\rm GS}$ of -20 V and variable values of $V_{\rm DS}$. The measured $|\Delta V_{\rm th}|$ exhibits two degradation regimes. At the low $|V_{\rm DS}|$ stress condition, the $|\Delta V_{\rm th}|$ decreases with the increase of the $|V_{\rm DS}|$. On the other hand, the $|\Delta V_{\rm th}|$ increases upon increasing the $|V_{\rm DS}|$ at high $|V_{\rm DS}|$ bias. It should be noticed that the device degradation is simply caused by the NBTI at $V_{\rm DS} = 0$ V. The $|\Delta V_{\rm th}|$ slightly decreases when the $V_{\rm DS}$ changes from 0 to -2.5 V; this indicates that the NBTI, which is induced by vertical electric field, is suppressed at low $|V_{\rm DS}|$ bias. However, the suppression of the NBTI is soon taken over by the influence of the horizontal electric field when the $V_{\rm DS}$ continuously decreases to be smaller than -2.5 V. The phenomenon is caused from the fact that an increment of the horizontal electric field will enhance the hot carrier

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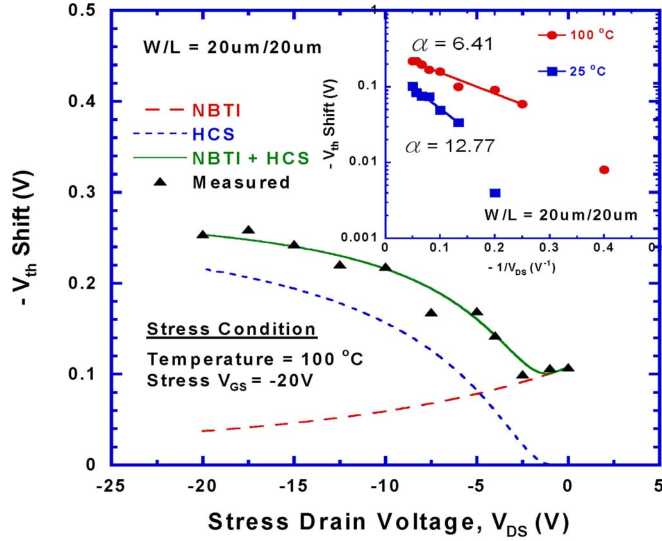

Fig. 1. Comparison of the measured $\Delta V_{\rm th}$ of the device having channel length of 20 μm with the predicted NBTI and HCS effects under stress temperature of 100 °C. The stress was performed with fixed $V_{\rm GS}$ of -20 V and $V_{\rm DS}$ ranging from 0 to -20 V. The inset shows the relationship between the magnitude of $\Delta V_{\rm th}$ and $1/V_{\rm DS}$.

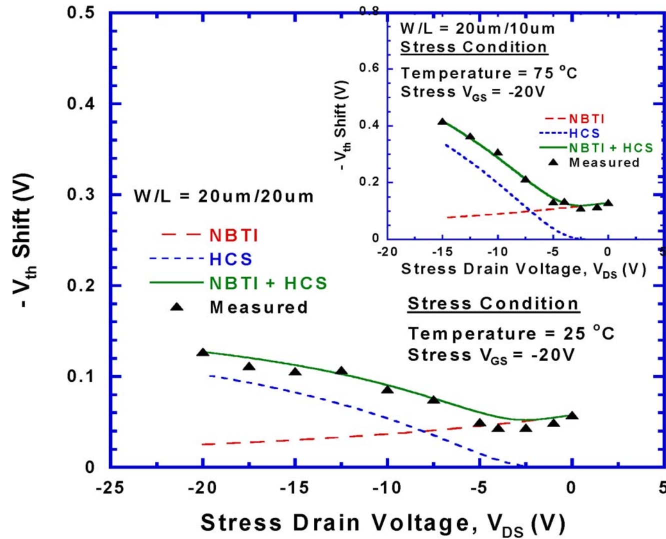

Fig. 2. Comparison of the measured $\Delta V_{\rm th}$ of the device having channel length of 20 μm with the predicted NBTI and HCS effects under stress temperature of 25 °C. The inset shows the measured $\Delta V_{\rm th}$ and predicted NBTI and HCS effects for the devices having channel length of 10 μm under 75-°C stress temperature.

generation; this is particularly true for the stress condition that $V_{\rm DS}$ and $V_{\rm GS}$ are equal to -20 V. Furthermore, from the comparison of Figs. 1 and 2, we found that the previously mentioned physical mechanisms are highly temperature dependent; this is due to the fact that both the NBTI and HCS can be thermally accelerated [9], [10].

To develop the reliability model, we introduced the parameter of the $V_{\rm DS}$ into the physical model of NBTI. In considering the mechanism of NBTI, the $\Delta V_{\rm th}$ can be expressed as the following equation [11], [12]:

$$\Delta V_{\rm th} = At^n \exp\left(-\frac{E_a}{kT}\right) \exp\left(C|V_G|\right) \tag{1}$$

where A, n, and C are the fitting parameters, and k, T, and E_a are the Boltzmann constant, temperature, and activation energy, respectively. Instead of the grounded drain, $V_{\rm DS}$ was applied to incorporate the HCS effects into the NBTI model; accordingly, the expression must be modified with respect to the theoretical calculations. The channel potential at the location y from p$^+$ source is almost a linear function of the location at low $|V_{\rm DS}|$, which can be concisely expressed as $V(y) = (y/L) \times V_{\rm DS}$ [13]. Furthermore, the vertical electric field becomes a function of $[|V_{\rm GS}| - |V(y)|]$, and the $\Delta V_{\rm th}$ can be rewritten as

$$\begin{aligned}\Delta V_{\rm th} &= At^n \frac{1}{L}\int_0^L \exp\left[C\left(|V_{\rm GS}| - |V(y)|\right)\right] dy \\ &= \frac{At^n}{C|V_{\rm DS}|} \exp\left(C|V_{\rm GS}|\right)\left[1 - \exp\left(-C|V_{\rm DS}|\right)\right]. \end{aligned} \tag{2}$$

This simple and analytic model can be used to interpret and quantify the NBTI effect under different $V_{\rm DS}$ biases, as shown in Figs. 1 and 2. In subjecting to the HCS at high $|V_{\rm DS}|$, the $\Delta V_{\rm th}$ can be experimentally expressed by the formula constructed by Takeda and Suzuki [14]

$$\Delta V_{\rm th} = Bt^n \exp\left(-\frac{\alpha}{|V_{\rm DS}|}\right). \tag{3}$$

The parameter α can be extracted from the linear fit in the inset of Fig. 1. The $\Delta V_{\rm th}$ that we used here to extract the parameter α is derived from subtracting the calculated $\Delta V_{\rm th}$ of (2) from the measured $\Delta V_{\rm th}$. In the inset, the $\Delta V_{\rm th}$ under low $|V_{\rm DS}|$ stress condition shows division from the linear fitting, implying that the generation of hot carriers can be neglected and the HCS model is not valid in the low $|V_{\rm DS}|$ bias region. The overall $\Delta V_{\rm th}$ caused by NBTI and HCS can be predicted by combining (2) and (3). The proposed model is highly consistent with the experimental results, as shown in Figs. 1 and 2. Besides, the devices with channel length of 10 μm, stressed at 75 °C, also show the same trend, as shown in the inset of Fig. 2. This implies that the model we proposed is valid for devices with different gate length and under different stress temperatures.

Fig. 3 displays the degradations of the subthreshold swing (S) and maximum transconductance (inset), which reflect the generation of deep interface states and tail interface states, respectively [15]. We found that the degradations of the subthreshold swing and maximum transconductance show similar trend with the degradations of the $\Delta V_{\rm th}$; this means that the interface state generation is suppressed at low $|V_{\rm DS}|$ stress conditions and further enhanced at high $|V_{\rm DS}|$ stress conditions.

Fig. 4 shows the correlations between the drive current ($I_{\rm ON}$) degradations and acceleration stresses. The $I_{\rm ON}$ is defined as the drain current measured at $V_{\rm GS} = -10$ V and $V_{\rm DS} = -5$ V. The degree of $I_{\rm ON}$ degradation is extracted from the methods of both forward and reverse measurement modes. For the forward mode, we obtained the transfer current–voltage characteristic by defining the drain, gate, and source electrodes exactly the same with the definition in the acceleration stresses. In contrast, the biases of source and drain were exchanged in the

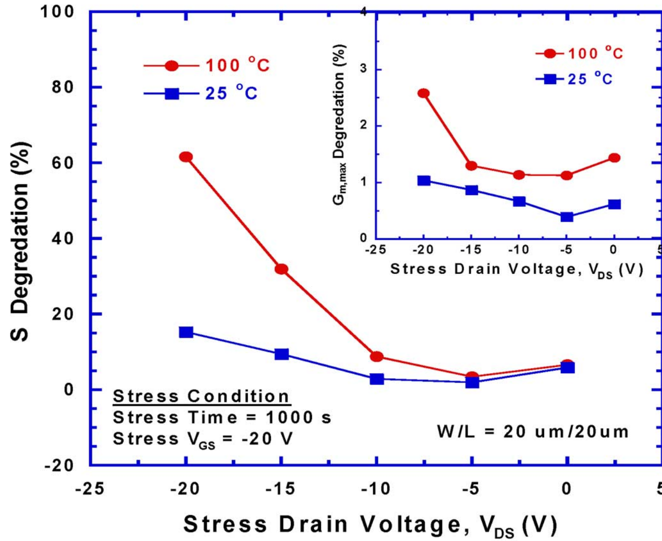

Fig. 3. Degradation of the subthreshold swing (S) and maximum transconductance (inset) as a function of $V_{\rm DS}$.

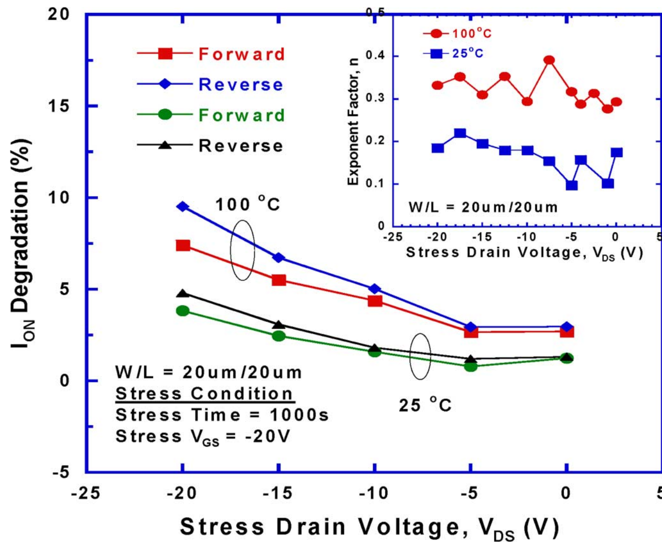

Fig. 4. Degradation of the drive current as a function of $V_{\rm DS}$ with fixed $V_{\rm GS}$ of -20 V for the devices having channel length of 20 μm. The exponent factors (n) are shown in the inset.

reverse mode. At the low $|V_{\rm DS}|$ conditions, the difference of the $I_{\rm ON}$ degradation between the forward and reverse modes is insignificant. This indicates that the NBTI-induced degradation is geometrical symmetry. However, in subjecting to the high $|V_{\rm DS}|$, the $I_{\rm ON}$ degradation in the reverse mode is significantly larger than that in the forward mode, implying that the damage caused by HCS is mainly located in the drain side.

In our experiment, the $\Delta V_{\rm th}$ follows a power law dependence on the stress time $(\Delta V_{\rm th} \sim t^n)$ that exhibits an exponent factor (n), as shown in the inset of Fig. 4. For all cases, the n values are about 0.2 at 25 °C and 0.3–0.4 at 100 °C; in analogous to the hot carrier mechanism proposed by Heremans *et al.* [16], the device degradation mechanism at 25 °C is mainly attributed to the charge trapping mechanism, while at 100 °C, the generation of interface state becomes significant.

IV. Conclusion

We demonstrate here a reliability model that could be successfully used to predict the performance of LTPS TFT's driving circuit. The model mainly includes both the drain-bias-correlated NBTI and HCS effects that are responsible for the performance degradation. Experimental results confirm that the model could precisely describe the reliability behaviors of the p-channel LTPS TFTs. The significant feature of the model is that the $\Delta V_{\rm th}$ exhibits two degradation regimes: In the low $|V_{\rm DS}|$ regime, the device degradation is dominated by the drain-bias-modulated NBTI; after that, the HCS dominates the degradation mechanism in the high $|V_{\rm DS}|$ regime. We conclude that the proposed model shows a capability in well expressing the entire reliability behavior of CMOSFET operations. Consequently, it is very attractive for the LTPS TFT circuitry design.

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