On the RF Extrinsic Resistance Extraction for Partially-Depleted SOI MOSFETs

Sheng-Chun Wang, Pin Su, *Member, IEEE*, Kun-Ming Chen, Chien-Ting Lin, Victor Liang, and Guo-Wei Huang, *Member, IEEE*

***Abstract*—We have investigated the radio frequency (RF) extrinsic resistance extraction for partially-depleted (PD) silicon-on-insulator (SOI) metal-oxide-semiconductor field effect transistors (MOSFETs). Although the thick buried oxide in SOI devices can block the substrate coupling, the SOI neutral-body coupling effect is significant for RF applications. An equivalent circuit considering this effect has been proposed. Based on this equivalent circuit, a new model capturing the frequency dependence of extrinsic resistances has been derived. After considering the impact of quasi-neutral body, we have developed a physically accurate RF extrinsic resistance extraction methodology for PD SOI MOSFETs.**

***Index Terms*—Metal-oxide-semiconductor field effect transistors (MOSFETs), radio frequency (RF), resistance extraction, silicon-on-insulator (SOI) technology.**

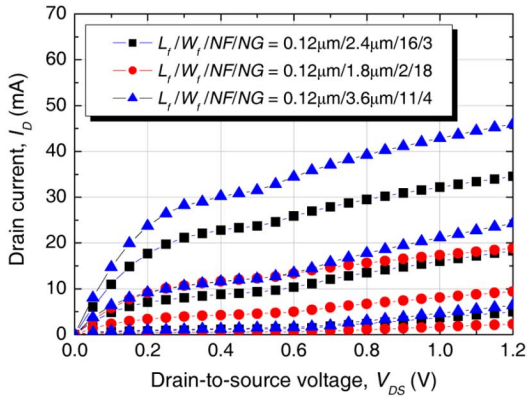

Fig. 1. I_D versus $V_{\rm DS}$ characteristics for PD SOI MOSFETs used in this study. $V_{\rm GS}$ is from 0.4 to 0.8 V with step 0.2 V.

I. Introduction

DUE to its highly integrated nature, CMOS technology has become an excellent choice for radio frequency (RF) applications. Silicon-on-insulator (SOI) CMOS is especially promising for RF system-on-chip integration because of the reduction in crosstalk between RF and digital circuits and easy integration of high quality passive elements [1], [2]. With the penetration of SOI CMOS into RF applications [3], [4], RF SOI modeling becomes a crucial design issue.

For RF CMOS modeling, the model accuracy hinges upon the extraction of extrinsic gate/source/drain resistance $(R_g/R_s/R_d)$ for small-signal, noise, and large-signal applications. Several studies [5]–[7] have presented resistance extraction methods for SOI metal-oxide-semiconductor field effect transistors (MOSFETs) based on those developed for their bulk counterparts [8], [9]. Among these approaches, the zero method [5], [8] developed under the zero condition (i.e., $V_{\rm GS} = V_{\rm DS} = 0$) is attractive because it simplifies the corresponding equivalent circuit and avoids the error caused by the non-quasi-static (NQS) effect [7]. Based on the equivalent circuit built for bulk MOSFETs under the zero condition without considering the substrate loss [8], the following frequency-independent resistance expressions have been derived to directly determine R_s, R_d, and R_g, respectively

$$\mathrm{Re}(Z_{21}) = \mathrm{Re}(Z_{12}) = R_s \tag{1}$$

$$\mathrm{Re}(Z_{22} - Z_{12}) = R_d \tag{2}$$

$$\mathrm{Re}(Z_{11} - Z_{12}) = R_g. \tag{3}$$

For partially-depleted (PD) SOI MOSFETs, however, (1)–(3) may not be valid due to the existence of the floating body region. In this work, we investigate the RF extrinsic resistance extraction for PD SOI MOSFETs. We will show that, for RF SOI MOSFETs, the coupling path between the source and drain terminals through the quasi-neutral body region makes the resistance expressions behave frequency-dependently. After taking this effect into account, we develop a physical RF extrinsic resistance extraction methodology for PD SOI MOSFETs.

II. Devices and Measurements

The PD SOI MOSFETs used in this study were fabricated using UMC 0.13-μm SOI technology. The thicknesses for gate oxide, SOI layer, and buried oxide are 1.4, 40, and 200 nm, respectively. The presence of kinks in Fig. 1 shows that the devices under study are partially depleted. These RF devices were laid out in the multi-finger and multi-group structure with various finger number NF, group number NG, and finger length W_f for a given gate length L_f (0.12 μm). On-wafer two-port S parameters up to 20 GHz were measured, de-embedded with an open dummy, and then transformed to Z parameters to obtain the resistance versus frequency characteristics.

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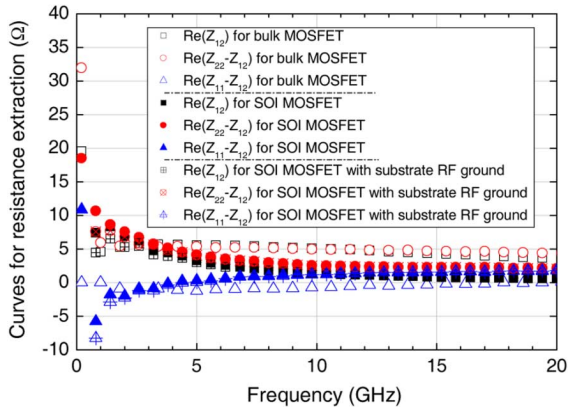

Fig. 2. Resistance curves for the bulk and PD SOI MOSFETs with $L_f/W_f/\mathrm{NF}/\mathrm{NG} = 0.12\ \mu\mathrm{m}/2.4\ \mu\mathrm{m}/16/3$.

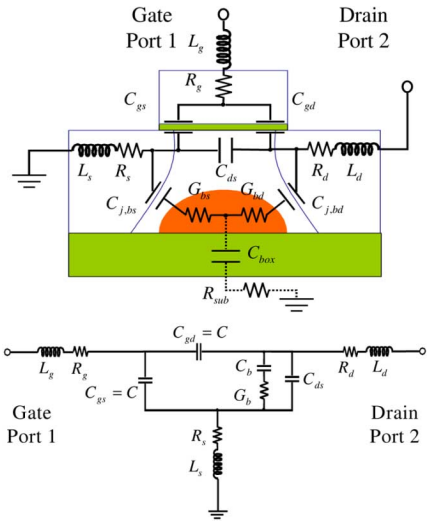

Fig. 3. (a) Cross-sectional view of the zero PD SOI MOSFET. (b) Equivalent circuit for zero PD SOI MOSFETs.

To further minimize possible substrate resistive loss through the buried oxide layer [10], a bias-network connected to the chuck of the probe station was used to provide the substrate dc ground (i.e., back-gate voltage $V_{\mathrm{ES}} = 0$) with RF floating. In fact, as shown in Fig. 2, whether the substrate RF ground is provided or not, the resistance curves are almost unchanged. This indicates that the substrate effect is negligible in this experiment.

III. Results and Discussions

Fig. 2 also compares the resistance versus frequency characteristics under the zero condition for PD SOI MOSFET and its bulk counterpart with identical layout structure and geometry. All of these curves more or less are frequency-dependent. The poor shapes for the bulk MOSFET can be attributed to the complicated and significant substrate resistive loss [11], [12]. For the SOI MOSFET, however, the substrate loss may not be responsible for this frequency-dependent behavior because the thick buried oxide layer in the SOI transistor has provided good isolation from the substrate.

Fig. 3(a) shows a cross-sectional view of the PD SOI MOSFET under the zero condition. The neutral-body coupling path is constituted by source- and drain-side junction capacitances ($C_{j,\mathrm{bs}}$ and $C_{j,\mathrm{bd}}$), and body conductances (G_{bs} and G_{bd}). Its corresponding equivalent circuit without substrate RF ground is depicted in Fig. 3(b). Here, the neutral-body coupling path is represented by a lumped junction capacitance $C_b(=(1/C_{j,\mathrm{bs}}+1/C_{j,\mathrm{bd}})^{-1})$ and a lumped body conductance $G_b(=(1/G_{\mathrm{bs}}+1/G_{\mathrm{bd}})^{-1})$. Based on this equivalent circuit, the following resistance expressions regarding R_s, R_d, and R_g can be derived:

$$\mathrm{Re}(Z_{21}) = \mathrm{Re}(Z_{12}) = R_s + A/(\omega^2 + B) \tag{4}$$

$$\mathrm{Re}(Z_{22} - Z_{12}) = R_d + A/(\omega^2 + B) \tag{5}$$

$$\mathrm{Re}(Z_{11} - Z_{12}) = R_g - 0.5 \times A/(\omega^2 + B) \tag{6}$$

where

$$A = 2C_b^2 G_b/D$$

$$B = G_b^2\left(4C_{\mathrm{ds}}^2 + C^2 + 4C_b^2 + 4CC_{\mathrm{ds}} + 8C_{\mathrm{ds}}C_b + 4CC_b\right)/D$$

and

$$D = \left(C^2C_b^2 + 4C_{\mathrm{ds}}CC_b^2 + 4C_{\mathrm{ds}}^2C_b^2\right).$$

Note that we have assumed $C_{\mathrm{gs}} = C_{\mathrm{gd}} = C$ in the derivation. Equations (4)–(6) predict that the existence of neutral body may cause the resistance curves regarding R_s, R_d, and R_g frequency-dependent and explain the anomalous SOI behavior in Fig. 2. It is worth noting that (4)–(6) will approach (1)–(3), respectively, as the frequency (or angular frequency,

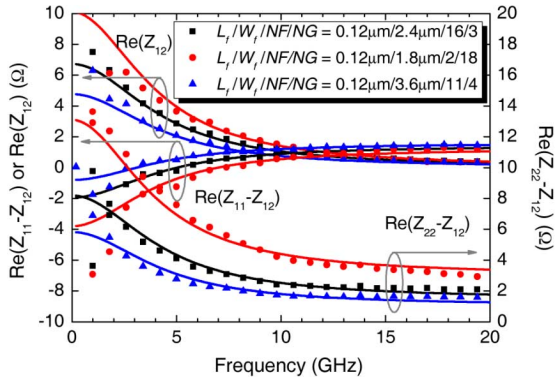

Fig. 4. Modeling results for extrinsic resistance extraction considering the neutral-body effect (points: measured data. lines: model).

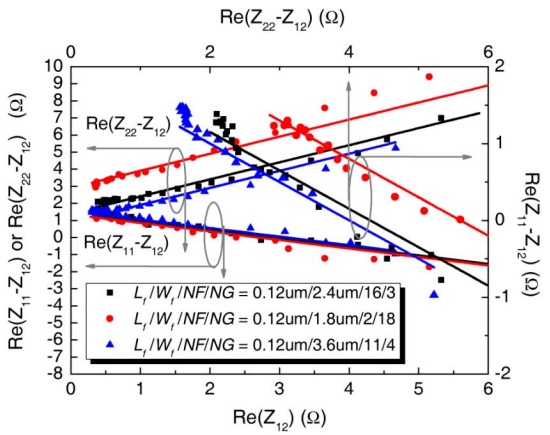

Fig. 5. Correlation between $\mathrm{Re}(Z_{22} - Z_{12})$, $\mathrm{Re}(Z_{12})$ and $\mathrm{Re}(Z_{11} - Z_{12})$ (Points: measured data. lines: model).

TABLE I
MODEL PARAMETERS

	W_{total} (μ m)	A ($\times 10^{21}$F^{-1}.S^{-1})	B ($\times 10^{20}$S^{-2})	R_{ds} (Ω)	R_{gs} (Ω)	R_{gd} (Ω)	R_s (Ω)	R_d (Ω)	R_g (Ω)
FET1	115.2	4.9	7.2	1.4	1.45	2.15	0.1	1.5	1.4
FET2	64.8	6.4	6.4	2.9	1.35	2.8	0.1	3	1.3
FET3	158.4	3.5	7.4	0.9	1.55	2	0.1	1	1.5

The values of $L_f/W_f/NF/NG$ for FET1, FET2 and FET3 are 0.12μ m/2.4μ m/16/3, 0.12μ m/1.8μ m/2/18, 0.12μ m/3.6μ m/11/4, respectively.

ω) approaches infinity. In other words, the extrinsic resistances can be determined by the high frequency asymptotes of $\mathrm{Re}(Z_{12}), \mathrm{Re}(Z_{22} - Z_{12})$, and $\mathrm{Re}(Z_{11} - Z_{12})$. Note that the drain-source coupling capacitance, C_{ds}, will short the neutral-body path and hence eliminate this neutral-body effect at very high frequency.

Using this new model, a physical RF extrinsic resistance extraction methodology for PD SOI MOSFETs can be developed. The model-data comparison for the extraction of R_s, R_d, and R_g with various layout geometries are shown in Fig. 4. It can be seen that the frequency-dependent resistance characteristics are well fitted by our model. Moreover, according to (4)–(6), $\mathrm{Re}(Z_{22}-Z_{12}), \mathrm{Re}(Z_{12})$, and $\mathrm{Re}(Z_{11}-Z_{12})$ are mutually correlated [6] by

$$\mathrm{Re}(Z_{22} - Z_{12}) = \mathrm{Re}(Z_{12}) + R_{\mathrm{ds}} \quad (7)$$

$$\mathrm{Re}(Z_{11} - Z_{12}) = -0.5 \times \mathrm{Re}(Z_{12}) + R_{\mathrm{gs}} \quad (8)$$

$$\mathrm{Re}(Z_{11} - Z_{12}) = -0.5 \times \mathrm{Re}(Z_{22} - Z_{12}) + R_{\mathrm{gd}} \quad (9)$$

where $R_{\mathrm{ds}} = R_d - R_s, R_{\mathrm{gs}} = R_g + 0.5 \times R_s, R_{\mathrm{gd}} = R_g + 0.5 \times R_d$. Equations (7)–(9) have been verified in Fig. 5.

The extracted extrinsic resistances and model parameters $A, B, R_{\mathrm{ds}}, R_{\mathrm{gs}}$, and R_{gd} for each SOI device are listed in Table I. One can find that R_s is nearly equal to zero whereas R_d is not. This is because the RF devices were laid out in the multi-finger and multi-group structure. The multi-source regions were out-connected at two ends of each finger, while the multi-drain regions were out-connected at only one side. In addition, the interconnection between each group may provide additional resistance for the drain terminal and result in discrepancy between R_d and R_s.

Since all the involved device conductance and capacitances in (4)–(6) are proportional to the total gate width $W_{\mathrm{total}} (\approx W_f \times \mathrm{NF} \times \mathrm{NG})$, the parameter A should increase as W_{total} decreases. As indicated in Fig. 4, the resistance curves for the device with smaller W_{total} indeed have a larger deviation from its high-frequency asymptote in the lower frequency regime. Therefore, one can minimize the extraction error resulted from the SOI neutral-body effect by using the wide device.

IV. CONCLUSION

We have investigated the extrinsic resistance extraction for PD SOI MOSFETs. Although the thick buried oxide in SOI devices can block the complicated substrate network, the SOI neutral-body coupling effect may become significant for RF applications. An equivalent circuit considering this effect has been proposed. Based on the equivalent circuit, a new model capturing the frequency dependence of extrinsic resistances has been derived. After considering the impact of quasi-neutral body, we have developed a physically accurate RF extrinsic resistance extraction methodology for PD SOI MOSFETs.

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