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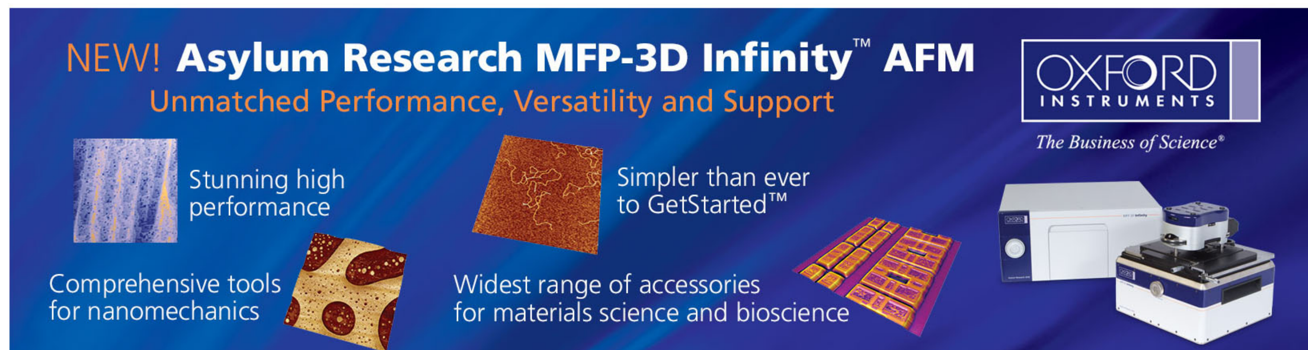

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Nonvolatile low-temperature polycrystalline silicon thin-film-transistor memory devices with oxide-nitride-oxide stacks

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Nonvolatile memory devices with oxide-nitride-oxide stack structures were fabricated on glass substrates using low-temperature polycrystalline silicon technology. The *Fowler-Nordheim* tunneling scheme is more suitable than channel hot carrier injection for the programming of the polycrystalline silicon nonvolatile memory device. A memory window of 1.5 V can be obtained at a programming voltage of 20 V. After 10^4 programming/erasing cycles, a threshold voltage shift of 1.5 V is maintained. Furthermore, the proposed memory device exhibits good retention for 50 h at 60 °C without a significant decline in the memory window. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2736293]

Low-temperature poly-silicon (LTPS) thin film transistors (TFTs) have been adopted in flat panel displays, including active-matrix liquid crystal displays and active-matrix organic light emitting diode displays.[1,2] The major advantage of polycrystalline silicon (poly-Si) TFT technology is its suitability for multifunctional active-matrix displays, because it enables the integration of driver electronics, sensors, memories, and peripheral circuits on the glass substrate to produce system-on-glass (SOG) displays.[3,4] The development of memory devices on glass substrates is critical to SOG technology, especially for data storage and power saving in applications of nonvolatile memories.[5] Nonvolatile memories such as flash memories and electrically erasable programmable read-only memories (EEPROMs) on silicon wafers have been extensively utilized in high-density memories, programmable logic, and microcontrollers.[6] However, fabricating nonvolatile memory devices with favorable electrical characteristics on glass substrates is difficult because of the limit on the glass transition temperature (T_g) of glass substrates.[7] Although EEPROMs with two active poly-Si regions have been manufactured using LTPS technology,[8] the areas that are occupied by memory devices must be considered in obtaining a high aperture ratio of the display panel. In this work, a poly-Si nonvolatile memory, fabricated on a glass substrate, was investigated to achieve good electrical characteristics. The poly-Si nonvolatile memory device with an oxide-nitride-oxide (ONO) stacked dielectric occupies a small area on a display panel. The memory characteristics and electrical reliability were also comprehensively examined.

The inset in Fig. 1 presents the low-temperature poly-Si TFT memory device, referred to as metal/oxide/nitride/oxide/poly-Si (MONOS) memory. It was fabricated on a Corning 1737 glass substrate using LTPS technology, briefly described as follows. A buffer layer of SiO_2 and a 50-nm-thick amorphous hydrogenated silicon (a-Si:H) layer were deposited sequentially by plasma-enhanced chemical vapor deposition (PECVD), and were then dehydrogenated by furnace annealing at 450 °C for 2 h. Following the dehydrogenation, the a-Si film was crystallized by typical XeCl excimer laser annealing (ELA) with a wavelength of 308 nm and an energy density of 400 mJ/cm^2. After the ELA poly-Si layer was islanded, stack structure was formed by the PECVD method with a 15-nm-thick tunnel silicon dioxide layer, a 25-nm-thick silicon nitride layer as a charge trapping center, and a 30-nm-thick blocking oxide layer. The blocking oxide prevents carriers in the gate electrode from being injected into the charge trapping layer by Fowler-Nordheim (FN) tunneling. MoW films were sputter deposited to produce the gate electrodes. Then, n^+ source and drain regions were formed by phosphorous ion doping with a dose of 4×10^{15} ions/cm^2 at 10 keV. Thermal annealing was conducted at 450 °C for 2 h to activate the dopant in the source (S) and drain (D) regions. Both dimensions, channel width

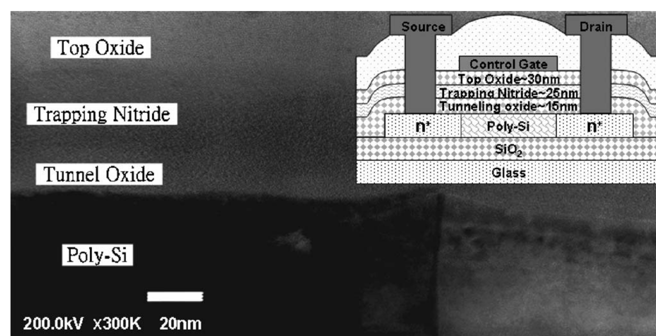

FIG. 1. TEM cross section of $SiO_2/SiN/SiO_2$ (ONO) stack layers on the surface of the poly-Si active region. The inset displays the geometric structure of LTPS TFT memory device with ONO stack dielectrics. The nitride layer plays as a charge trapping layer of the memory device.

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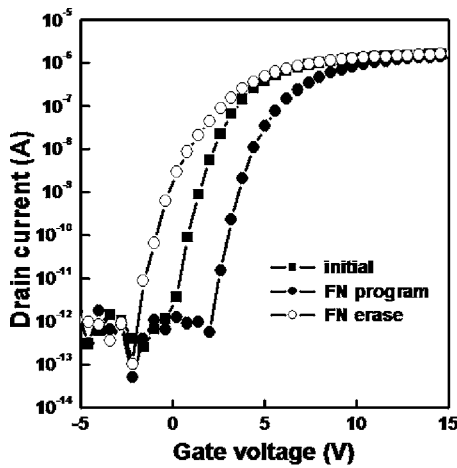

FIG. 2. I_D-V_G characteristics of the MONOS memory device after electrically programed with the gate bias of 20 V and erased at −40 V for 10 ms.

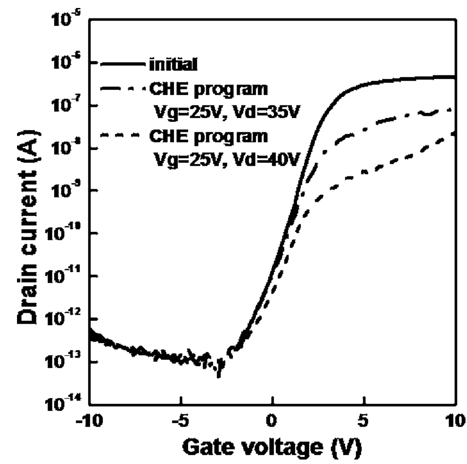

FIG. 3. I_D-V_G characteristics of the MONOS memory device that was programed with CHE scheme.

(W) and channel length (L), of the MONOS memory device are 8 μm. The overlap between the gate metal electrode and the n^+ doping region is 1 μm. Figure 1 shows the transmission electron microscope (TEM) cross section of the ONO films on the surface of the poly-Si active region.

FN tunneling and channel hot electron (CHE) injection are the two main methods for programming nonvolatile memory devices.[9] Figure 2 plots I_D-V_G curves of the MONOS memory device after it was electrically programed with a gate bias of 20 V and erased at −40 V for 10 ms. The programming and erasing were performed using FN tunneling over the entire channel region and in the overlap between the gate and the n^+ S/D regions. The transfer characteristics of the devices were measured at room temperature with V_D=0.1 V, as the gate voltage was varied from −5 to +15 V. The threshold voltage is defined by the criterion $I_D=(W/L)\times 10^{-8}$ A at V_D=0.1 V. The threshold voltage shift of the MONOS memory device is 1.5 V under the aforementioned operating conditions, as presented in Fig. 2. Additionally, the subthreshold swing (~0.54 decade/V) and the mobility (~63.2 cm^2/V s) remain almost constant during programming/erasing (P/E) operations. In the FN P/E operation, the threshold voltage shift is caused by the capture of charges in the nitride film (charge storage layer), and not the degradation of the device.[10,11]

The effects of CHE programming on the electrical characteristics of the MONOS memory device were also studied. Figure 3 plots the I_D-V_G characteristics of a device that was programed by the CHE method. The electrical degradation of the MONOS memory device was carefully observed. Traps in the grain boundaries of the poly-Si channels in the poly-Si TFT devices markedly affect electrical performance and reliability. The impact ionization activities of energetic carriers in a poly-Si TFT are enhanced by both the floating body effect and these traps, and contribute to the formation of the dangling bonds in the poly-Si film.[12] The CHE programming procedure provides electrons with high energy to enable them to pass from the channel into the charge storage layer, SiN_x. Accordingly, a large voltage drop between the drain and the control gate is typically used in CHE programming.[9] However, the transport of some high-energy electrons can degrade the tunneling oxide as they penetrate the tunneling layer. The degradation is believed to be caused mostly by the generation of traps at the interface between the low-temperature PECVD gate oxide and the poly-Si layer. Furthermore, avalanche breakdown occurs near the drain side of the MONOS memory device. A poly-Si TFT, fabricated on a glass substrate, exhibits the parasitic bipolar transistor activity, which causes the kink effect as in silicon-on-insulator devices.[13] The added drain current promotes impact ionization, worsening the floating body effect and causing premature breakdown. Therefore, channel hot electron injection is unsuitable for the programming of MONOS memory devices. FN tunneling that occurs in either the gate/drain overlap region or the channel region is acceptable for programming of poly-Si TFT memory devices.

Figure 4(a) plots the endurance characteristics of the MONOS memory device following various numbers of P/E cycles. The memory device can be P/E using the FN scheme

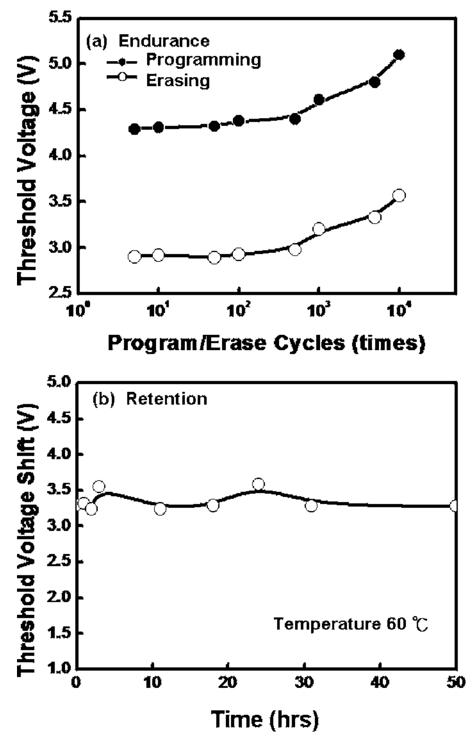

FIG. 4. (a) Endurance characteristics of the MONOS memory device, after various numbers of program/erase cycles. (b) Retention characteristics of MONOS-type memory devices measured after various periods, as the devices were heated at 60 °C.

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with positive (+20 V) and negative (−40 V) voltage pulses, respectively. The threshold voltage window is 1.5 V at a P/E time of 10^{-2} s. The memory window of 1.5 V is sufficiently large to identify digital states (0 or 1) in a logic memory circuit. The MONOS memory device maintains a wide threshold voltage window even after 10^4 P/E cycles. However, the memory device exhibits electrical degradation following 10^4 P/E circles. The upward threshold voltage shift may be caused by the creation of interface traps and the trapping of charges in the tunneling oxide.[13,14] The threshold voltage depends also on the oxide charges and the deep trap states in the poly-Si film.[11,15,16] In Fig. 4(b), the threshold voltage shift of the MONOS memory device was measured after various periods, as the devices were heated at 60 °C. MONOS memory exhibits good retention for 50 h, without a significant decline in the memory window, ΔV_t. It is robust when used in nonvolatile memory technology for active-matrix display applications.

In summary, the characteristics of a MONOS-type memory device that was fabricated by LTPS TFT technology were extensively studied. The ONO stack gate dielectrics in the MONOS poly-Si memory device serve as tunneling oxide/charge storage layer/control oxide layers. The CHE scheme was experimentally observed to be inappropriate for programming of MONOS memory devices, because of electrical degradation. FN P/E procedures yield a memory window of 1.5 V for a P/E pulse time of 10 ms, without device degradation. Additionally, the proposed MONOS memory device exhibits good data endurance, maintaining a large threshold voltage window even after 10^4 P/E cycles.

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[1] Y. Oana, J. Soc. Inf. Disp. **9**, 169 (2001).
[2] J. Y. Kwon, J. S. Jung, K. B. Park, J. M. Kim, H. Lim, S. Y. Lee, J. M. Kim, T. Noguchi, J. H. Hur, and J. Jang, SID Int. Symp. Digest Tech. Papers **37**, 1358 (2006).
[3] B. Lee, Y. Hirayama, Y. Kubota, S. Imai, A. Imaya, M. Katayama, K. Kato, A. Ishikawa, T. Ikeda, Y. Kurokawa, T. Ozaki, K. Mutaguch, and S. Yamazaki, *IEEE ISSCC* (IEEE, New York, 2003), 1, pp. 164–165.
[4] J. Kimmel, J. Hautanen, and T. Levola, Proc. IEEE **90**, 581 (2002).
[5] H. Asada, SID Int. Symp. Digest Tech. Papers **36**, 1434 (2005).
[6] P.. Hasler and T. S. Lande, *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* (IEEE, New York, 2001), Vol. 48, pp. 1–3.
[7] O. Nast, S. Brehme, D. H. Neuhaus, and S. R. Wenham, IEEE Trans. Electron Devices **46**, 2062 (1999).
[8] M. Cao, T. Zhao, K. C. Saraswat, and J. D. Plummer, IEEE Electron Device Lett. **15**, 304 (1994).
[9] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, Proc. IEEE **85**, 1248 (1997).
[10] C. W. Chen, T. C. Chang, P. T. Liu, H. Y. Lu, T. M. Tsai, C. F. Weng, C. W. Hu, and T. Y. Tseng, Electrochem. Solid-State Lett. **8**, H69 (2005).
[11] M. Hack, A. G. Lewis, and I. W. Wu, IEEE Trans. Electron Devices **40**, 890 (1993).
[12] M. Valdinoci, L. Colalongo, G. Baccarani, G. Fortunato, A. Pecora, and I. Policicchio, IEEE Trans. Electron Devices **44**, 2234 (1997).
[13] S. S. Chen and J. B. Kuo, Solid-State Electron. **41**, 447 (1997).
[14] N. Bhat, M. Cao, and K. C. Saraswat, IEEE Trans. Electron Devices **44**, 1102 (1997).
[15] J. C. Kim, J. H. Choi, S. S. Kim, and J. Jang, IEEE Electron Device Lett. **25**, 182 (2004).
[16] N. D. Young, IEEE Trans. Electron Devices **43**, 450 (1996).

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