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Guang-Li Luo, Yen-Chang Hsieh, Edward Yi Chang, M. H. Pilkuhn, Chao-Hsin Chien, Tsung-Hsi Yang, Chao-Ching Cheng, and Chun-Yen Chang

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High-speed GaAs metal gate semiconductor field effect transistor structure grown on a composite $Ge/Ge_xSi_{1-x}/Si$ substrate

Guang-Li Luo[a)]
National Nano Device Laboratories, Hsinchu, Taiwan 30078, Republic of China

Yen-Chang Hsieh, Edward Yi Chang, and M. H. Pilkuhn
Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan 30050, Republic of China

Chao-Hsin Chien, Tsung-Hsi Yang, Chao-Ching Cheng, and Chun-Yen Chang
Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan 30050, Republic of China

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In this study we used a low-pressure metal organic vapor phase epitaxy method to investigate the growth of GaAs metal gate semiconductor field effect transistor (MESFET) structures on a Si substrate. The buffer layer between the Si substrate and the grown GaAs epitaxial layers was a composite $Ge/Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ metamorphic layer. We used transmission electron microscopy to observe the microstructures formed in the grown $GaAs/Ge/Si_xGe_{1-x}/Si$ material and atomic force microscopy to analyze the surface morphology and the formation of antiphase domains in the GaAs epitaxial layers. The measured Hall electron mobility in the channel layer of a MESFET structure grown on a 6° misoriented Si substrate was 2015 $cm^2\ V^{-1}\ s^{-1}$ with a carrier concentration of $5.0\times10^{17}\ cm^{-3}$. The MESFET device fabricated on this sample exhibited good current-voltage characteristics. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2722245]

I. INTRODUCTION

Heteroepitaxial growth of GaAs on Si substrates has attracted a great deal of attention in recent years because potentially it can be integrated into Si CMOS devices with the aid of high-*k* gate dielectrics[1] to enhance performance and extend the roadmap. GaAs has a number of advantages over Si for some applications because of its higher electron mobility, wider band gap, and direct band gap. Nevertheless, silicon has several advantages over GaAs, including the ability to fabricate devices over larger areas using mature processes and its higher thermal conductivity. The main problems that must be overcome when growing GaAs on Si by heteroepitaxy are the large lattice mismatch (4%) and the difference in the thermal expansion coefficients (63%) of these two materials,[2] which can cause high-density dislocations in the epitaxial GaAs layer. Several methods for reducing the dislocation density have been reported, such as using strained layer superlattices (SLs) to confine dislocations and or using thermal cycle annealing to reduce threading dislocations.[3] Motorola has reported a molecular beam epitaxy (MBE)-grown GaAs metal gate semiconductor field effect transistor (MESFET) on Si using a $SrTiO_3$ buffer layer. Unfortunately, it is difficult to grow the $SrTiO_3$ buffer layer in the MBE system.[4]

Germanium is only 0.07% lattice mismatched with GaAs, and the thermal expansion coefficient difference between Ge and GaAs is only 2%, i.e., the lattice constant and thermal expansion coefficients of Ge are almost identical to those of GaAs. Although using a Ge layer as a buffer can solve the lattice mismatch problem between GaAs and Si, the question arises as to how a high-quality Ge buffer layer can be grown on Si because Ge also has a 4.2% lattice mismatch with Si.

Many publications[5,6] have described the growth of a pure Ge layer on a Si substrate using a graded SiGe buffer layer. The disadvantages are that the graded SiGe buffer layer must be sufficiently thick and that its surface must possess a high degree of roughness and a crosshatched pattern. A method utilizing chemical-mechanical polishing (CMP) was necessary to grow a relaxed graded SiGe buffer up to a 100% Ge layer.[6]

In a previous report, we proposed a simple Ge/SiGe buffer structure for the growth of high-quality GaAs layers on Si (100) substrates.[7] We demonstrated that such buffer structures are thin, have smooth surfaces, and exhibit a strong capability to block dislocations. This buffer growth technique has also been used by other authors for the fabrication of a high-performance Ge detector[8] and for high-quality ZnSe heteroepitaxial growth on Si.[9] To prepare such a Ge/SiGe buffer structure (see Fig. 1), a $Si_{0.1}Ge_{0.9}$ layer is first grown. Because of the large lattice mismatch between this layer and the Si substrate, many dislocations are intentionally generated in this first $Si_{0.1}Ge_{0.9}$ layer. A second $Si_{0.05}Ge_{0.95}$ layer and a third Ge layer are subsequently grown. The resulting $Ge/Si_{0.05}Ge_{0.95}/Si_{01}Ge_{09}$ and $Si_{0.05}Ge_{0.95}$ interfaces trap the upward-propagating dislocations very effectively; thereby, the dislocation density in the Ge layer is reduced significantly.

A common problem encountered at the GaAs/Ge interface is the formation of antiphase domains (APDs), which occur when growing polar GaAs on nonpolar Ge. Several models have been reported for suppression of APDs through the use of Ge(100) wafers misoriented by 6° toward the

[a)]Electronic mail: glluo@mail.ndl.org.tw

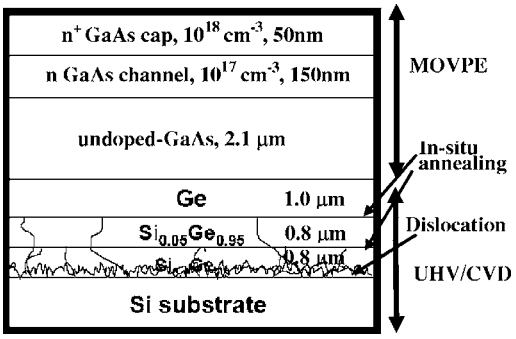

FIG. 1. Schematic illustration of a GaAs MESFET fabricated on a Si substrate.

<110> direction.[10,11] As growth proceeds, the initial nuclei grown only at the steps coalesce so that an APD-free GaAs is achieved. Another problem encountered during the growth of GaAs on Ge is the diffusion of Ge into the GaAs layer,[12,13] which acts as an *n*-type dopant in GaAs.

In this study, a Ge/SiGe buffer was first grown through ultrahigh-vacuum chemical vapor deposition (UHV/CVD). The sample was then transferred to another metal organic vapor phase epitaxy (MOVPE) system to grow the GaAs MESFET structure. Herein, we describe this GaAs/Ge/SiGe/Si heterostructure in detail.

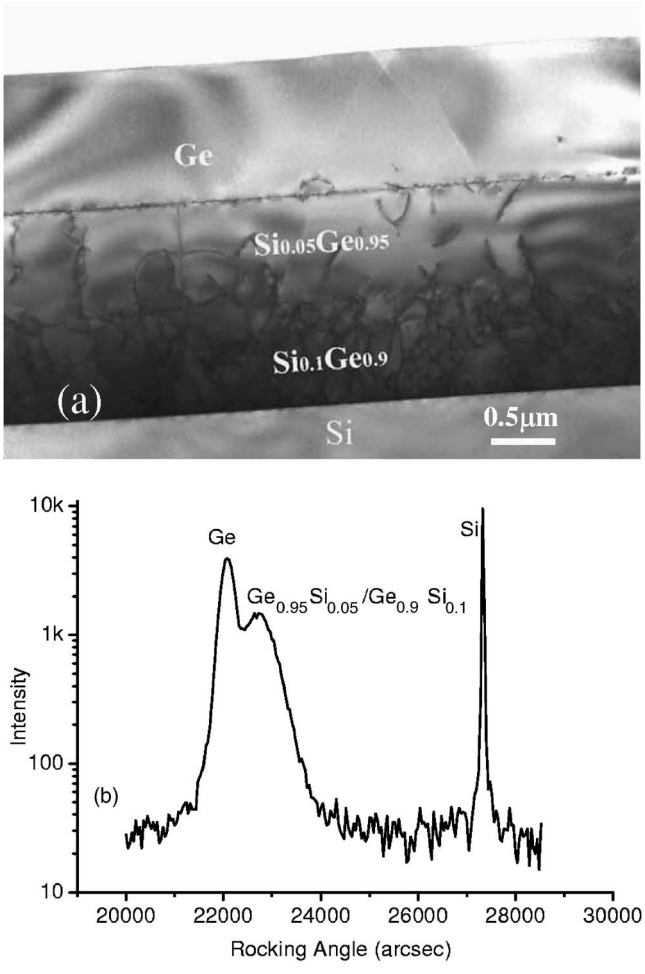

FIG. 2. (a) Cross-sectional TEM image and (b) x-ray rocking curve of stacked Ge and SiGe epilayers on a Si substrate.

II. EXPERIMENT

The growth of the SiGe and Ge buffer layers was undertaken using an UHV/CVD system operated at a base pressure below 2×10^{-8} Torr. Disilane (Si_2H_6) and germane (GeH_4) were used as source gases for Si and Ge, respectively. First, a 4-in. Si (100) wafer with a 6° misorientation toward the ⟨110⟩ direction was subjected to a standard RCA cleaning and a 10 s dip in 10% HF solution and then went through a high-temperature (800 °C) baking in the growth chamber for 5 min. Next, 0.8 μm $Si_{0.1}Ge_{0.9}$, 0.8 μm $Si_{0.05}Ge_{0.95}$, and 1.0 μm Ge layers were grown sequentially at 400 °C. Between successive layers, the growth was interrupted for *in situ* annealing for 15 min at 750 °C. Here, we did not grow Si buffer layer before $Si_{0.1}Ge_{0.9}$ growth, because we did not find any difference. After the growth of this Ge/SiGe/Si metamorphic structure was complete, the sample was loaded out and immediately transferred to a LP-MOVPE system for growth of GaAs at 630 °C under a reactor pressure of 40 Torr. The sources of Ga and As were triethylgallium (TEGa) and AsH_3, respectively. Diluted SiH_4 in H_2 was used as an *n*-type dopant. The investigations in this study were threefold. The first involved the formation of antiphase boundaries at different growth temperatures. For comparison, we attempted to grow GaAs buffer layers at different temperatures on Ge/SiGe/Si structures by using 0°-misoriented Si(100) substrates. In this case, GaAs buffer layers each having a thickness of 0.1 μm were grown at 450, 500, and 550 °C, respectively. Following the growth of each GaAs buffer layer, an undoped GaAs layer having a thickness of ~2.2 μm was grown at 630 °C. In our second investigation, we grew the same structures on Si(100) substrates with a 6° misorientation toward the ⟨110⟩ direction. This study focused on suppression of the antiphase boundaries using misoriented substrates. Finally, based on the material structure that was grown on a 6° misoriented Si substrate, GaAs MESFET devices having a gate length of 0.5 μm and a width of 100 μm were fabricated using standard III-V MESFET processing techniques. The source-drain ohmic contacts were AuGe/Ni/Au formed by rapid thermal annealing, while the gate metallization was TiPtAu. Throughout this study, transmission electron microscopy (TEM) was used to measure the thickness of the epitaxial layers and observe the dislocation distribution; double-crystal x-ray diffraction (DCXRD) was used to analyze the crystalline quality.

III. RESULTS AND DISCUSSION

A. Effect of low-temperature GaAs buffers on size of APDs

Figure 2(a) displays a cross-sectional TEM image of the Ge buffer layers grown on the Si substrate. The total thickness of the epitaxial structure was only ~2.6 μm. It can be found there were a large number of dislocations located in the $Si_{0.1}Ge_{0.9}$ layer near the $Si_{0.1}Ge_{0.9}$/Si interface due to the large Ge composition difference between $Si_{0.1}Ge_{0.9}$ and Si. The upward-propagated dislocations were bent sideways and terminated very effectively by the $Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ and $Ge/Si_{0.05}Ge_{0.95}$interfaces because of the compressive stress induced at the interfaces. Very few threading dislocations

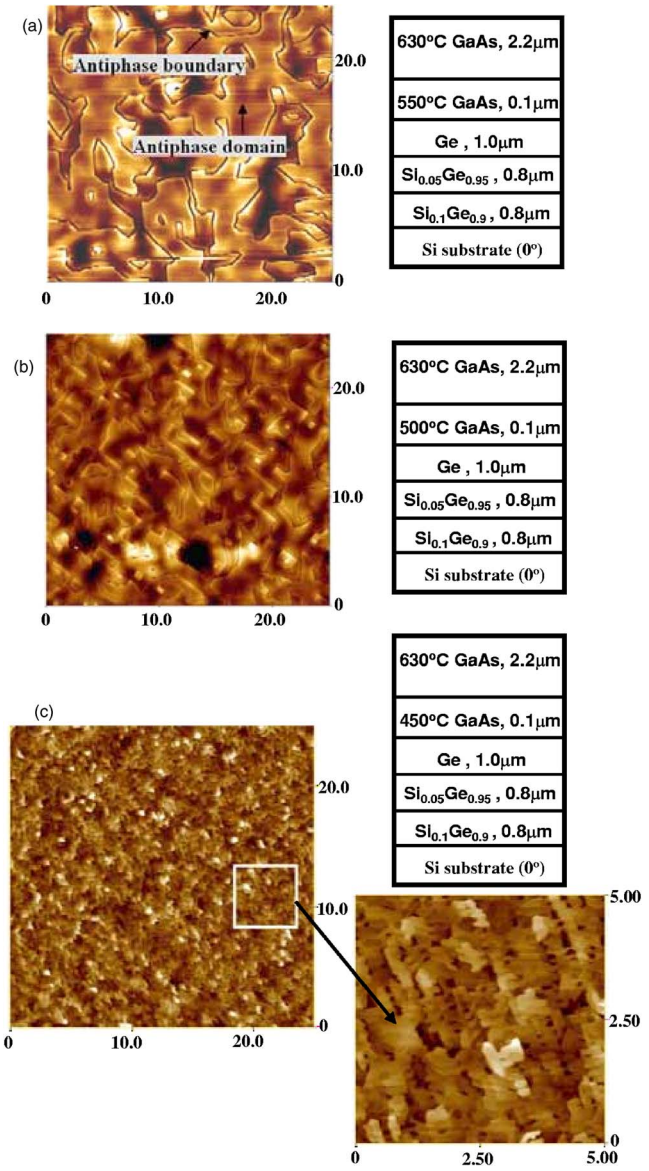

FIG. 3. (Color online) AFM images of GaAs layers grown on the composite $Ge/Si_xGe_{1-x}/Si$ substrate (the Si substrate was 0° misoriented) with different low temperature GaAs buffers (a) 550, (b) 500, and (c) 450 °C. Scanned area: 25×25 μm.

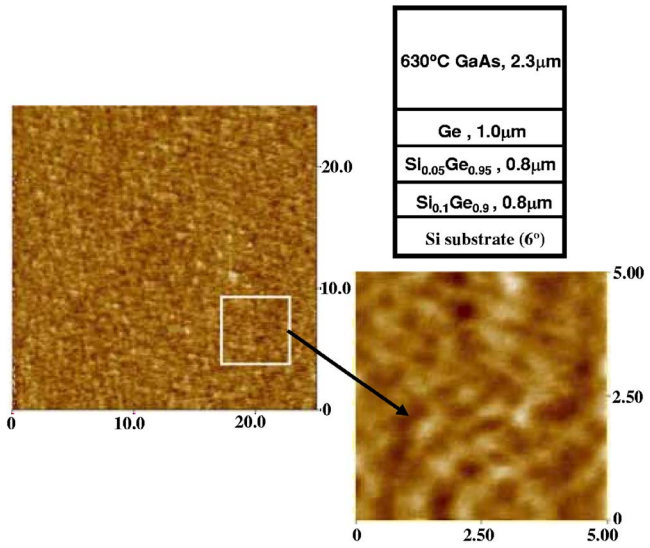

FIG. 4. (Color online) AFM image and layer structures of GaAs grown on the composite $Ge/Si_xGe_{1-x}/Si$ substrate at 630 °C (the Si substrate was 6° misoriented). Scanning area: 25×25 μm.

could propagate into the top Ge layer. Details of the growth of the Ge/SiGe buffer layers can be found elsewhere.[7] Figure 2(b) displays the rocking curve of the stacked Ge and SiGe epilayers. The intense and sharp Ge peak indicates that the grown top Ge layer was of a very high crystalline quality.

A LP-MOVPE system was used to grow GaAs layers on the above-mentioned composite Ge/SiGe/Si substrates. Although the low lattice mismatch of the GaAs/Ge system suggests that it should be almost dislocation-free, considerable problems remained during the epitaxy between the polar (GaAs) on nonpolar (Ge) semiconductors, resulting in the formation of antiphase domains (APDs). On (100) surfaces, the atoms nucleate at both steps and terraces with the latter having a crystal orientation that is rotated by 90°; the phase (or domain) polarity depends on the growth temperature and the substrate misorientation angle.[10] At the boundary between two APDs, an antiphase boundary (APB) is created. The APB consists of wrong bonds of As–As or Ga–Ga, which can provide deep levels in the forbidden gap and act as nonradiative recombination centers. We attempted to suppress APBs by growing low-temperature GaAs buffer layers on the Ge surfaces with Si substrates having a 0° misorientation. Unfortunately, we could not control the adatoms to nucleate only at steps or terraces; i.e., the GaAs layer could not be grown in only one domain. Figure 3(a) presents the surface morphology of the GaAs layer grown on the 0°-misoriented substrate at 550 °C. Two domains are clearly evident. The winding dark lines between two antiphase domains are antiphase boundaries. Taken together with Figs. 3(b) and 3(c), we observed that the sizes of the APDs increased upon increasing the growth temperature of the GaAs buffer layer, possibly because a higher temperature increased the diffusion length of the surface species. At a low growth temperature, the mobility of the atoms was kinetically delayed, such that atoms could only diffuse a short distance before they became incorporated. As a result, we observe high-density APDs of a smaller size in Fig. 3(c). As a consequence of the formation of APBs, the surface of each sample was very rough. For the sample for which the GaAs buffer layer was grown at 550 °C, the surface root mean square (rms) roughness was 70.35 Å and the roughness average (R_a) was 60.61 Å.

B. Suppression of APBs using misoriented Si substrates

The low-temperature GaAs buffer could not sufficiently suppress the APBs. The most common method for avoiding the formation of APDs at GaAs/Ge interfaces is the use of misoriented substrates and a sufficient amount of thermal annealing. The suppression of APDs can be achieved by using a Si wafer with a misorientation angle. For substrates having a larger misorientation angle ($\geqslant6°$), in which the terraces between the steps are very narrow, the steps are so close to each other that the nuclei can be formed only at the steps, with a diminished possibility for two-dimensional

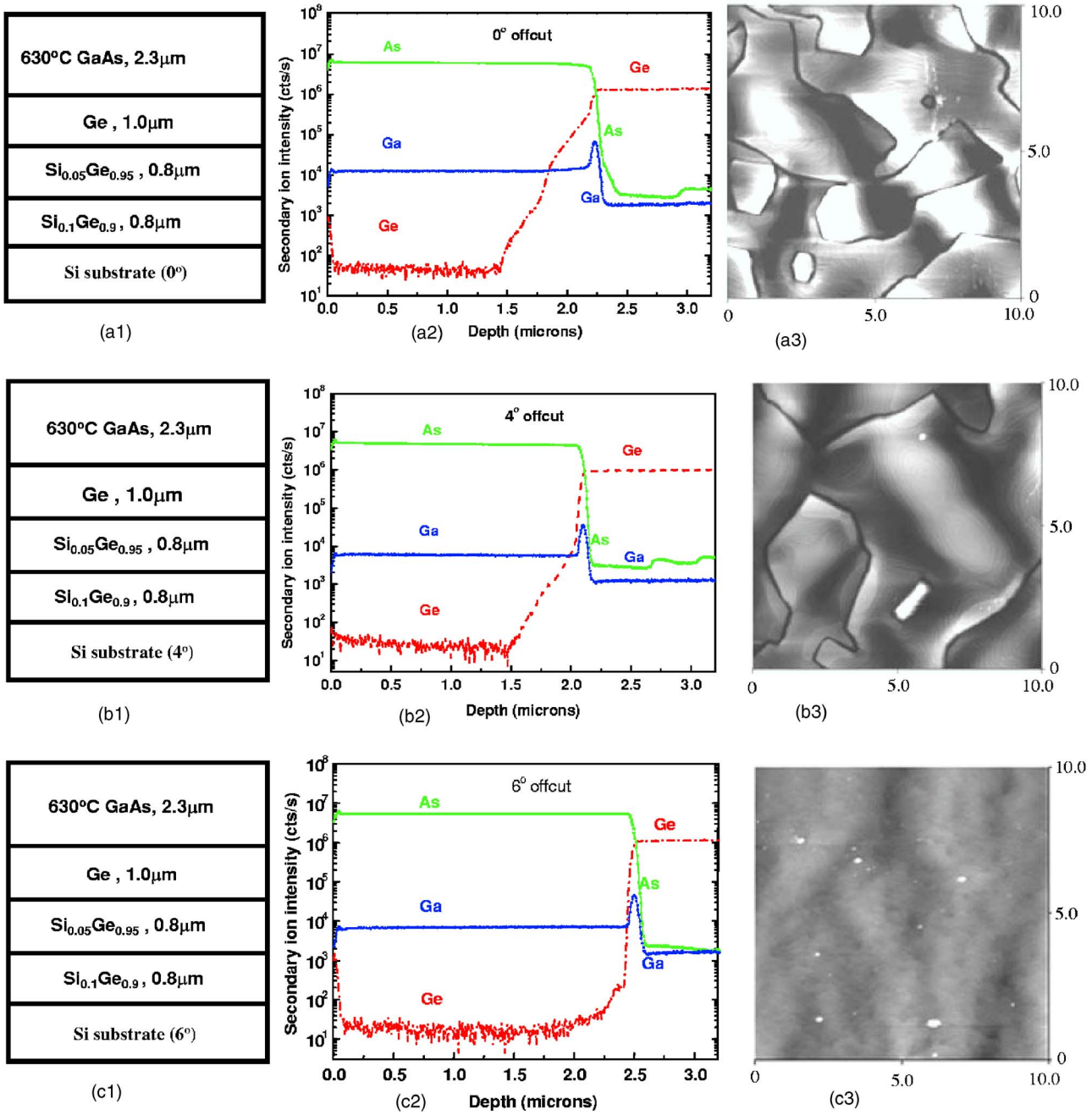

FIG. 5. (Color online) Layer structures, SIMS profiles, and AFM images for the GaAs layers grown on the $Ge/Si_xGe_{1-x}/Si$ substrates at misorientation angles of ($a1-a3$) 0°, ($b1-b3$) 4°, and ($c1-c3$) 6°.

nucleation on the terraces. As the growth proceeds, the initial nuclei that formed at the steps coalesce so that only one domain of GaAs is achieved; other domains associated with nucleation on terraces are avoided. Consequently, a blanket GaAs layer with a single sublattice orientation (or phase) can be grown on a $\geqslant 6°$ misoriented (100) surface. In this study, we grew the sample on a Ge/SiGe/Si substrate at a 6° misorientation angle. Here, the growth temperature was 630 °C; no low-temperature GaAs buffer was employed. The atomic force microscopy (AFM) image in Fig. 4 indicates that no APDs existed on the surface. The measured rms roughness was only 7.35 Å and the value of R_a was only 5.81 Å. We believe that the reason for this smoothness was the suppression of APBs on the misoriented (100) surface.

We used secondary ion mass spectrometry (SIMS) techniques to verify the interdiffusion of the Ge layer into GaAs. This technique provides quantitative measurements of the levels of dopants and impurities in semiconductors. As mentioned above, the formation of APBs depended primarily on the magnitude of the misorientation angle of the Si (100) substrate. Figures 5(a)–5(c) display the depth profiles for Ge diffusion into the GaAs layer. We observed different lengths of Ge diffusion into the GaAs layer according to the various misorientation angles of the Si substrate. Figure 5(a) indicates that the Ge diffused by ~0.75 μm into the GaAs layer when the substrate was misoriented by 0°. When the degree of substrate misorientation was greater than 6°, the Ge diffusion into the GaAs layer was only ~0.25 μm [see Fig.

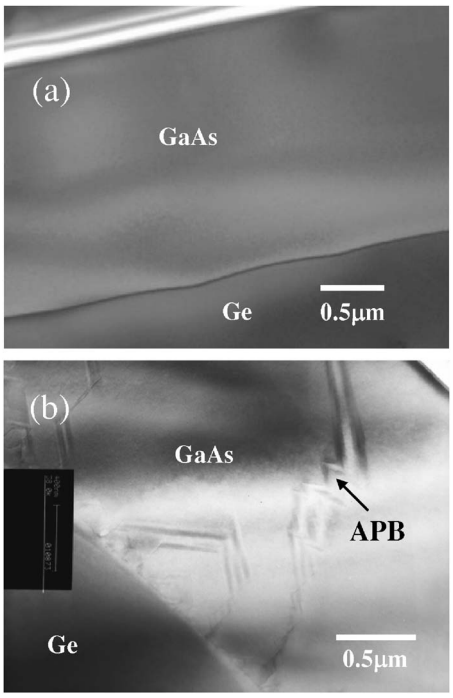

FIG. 6. TEM images of GaAs grown on composite Ge/SiGe/Si substrates at Si substrate misorientation angles of (a) 6° and (b) 0°.

5(c)]. Here, the APBs may be considered as routes for Ge diffusion into the GaAs layer during the growth process. The lowest degree of Ge diffusion into GaAs in Fig. 5(c) may be due to the total suppression of the formation of APDs. Figure 6(a) displays the GaAs layer grown on the 6° misoriented Si substrate; no twins or lattice defects appear around the GaAs/Ge interface. Figure 6(b) presents the GaAs layer grown on the 0° misoriented Si substrate ; we observed APBs penetrating through the GaAs layer from the Ge layer. These results suggest that a relationship exists between the degree of Ge diffusion and the formation of APBs.

C. Material characterization and MESFET devices

MESFET devices were fabricated on the material structure displayed in Fig. 6(a). In this sample, the total thickness of GaAs was 2.3 μm μm, on top of which were grown a 1500 Å thick channel (Si doped at 5.0×10^{17} cm^{-3}) and a 500 Å contact layer (Si doped at 5×10^{18} cm^{-3}). A double-crystal x-ray measurement of the sample displays five peaks in the diffraction spectrum; i.e., for GaAs, pure Ge, $Si_{0.1}Ge_{0.9}$, $Si_{0.05}Ge_{0.95}$, and the Si substrate (Fig. 7). The full width at half maximum (FWHM) for the GaAs peak was 120 arcsec. By using the common formula $N=(\Delta\omega/b)^2$ [where N is the dislocation density, $\Delta\omega$ is the FWHW, and b is the Burgers vector (0.4 nm)],[14–16] we roughly estimate the dislocation density in GaAs to be 6.0×10^6 cm^{-2}. We also did the etch pits test by using KOH etching; the pit density is about 7×10^6/cm^2, which is of the same order as the value of XRD measurement. A Hall measurement was performed on the GaAs/Ge/SiGe structure at room temperature using the van der Pauw method. The measured electron mobility was 2015 cm^2 V^{-1} s^{-1} with a carrier concentration of 5.0×10^{17} cm^{-3}. Figure 8(a) displays the drain current-voltage

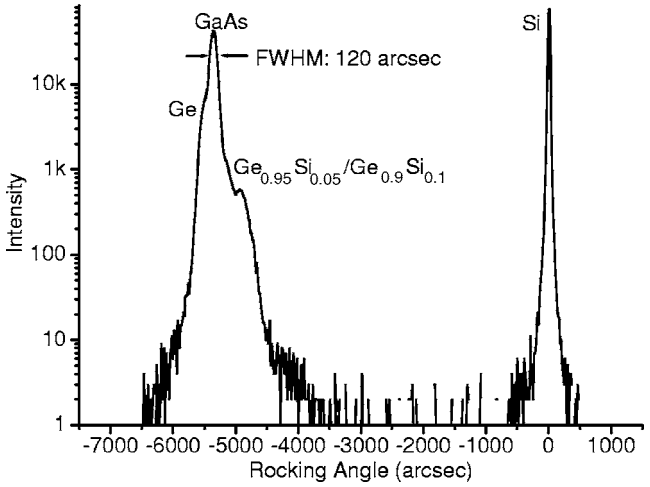

FIG. 7. Double-crystal x-ray diffraction spectrum of a GaAs layer grown on a composite $Ge/Si_xGe_{1-x}/Si$ substrate.

(I-V) characteristics for the MESFET device; the good pinch-off behavior indicates the good crystallinity of the GaAs layer grown on the Si substrate. The saturation current is 142 mA/mm at gate voltage $V_G=0$ V. The transfer characteristic of Fig. 8(b) displays a maximum transconductance of 150 mS/mm at drain-source voltage $V_{DS}=1.5$ V. These results suggest that the material structure grown in this work is very promising for the fabrication of Si-based GaAs channel high-speed electronic devices.

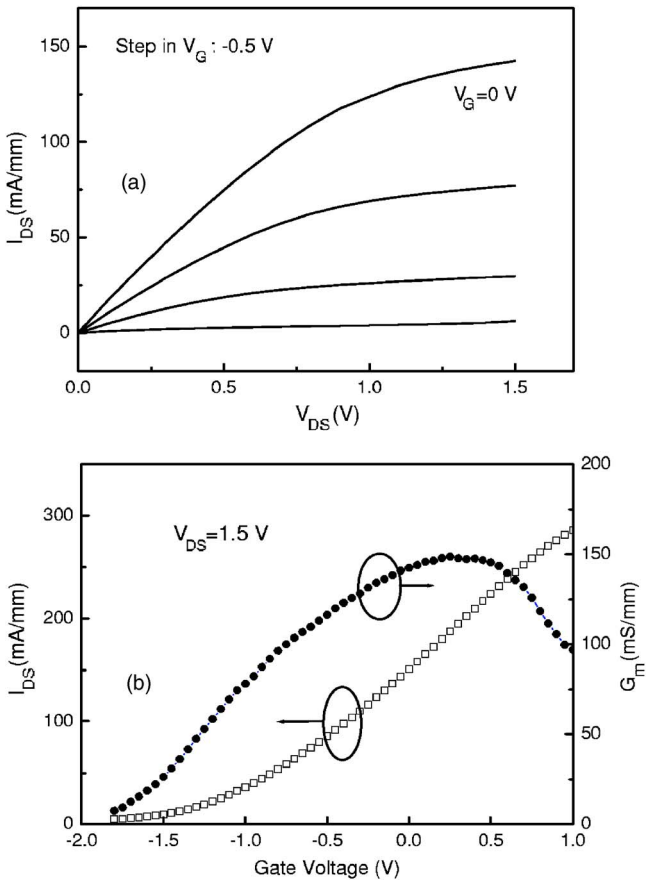

FIG. 8. (Color online) (a) Drain I-V characteristics and (b) transfer characteristics of a fabricated 0.5×100 μm^2 MESFET device based on GaAs grown on a composite $Ge/Si_xGe_{1-x}/Si$ substrate at a 6° misorientation.

IV. CONCLUSIONS

A $Ge/Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}$ buffer layer was used to accommodate the strain induced between a Si substrate and a GaAs layer and to prevent threading dislocations from penetrating into the top GaAs layers. A misoriented substrate ($\geqslant 6°$) was employed to suppress APB formation in the GaAs layer. We found that the sizes of the APDs depended upon growth temperature of the GaAs buffer layers. The Hall electron mobility of the GaAs channel layer grown on the $Ge/Si_xSi_{1-x}/Si$ structure was 2015 $cm^2\ V^{-1}\ s^{-1}$ with a carrier concentration of $5.0\times 10^{17}\ cm^{-3}$. A GaAs MESFET device fabricated on this material exhibited good dc characteristics.

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