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Resistance switching properties of sol–gel derived $SrZrO_3$ based memory thin films

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Abstract
Sol–gel derived $SrZrO_3$ based metal/insulator/metal (MIM) devices were fabricated to study their reversible resistance switching properties operated by dc voltage sweep and voltage pulses. The leakage-state of the device is changed from the original-state and finally switched between the high leakage-state (H-state) and the low leakage-state (L-state). The resistance ratio between the H-state and the L-state is about 10^4, and the leakage-states are not changed without power supply, which is suitable for nonvolatile memory application. The conduction mechanisms of the original-state, the H-state and the L-state obey Schottky emission, Frenkel–Poole emission and Ohmic conduction, respectively. The first device resistance switching, called the forming process, changed from the original-state to the H-state. The switching time from the H-state to the L-state is much longer than that from the L-state to the H-state and that of the forming process. The decay behaviours of leakage current after resistance switching are influenced by pulse width and voltage stress directions. The switching time can be accumulated to switch the device from the H-state to the L-state, which could be a guide to multi-level memory applications. The model of conducting paths can well explain the electrical behaviours of our resistance switching devices.

1. Introduction

Perovskite structured ceramics have been investigated for many applications such as gate dielectrics [1], dynamic random access memory (DRAM) [2], superconductor [3], ferroelectric memory [4] and tunable device [5]. Recently, perovskite ceramics have attracted much interest for their reversible resistance switching properties used for making resistive random access memory (RRAM) [6,7]. Following the popularity of mobile equipment, nonvolatile memory (NVM) plays an important role in the electronic industries. Nonvolatile memory should keep the stored information without power supply for a long time. Nowadays flash memory is the mainstream of nonvolatile memory. However, flash memory has drawbacks including high operation voltage, low operation speed and low endurance. RRAM is a promising candidate for the next generation of nonvolatile memory due to its low operation voltage, low power consumption, long retention time, simple structure and non-destructive readout [8]. Various materials are investigated for the RRAM application, such as $SrZrO_3$, polymer and binary metal oxide [9]. Beck and co-workers [6, 10] adopted the (100)-oriented $SrTiO_3$ crystals doped with 0.2% Cr grown by flame fusion and 0.2% Cr doped $SrZrO_3$ thin films grown by pulsed laser deposition to study their resistive switching behaviours. The leakage current drops to a lower value with biasing a sufficiently

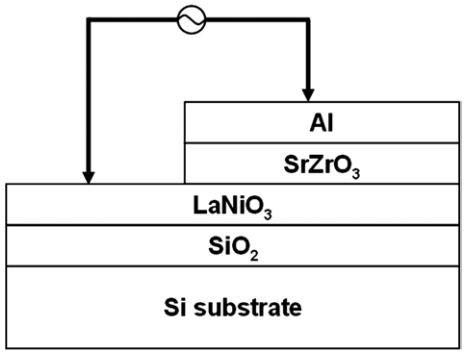

Figure 1. Schematic diagram of the Al/$SrZrO_3$/$LaNiO_3$ structure.

large positive voltage while the leakage current violently increases with biasing a sufficiently large negative voltage. The reversible resistance switching phenomenon was demonstrated in their study. However, there are only a few reports about the RRAM fabricated by perovskite structured ceramics on Si substrates and it is still unclear about the resistance switching mechanisms. In this study, the sol–gel method is adopted to deposit the perovskite $SrZrO_3$ (SZO) resistive layer. The resistance switching properties can be operated by dc bias sweep and voltage pulses. The influence of applied voltage pulses on the resistance switching behaviour is investigated. In addition, the decay behaviours of the leakage current after resistance switching by voltage pulses is also characterized. Based on the resistance switching properties and decay behaviours of the leakage current, the behaviours of resistance switching can be well explained by the model of conducting paths.

2. Experimental procedures

The 4 in. boron-doped p-type (1 0 0) silicon wafers were cleaned by the standard Radio Corporation of America (RCA) cleaning process and then a 200 nm thick SiO_2 layer was thermally grown in a furnace to isolate the leakage current from the silicon substrate. Then, a 100 nm thick $LaNiO_3$ (LNO) film was deposited at 250 °C by radio-frequency (rf) magnetron sputter as the bottom electrode [11]. The 0.1 M SZO precursor solution with 0.2 mol% vanadium (V) and 0.1 mol% thulium (Tm) dopant was spin-coated on the $LaNiO_3$/SiO_2/Si substrates to form the sol–gel films [12]. Then such a deposited layer was heat-treated at 200 °C for 10 min and then pyrolyzed at 500 °C for 30 min. The coating and heating steps were repeated to obtain a 50 nm thick SZO film. Finally, a 300 nm thick Al film was deposited by a thermal evaporator to form a metal/insulator/metal (MIM) structure, and patterned by a metal mask as the top electrode of area 2.86×10^{-4} cm^2 to perform the electrical measurements, as shown in figure 1. Agilent 81110A was used to generate voltage pulses with the rise time of 2 ns and Agilent 4155C was used to record the current–voltage (I–V) characteristics. For transient measurement, after applying a voltage pulse on the MIM structure, the 4155C signals were switched by an Agilent E5250A low-leakage switch mainframe to characterize the I–V properties of the MIM structure.

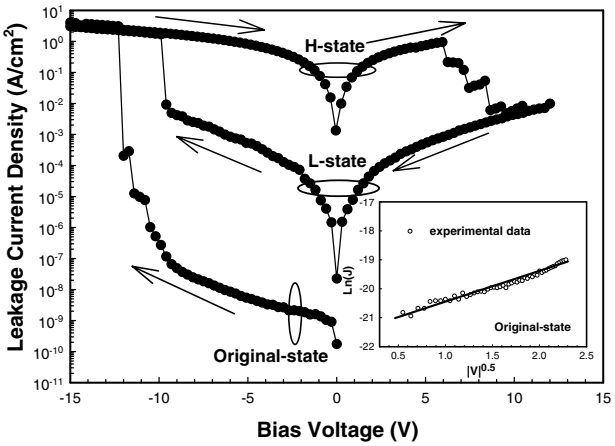

Figure 2. Plot of leakage current density versus bias voltage of Al/SZO/LNO structure. The inset is the comparison between the Schottky emission model and experimental data of the original-state under the negative bias voltages.

3. Results and discussion

Figure 2 shows the plot of leakage current density versus bias voltage for a SZO based MIM device. Before any resistance switching occurred, the leakage current density increases with increasing bias voltage, which is defined as the original-state. While the negative bias voltage is higher than −12 V, the leakage current density increases abruptly to a higher value, which is defined as the H-state. The first resistance switching is called the forming process and needs larger switching voltage. The forming process occurs only in the negative bias voltage direction. Before the forming process, the resistance switching property would be destroyed by applying a large positive voltage on the device. The reason is still unclear, and needs further study. After the forming process, while the positive bias voltage is higher than 10 V, the leakage current density drops abruptly to a low value, which is defined as the L-state. After that, while the negative bias voltage is higher than −10 V, the leakage current density increases abruptly to that of the H-state again. The device resistance is switched between the H-state and the L-state and is never switched back to the original-state with the electrical operation. The leakage-states are not changed without power supply and the resistance ratio between the H-state and the L-state is about 10^4, which is expected to be suitable for nonvolatile memory application. The process switched from the H-state to the L-state is believed to cause the conducting paths to rupture. The conducting paths are randomly ruptured while the positive voltage is applied, which leads to the leakage current decrease. In the transition region from 6 to 10 V, part of the conducting paths are broken and some new conducting paths are formed temporarily; therefore, the current does not decrease to the stable L-state at a time. While the applied voltage is larger than 10 V, all conducting paths are broken and the leakage-state is returned to the stable L-state. Therefore, the uneven switching property occurs in the process changed from the H-state to the L-state [13]. As shown in the inset of figure 2, Ln(J) versus $V^{1/2}$ is plotted. The solid line illustrated in the inset of figure 2 provides a good fit to the experimental data, which corresponds to the Schottky emission mode. Therefore, the Schottky emission is responsible for

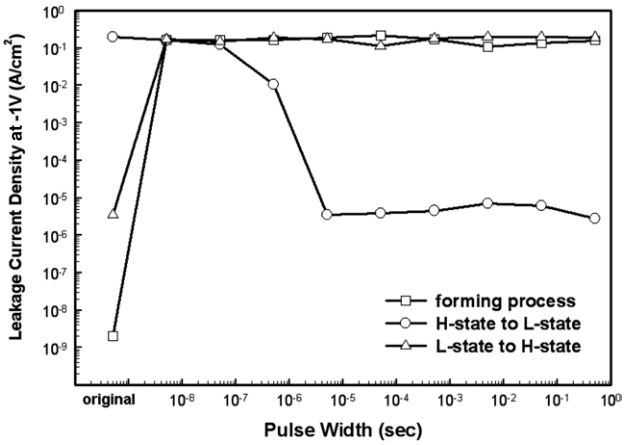

Figure 3. Plot of leakage current density versus pulse width.

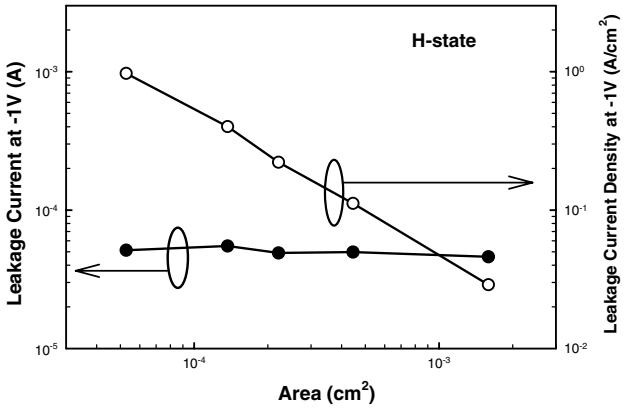

Figure 4. Plot of the leakage current and leakage current density of the H-state versus area of the top electrode.

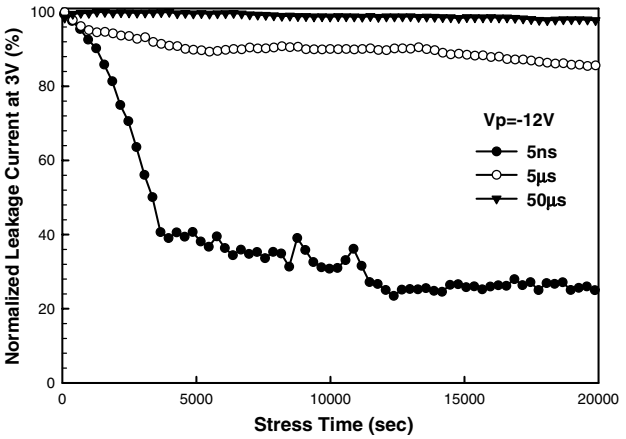

Figure 5. Plot of normalized leakage current versus stress time with various pulse widths.

the leakage current density of the original-state [14]. The conduction mechanisms of the H-state and the L-state were reported to be Ohmic conduction and Frenkel–Poole emission, respectively [15]. Furthermore, the resistance switching can also be operated by voltage pulses. The switching cycling is more than 10^3 times. The mechanism of resistance switching is not clear. However, a suitable processing temperature and dopant are important for obtaining the device with good resistance switching properties [15]. The carbon residual in the sol–gel derived film and dopant in the SZO film could be related to the reproducible resistance switching. The role of carbon in the resistance switching behaviour has been reported in some previous reports [16, 17]. It was indicated that the reproducible resistance switching may be due to the formation of a conducting filament, which possibly consists of point defects such as oxygen vacancies, metallic elements or carbon. After applying a negative bias voltage on the device, the oxygen vacancies, metallic elements or carbon would form conducting filaments as the conducting paths and the leakage-state is changed to the H-state. While giving a positive bias voltage on the device, the conducting paths would be destroyed and the leakage-state is changed to the L-state. Figure 3 depicts the effect of the pulse width with 15 V pulse amplitude on the resistance switching behaviour. While a −15 V, 5 ns voltage pulse is added, the device is changed from the original-state to the H-state, indicating that the forming process is completed within 5 ns. Before measuring the switching times from the H- to the L-state and from the L- to the H-state, the leakage-states were set to the H- and the L-state by negative and positive dc bias voltages, respectively. The H-state is not changed to the L-state until adding a 15 V, 5 μs voltage pulse, indicating that the switching time is between 500 ns and 5 μs. However, before the abrupt resistance switching occurs, the leakage current density of the H-state gradually decreases with increasing pulse width. On the other hand, the L-state is changed to the H-state while a −15 V, 5 ns voltage pulse is added. The switching time from the H-state to the L-state is much longer than that from the L-state to the H-state and that of the forming process. Such a difference of switching times is a disadvantage for memory operation, but it is easily solved by circuit design, such as block erase in flash memory. The top electrodes with various areas were patterned by a metal mask to investigate the size effect of resistance switching property. The leakage current of the L-state and the original-state is proportional to the area of the top electrodes. Hence, there is no size effect. However, as can be seen in figure 4, the leakage current of the H-state does not vary with the increasing area of the top electrode. In other words, the leakage current density of the H-state increases with decreasing area of the top electrode. A similar phenomenon was also observed by other researchers [18, 19]. The amount of conducting paths may not vary with increasing area of the top electrode, causing the leakage current of the H-state to remain almost the same [18]. Although there is no model that can well explain the resistance switching distinctly so far, most related reports [4, 18–20] proposed that the leakage current of the H-state is independent of the area of the top electrode. Figure 5 shows the plot of normalized leakage current versus stress time with various pulse widths. After the leakage-state is switched from the L-state to the H-state by voltage pulse, the decay of the leakage current increases with decreasing pulse width. After switching by a −12 V, 50 μs voltage pulse, the leakage current remains almost the same after stressing 1200 s at 3 V. However, after switching to the H-state by a −12 V, 5 ns voltage pulse, the leakage current is decayed about 80% of the initial value after voltage stressing. The phenomenon should be due to some unstable conducting paths which are built by smaller pulse width. After voltage stressing, the unstable conducting paths would be broken, which leads to

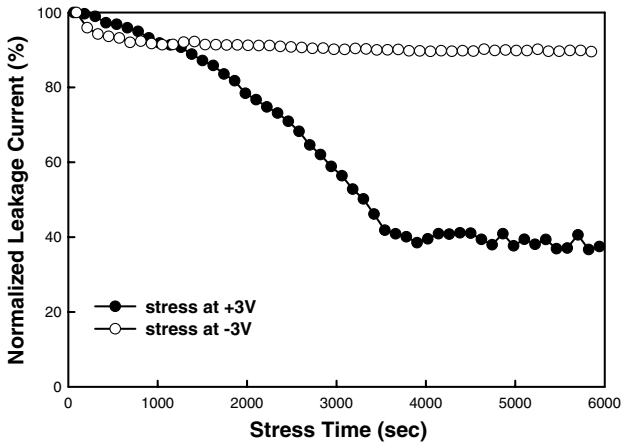

Figure 6. Plot of normalized leakage current versus stress time for different bias voltage directions.

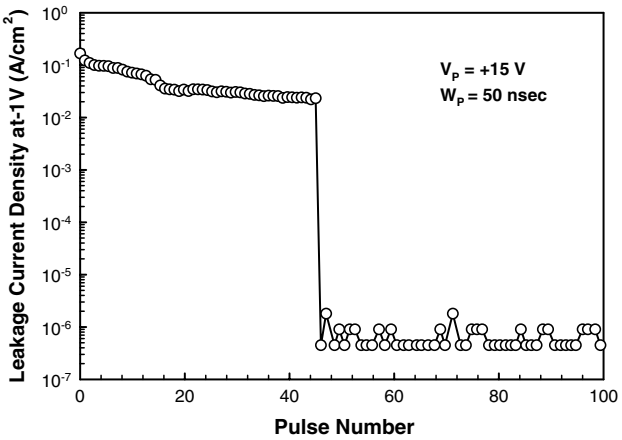

Figure 7. Plot of leakage current density of the H-state versus pulse number after applying 15 V, 50 ns voltage pulses.

the decay of the leakage current. Therefore, the resistance switching by smaller pulse width has larger decay of the leakage current. Figure 6 shows the plot of normalized leakage current versus stress time for different stress voltage directions. After switching to the H-state by a −12 V, 5 ns voltage pulse, the decay under 3 V voltage stress is much larger than that under −3 V voltage stress. In other words, significant decay occurs while the direction of the voltage stress is different from that of the voltage pulse. From figure 2, it is clear that the positive voltage tends to change the leakage-state to the L-state and the negative voltage tends to change the leakage-state to the H-state. Therefore, some unstable conducting paths would be broken under the positive voltage stress and cause the decay of leakage current density while those would not be broken under the negative voltage stress and the leakage current remains almost the same. From the difference of decay behaviour between positive and negative voltage stress, the read voltage should be considered carefully for memory application. Figure 7 depicts the plot of the leakage current density versus the pulse number. The applying pulse width is 50 ns and the amplitude is +15 V. Before applying the voltage pulse on the device, the leakage-state was set to the H-state by a negative dc voltage sweep. One can observe from figure 7 that the single +15 V, 50 ns voltage pulse cannot change the H-state to the L-state. Before the abrupt resistance switching occurs, the leakage current density decreases gradually with increasing applied voltage pulse number, which is similar to the resistance switching from the H-state to the L-state of figure 3. While the applied voltage pulse number is greater than 45, the leakage current density of the device drops abruptly and the leakage-state is changed to the L-state. After the leakage-state is set to the H-state, the conducting paths would be formed and then a part of the paths is expected to be broken by a 15 V, 50 ns voltage pulse. The gradual decrease in the leakage current density shown in figure 7 is believed to be due to such a decrease in the amount of the conducting paths. The leakage-state would be switched to the L-state until all conducting paths are broken by the voltage pulses. The accumulative time of the voltage pulse is 2.25 μs, which is between 500 ns and 5 μs. This is consistent with the result indicated in figure 3. Therefore, the voltage pulse can be accumulated to destroy all the conducting paths. However, no matter how many pulses with lower amplitude (<10 V) are applied, the resistance switching does not occur, indicating that the conducting paths are not broken until a large enough electric field is applied. The effect of accumulative voltage pulses on resistance switching behaviour can be a guide to multi-state memory application.

4. Conclusions

In conclusion, a Al/SZO/LNO MIM structure was fabricated to investigate the behaviours of resistance switching. There are three leakage-states in this device: original-state, L-state and H-state. The leakage-states are not changed without power supply and the resistance ratio between the H-state and the L-state is about 10^4, which is suitable for nonvolatile memory application. Furthermore, the switching time from the H-state to the L-state is much longer than that from the L-state to the H-state and that of the forming process. The leakage current of the H-state does not vary with increasing area of the top electrode, which is similar to the results reported by other researchers. The decay behaviours of the leakage current density after resistance switching are influenced by the pulse width and the stress voltage direction. The voltage pulses can be accumulated to change the H-state to the L-state, which is suitable for designing multi-level memory applications. Although the detailed formation mechanism of conducting paths is not quite clear, the model of conducting paths can well explain the electrical behaviours of our resistance switching devices.

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