A Wide Tuning Range G_m–C Continuous-Time Analog Filter

Tien-Yu Lo, *Student Member, IEEE*, and Chung-Chih Hung, *Member, IEEE*

***Abstract*—A CMOS operational transconductance amplifier (OTA) for low-power and wide tuning range filter application is proposed in this paper. The OTA can work from the weak inversion region to the strong inversion region to maximize the transconductance tuning range. The transconductance can be tuned by changing its bias current. A fifth-order Elliptic low-pass filter implemented with the OTAs was integrated by TSMC 0.18-μm CMOS process. The filter can operate with the cutoff frequency of 250 Hz to 1 MHz. The wide tuning range filter would be suitable for multi-mode applications, especially under the consideration of saving chip areas. The third-order inter-modulation (IM3) of -40 dB was measured over the tuning range with two tone input signals. The power consumption is 0.8 mW at 1-MHz cutoff frequency and 1.8-V supply voltage with the active area less than 0.3 mm^2.**

***Index Terms*—G_m–C filters, low power, operational transconductance amplifier (OTA), strong inversion region, tuning, weak inversion region.**

I. Introduction

THE CURRENT trend of the portable solutions tends to include multiple applications in a long-standby system. Cost and power consumption are two most important factors for these products. Cost efficiency has been greatly increased with the emergence of CMOS technology in high-performance VLSI implementations. Moreover, to save the silicon area in a multimedia system-on-a-chip solution, re-usable circuits for different system applications can be even cost-effective. For the power consumption, digital circuits can benefit from the supply voltage reduction, but analog circuits can not necessarily decrease the power consumption with the decrease of supply voltage. To meet different specifications for low power consumption, new basic analog building blocks should be re-designed.

In the analog signal processing, the low-pass filter would be one of the most important circuits in the transceiver architecture. There are different ways to implement low-pass filters by CMOS technology at the circuit level. The switched-capacitor (SC) technique which uses switches, capacitors, and operational amplifiers exhibits good linearity, but with the problems of larger power consumption. The active-*RC* technique which uses operational amplifiers, resistors, and capacitors also exhibits high linearity, but large chip areas will be consumed for resistors or capacitors. MOS varactors were demonstrated to achieve frequency tuning in the active-*RC* structure [2]. Another technique to realize continuous-time analog filters is to utilize transconductors and capacitors to implement integrators [3]–[7]. The absence of the local feedback in the G_m–C analog filter technique performs good frequency responses of the signal transfer functions [8]. Furthermore, G_m–C analog filters do not require extra processing steps, as compared with active-*RC* filters, and their frequency tuning is easily achieved using dc bias voltage or current. The performance of the transconductor will largely affect the G_m–C analog filters. Many of the previously published papers made efforts on improving the speed, linearity, or dynamic range of transconductor circuits [9]–[12].

This work presents a CMOS implementation of a low-power fifth-order elliptic low-pass G_m–C filter for a very wide frequency tuning range, which can operate as the channel selection filter for the audio, speech, bio-medical, and wireless application. The high-performance voltage-to-current circuit which can operate in both weak inversion and strong inversion regions is designed to achieve a wide transconductance tuning range. The working mode of the transconductor can be set in different inversion regions and the transconductance can be widely tuned by changing dc bias current. The transconductor is used as an operational transconductance amplifier (OTA) in the design of the fifth-order elliptic low-pass G_m–C filter. In the paper, Section II develops the low power and wide tuning range OTA architecture. The equivalent resistor used in the proposed OTA is discussed in Section III. The G_m–C filter is developed in Section IV, followed by the experimental results of both the OTA and the filter in Section V. Conclusions are presented in Section VI.

II. Proposed Transconductor Cell

A. Implementation of Linearization Technique

In order to increase the tuning range of the filter, the range of the transconductance should be increased first. The proposed transconductor circuit based on the translinear loop is shown in Fig. 1. The MOSFETs M1 to M9 should be appropriately designed to operate in both weak and strong inversion regions in order to increase the transconductance range. The linearity has been well maintained while tuning the transconductance.

1) Transconductor Cell Operating in the Weak Inversion Region: For a MOSFET operating in the weak inversion region with $V_{\rm DS}$ larger than a few times of thermal voltage U_T, its current exhibits an exponential dependence of $V_{\rm GS}$, as shown in (1) [1]

$$I_D = I_{D0}\frac{W}{L}\exp\left(\frac{V_{\rm GS}}{nU_T}\right) \tag{1}$$

Manuscript received April 17, 2006; revised August 28, 2006. This work was supported by National Science Council of Taiwan, R.O.C. This paper was recommended by Associate Editor P. Carbone.

The authors are with the Department of Communication Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: cchung@mail.nctu.edu.tw).

Digital Object Identifier 10.1109/TCSI.2007.890614

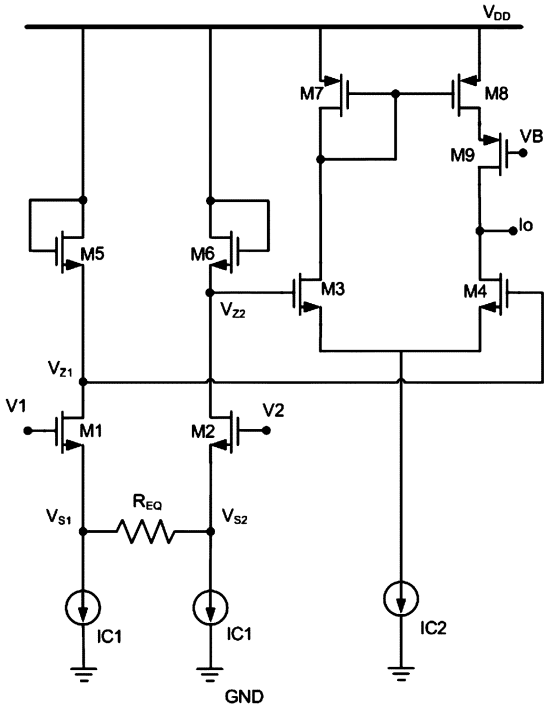

Fig. 1. Proposed transconductor circuit.

where W and L are the width and the length of the transistor, respectively, I_{D0} is the reverse saturation current, n is the subthreshold slope factor, and U_T is the thermal voltage. With the weak inversion characteristic, the input voltage should be logarithmically determined first and through the exponential function, the output current can then be linearized, as shown in transistors M1 to M6 of Fig. 1. When both the input and the output stages of the transconductor operate in the weak inversion mode (weak-in weak-out mode), and the same transistor sizes for M1 to M6 are used, the relationship between differential input voltage and output current can be derived and analyzed. The diode-connected transistors M5 and M6 carry the current I_{D5} and I_{D6}, respectively, and we assume the two gate voltage of transistors M3 and M4 are V_{z2} and V_{z1}. $V_{z1} - V_{z2}$ can be obtained by

$$\begin{aligned} V_{z1} - V_{z2} &= (V_{\rm DD} - V_{gs5}) - (V_{\rm DD} - V_{gs6}) \\ &= V_{gs6} - V_{gs5} \end{aligned} \tag{2}$$

$$V_{z1} - V_{z2} = nU_T \ln\left(\frac{I_{D6}}{I_{D5}}\right). \tag{3}$$

For current I_{D3} and I_{D4}

$$\frac{I_{D4}}{I_{D3}} = \exp\left(\frac{V_{z1} - V_{z2}}{nU_T}\right). \tag{4}$$

From (3) and (4), we can obtain

$$I_o = I_{D3} - I_{D4} = \frac{I_{C2}}{I_{C1}} \frac{(I_{D5} - I_{D6})}{2}. \tag{5}$$

To make sure a linear voltage-to-current conversion is achieved, a resistor $R_{\rm eq}$ connected at the source terminals of transistors M1 and M2 is introduced. The resistor should be chosen much larger than U_T/I_{C1} so that we can have

$$\frac{(I_{D5} - I_{D6})}{2} R_{\rm eq} = V_1 - V_2. \tag{6}$$

By substituting (6) into (5), we can obtain

$$I_o = \frac{I_{C2}}{I_{C1}} \frac{(V_1 - V_2)}{R_{\rm eq}}. \tag{7}$$

The output current can be tuned by two dc bias current I_{C1} and I_{C2} for various transconductance values. In the weak inversion structure, the output current will be small due to the large resistor $R_{\rm eq}$ and thus it will be strongly affected by the output dc voltage. Transistor M9 is added to reduce the channel length modulation effect from the current mirror M7 and M8 because of the different $V_{\rm DS}$ voltage.

In order to take nonlinearity performance into consideration, from a Taylor series analysis, it turns out that the total harmonic distortion (THD) of the proposed circuit is dominated by the third-order harmonic distortion measure ($\rm HD_3$) of this voltage-to-current conversion. The $\rm HD_3$ could be approximated as

$$\begin{aligned} {\rm HD}_3 = \frac{2(I_{C1}R_{\rm eq})^2 nU_T}{(2I_{C1}R_{\rm eq} + nU_T)^4 (2I_{C1}R_{\rm eq} + 2nU_T)} \\ \times (V_1 - V_2)^2. \end{aligned} \tag{8}$$

As the equation shown, the linearity performance can be improved by increasing the tail current I_{C1} and the equivalent resistor $R_{\rm eq}$. However, the increased I_{C1} would lead to higher power consumption, and thus we should choose smaller I_{C1} and larger $R_{\rm eq}$ in order to achieve low-power and high linearity. As long as the resistance of $R_{\rm eq}$ can be kept large enough, in the order of Mega ohm, a linear OTA operation in the weak inversion region can be accomplished. In addition, it is noted that I_{C2} does not affect the linearity performance in the circuit.

2) Transconductor Cell Operating in the Strong Inversion Region: As the transistors M1 to M6 are working in the strong inversion region (strong-in strong-out mode) with the same sizes, the relationship between the output current and the input voltage can be derived as follows:

Again, $V_{z1} - V_{z2} = V_{\rm gs6} - V_{\rm gs5}$. Because the drain current of M1 and M5 are the same and the drain current of M2 and M6 are the same,

$$(V_{\rm gs5} - V_T)^2 = (V_{\rm gs1} - V_T)^2 = (V_1 - V_{s1} - V_T)^2 \tag{9}$$

$$(V_{\rm gs6} - V_T)^2 = (V_{\rm gs2} - V_T)^2 = (V_2 - V_{s2} - V_T)^2 \tag{10}$$

$$V_{gs5} = V_{gs1} = V_1 - V_{s1} \tag{11}$$

$$V_{gs6} = V_{gs2} = V_2 - V_{s2} \tag{12}$$

From (9) to (12), assume $I_{D5} > I_{D6}$ and the current flowing through $R_{\rm eq}$ is $\triangle I$

$$\begin{aligned} V_{z1} - V_{z2} &= (V_2 - V_{s2}) - (V_1 - V_{s1}) \\ &= (V_2 - V_1) - (V_{s2} - V_{s1}) \\ &= (V_2 - V_1) + R_{\rm eq}\Delta I \end{aligned} \tag{13}$$

$$V_1 - V_2 = (V_{z2} - V_{z1}) + R_{\rm eq}\Delta I \tag{14}$$

For the current through transistors M5 and M6, we can have

$$I_{D5} = I_{C1} + \Delta I = \frac{K}{2}(V_{\rm gs1} - V_T)^2 \tag{15}$$

$$I_{D6} = I_{C1} - \Delta I = \frac{K}{2}(V_{\rm gs2} - V_T)^2 \tag{16}$$

where $K = \mu_n C_{\rm ox}(W/L)$, W and L are the width and length of the device, respectively, $C_{\rm ox}$ is the oxide capacitance per unit channel area, and μ_n is the low-field mobility. Therefore

$$V_{\rm gs1} = \sqrt{\frac{2(I_{C1} + \Delta I)}{K}} + V_T \tag{17}$$

$$V_{\rm gs2} = \sqrt{\frac{2(I_{C1} - \Delta I)}{K}} + V_T. \tag{18}$$

From (11), and (12), we can find

$$\begin{aligned} V_{z2} - V_{z1} &= V_{\rm gs1} - V_{\rm gs2} \\ &= \sqrt{\frac{2}{K}}(\sqrt{I_{C1} + \Delta I} - \sqrt{I_{C1} - \Delta I}) \\ &= \sqrt{\frac{2I_{C1}}{K}}\left(\sqrt{1 + \frac{\Delta I}{I_{C1}}} - \sqrt{1 - \frac{\Delta I}{I_{C1}}}\right). \end{aligned} \tag{19}$$

If we assume $\triangle I/I_{C1} \ll 1$, i.e., $\triangle I \ll I_{C1}$

$$\begin{aligned} V_{z2} - V_{z1} &= \sqrt{\frac{2I_{C1}}{K}}\left[\left(1 + \frac{\Delta I}{2I_{C1}}\right) - \left(1 - \frac{\Delta I}{2I_{C1}}\right)\right] \\ &= \sqrt{\frac{2}{KI_{C1}}}\Delta I. \end{aligned} \tag{20}$$

Substituting (20) into (14), we obtain

$$V_1 - V_2 = \sqrt{\frac{2}{KI_{C1}}}\Delta I + R_{\rm eq}\Delta I. \tag{21}$$

Therefore

$$\Delta I = \frac{1}{\sqrt{\frac{2}{KI_{C1}}} + R_{\rm eq}}(V_1 - V_2) \tag{22}$$

$$V_{z1} - V_{z2} = \frac{\sqrt{\frac{2}{KI_{C1}}}}{\sqrt{\frac{2}{KI_{C1}}} + R_{\rm eq}}(V_1 - V_2). \tag{23}$$

The value of the equivalent resistor $R_{\rm eq}$ should be chosen much smaller than the equivalent resistor in the weak inversion structure. If the equivalent resistor $R_{\rm eq}$ were too large, for example, in the order of mega-ohms, $\triangle I$ would be almost zero. The voltage difference between V_{z1} and V_{z2} would be zero as well, so there would be no current flowing to the output. The value of the equivalent resistor $R_{\rm eq}$ should be made comparable to the other term in the denominator of (23), so the difference, $\triangle V_z = (V_{z1} - V_{z2})$, would be large enough to produce output current. From the equations of the differential amplifier, the output current I_o can be obtained by

$$I_o = I_{D3} - I_{D4} = \frac{K}{2}(\Delta V_z)\sqrt{\frac{4I_{C2}}{K} - \Delta V_z^2}. \tag{24}$$

For a small $\triangle V_z^2$ compared to $4I_{C2}/K$

$$I_o \approx \frac{K}{2}(\Delta Vz)\sqrt{\frac{4I_{C2}}{K}} = \frac{\sqrt{\frac{2I_{C2}}{I_{C1}}}}{\sqrt{\frac{2}{KI_{C1}}} + R_{\rm eq}}(V_1 - V_2). \tag{25}$$

The relationship between the output current and the input differential voltage can be tuned by I_{C1} and I_{C2}. With a suitable value of I_{C1}, we can increase I_{C2} to increase the overall transconductance. In addition, in the strong inversion region, the $\rm HD_3$ of the proposed transconducor can also be analyzed by a Taylor series expansion and approximated as

$${\rm HD}_3 = \frac{1}{4\left(R_{\rm eq} + \sqrt{\frac{2}{KI_{C1}}}\right)^2 I_{C1}I_{C2}}(V_1 - V_2)^2. \tag{26}$$

Thus, the low-power and the high-linearity performance call for increasing $R_{\rm eq}$.

3) Transconductor Cell Operating in the Multi-Inversion Regions: In order to increase the tuning range of the transconductance, the transconductor is designed to be able to switch from the weak inversion region to the strong inversion region continuously. This means that the largest transconductance in the weak inversion region should be larger than the smallest transconductance in the strong inversion region. (The detailed analyses of bias current conditions will be shown in Section III). Thus, the transconductor circuit would operate in the regions where the input stage, including transistors M1, M2, M5, and M6, remains in the same inversion condition, weak or strong, while the output stage, including transistors M3, M4, M7, M8, and M9, is forced to move from weak to strong inversion region or vice versa.

If we need to increase the transconductance when the transconductor works in the weak inversion region, we should increase the value of I_{C2} to move from weak-in weak-out to weak-in strong-out operation. At a certain point, the increased value of I_{C2} will enable M3, M4, M7, M8, and M9 to enter the strong inversion region. The relationship between output current and the input differential voltage can be approximated to

$$I_o = \frac{\sqrt{KI_{C2}}}{I_{C_1}} nU_T \frac{2}{R_{\rm eq}}(V_1 - V_2). \tag{27}$$

On the other hand, if we need to decrease the transconductance when the transconductor works in the strong inversion region, we should decrease the value of I_{C2}. At certain point, the decreased value of I_{C2} will have M3, M4, M7, M8, and M9 to enter the weak inversion region. The relationship between the output current and the input differential voltage can now be approximated to

$$I_o = \frac{I_{C2}}{nU_T}\frac{\sqrt{\frac{2}{KI_{C1}}}}{2\left(\sqrt{\frac{2}{KI_{C1}}} + R_{\rm eq}\right)}(V_1 - V_2). \tag{28}$$

However, the nonlinear term in the voltage-to-current relationship will increase in the transition of multi-mode inversion. If we need to achieve a large tuning range and an acceptable

linearity, the input voltage swing should be kept limited when operation in multi-mode inversion.

B. Noise Analysis of the Proposed Transconductor

Flicker noise is the dominant input-referred noise source for low frequencies. Using the Flicker noise model of transistors reported in [1], the low frequency noise referred to the input terminals of transconductors can be calculated and its equivalent noise power spectral density (PSD) is given by

$$\frac{V_{f-in}^2}{\Delta f} = 2v_{M1}^2 + v_{R_{\mathrm{eq},f}}^2 + 2v_{\mathrm{tail}}^2 g_{m\mathrm{tail}}^2 R_{\mathrm{eq}}^2 + 2\left[v_{M5}^2 + v_{M3}^2 + v_{M7}^2\left(\frac{g_{m7}}{g_{m3}}\right)^2\right] \times \left[\frac{(1+g_{m1}R_{\mathrm{eq}})g_{m5}}{g_{m1}}\right]^2 \quad (29)$$

where g_{mi} is the small signal transconductance of transistor M_i, $g_{m\mathrm{tail}}$ is the transconductance of the MOS current sources, $V_{R\mathrm{eq},f}^2$ is the Flicker noise contributed by the equivalent resistor, V_{tail}^2 is the Flicker noise contributed by the tail current source I_{C1}, and $V_{Mi}^2 = K_F I_D/W_i L_i f$, K_F being the Flicker noise coefficient, f being frequency, W_i and L_i being the width and length of transistor M_i, is the Flicker noise contributed by transistor M_i. Thus, low frequency noise can be minimized by proper design of transistor dimensions and bias current source.

As frequency higher than noise corner frequency, estimated around 300 Hz, the noise source is dominated by the thermal noise. By the thermal noise model given in [13], the input-referred thermal noise can be expressed by

$$\frac{V_{\mathrm{th-in}}^2}{\Delta f} = 8kT\gamma_a\left(\frac{1}{g_{m1}} + g_{m,\mathrm{tail}}R_{\mathrm{eq}}^2 + g_{m5}\left[\frac{(1+g_{m1}R_{\mathrm{eq}})}{g_{m1}}\right]^2\right) + 8kT\gamma_b\left(\frac{1}{g_{m3}} + \frac{g_{m7}}{g_{m3}^2}\right)\left[\frac{(1+g_{m1}R_{\mathrm{eq}})g_{m5}}{g_{m1}}\right]^2 + I_{R_{\mathrm{eq}},\mathrm{th}}^2 R_{\mathrm{eq}}^2 \quad (30)$$

where k is the Boltzmann constant, T is the temperature, γi is the noise parameter depending on the device bias condition, and $I_{R\mathrm{eq},\mathrm{th}}^2$ is the thermal noise contributed by the equivalent resistor. According to [13], the noise parameter γ would be equal to $1/2$ and $2/3$ at weak and strong inversion regions, respectively. From the equation shown above, a high value of R_{eq}, which improves the linearity, would also induce increased noise. Thus, large aspect ratios of input transistors and small aspect ratios of load and tail current transistors should be chosen for smaller thermal noise PSD.

III. Equivalent Resistor R_{eq}

A. Switching Methodology

According to the above analysis of different requirement of the equivalent resistor, we would use two different scales of resistors for linearity consideration. Fig. 2 shows the equivalent circuit of resistor R_{eq}. The resistor can be modeled by the parallel connection of a large resistor and a small resistor. For the constraint of limited chip areas, to implement the large resistor, the equivalent resistor circuit is implemented by CMOS, instead of poly resistors, and we use the output impedance r_o of saturated transistors in our design to emulate the large resistance. The nodes V_{S1} and V_{S2} are connected to the source terminals of M1 and M2 in Fig. 1. When M1, M2, M5, and M6 operate in the weak inversion region, V_{mode} is set low to turn off MRS and the equivalent resistance is the output impedance of four parallel connected MOSFETs in the saturation region so as to provide the high resistance. In Fig. 2, the transistors MR1 to MR8 working in the saturation region will be used as the equivalent resistor when the transconductor operates in the weak inversion region. V_{S1} and V_{S2} are set to half of the supply voltage to achieve largest swing ranges. Under the dc voltage constraint, to maintain the correct operation region of the equivalent saturated resistor circuit, MS1 to MS4 in Fig. 3 are introduced as the level shifter circuit. Thus, the output common mode voltage of the saturated resistor would be approximately equal to the input common mode voltage of the transconductor cell for the largest swing range operation. On the other hand, when M1, M2, M5, and M6 work in the strong inversion region and V_{mode} is set high, a low-value resistor is obtained by the transistor MRS working in the triode region.

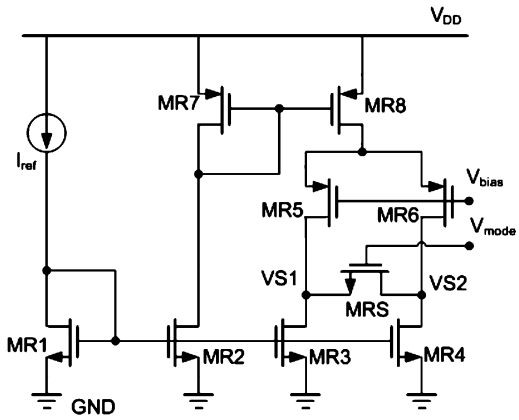

Fig. 2. Equivalent resistor circuit.

B. Bias Current Condition

In order to make sure that the transconductor can continuously operate over the entire range, we should properly design the values of the linear and the saturated resistors.

For the saturated resistors, the conductance can be approximated by [14]

$$\frac{1}{R_{\mathrm{eq,large}}} = g_o = \frac{I_{\mathrm{ref}}X_D\sqrt{K_a}}{4L\sqrt{V_X}} + \sigma\sqrt{K_R I_{\mathrm{ref}}} \quad (31)$$

where σ is inversely proportional to the cube of the transistor length, K_a is the kappa voltage, X_D is a device fitting parameter, and K_R is the device parameter of MR5 and MR6. The voltage V_X is given by

$$V_X = V_{\mathrm{DS}} - V_{\mathrm{DSAT}} + \frac{1}{K_a}\left(\frac{E_a X_D}{2}\right)^2 \quad (32)$$

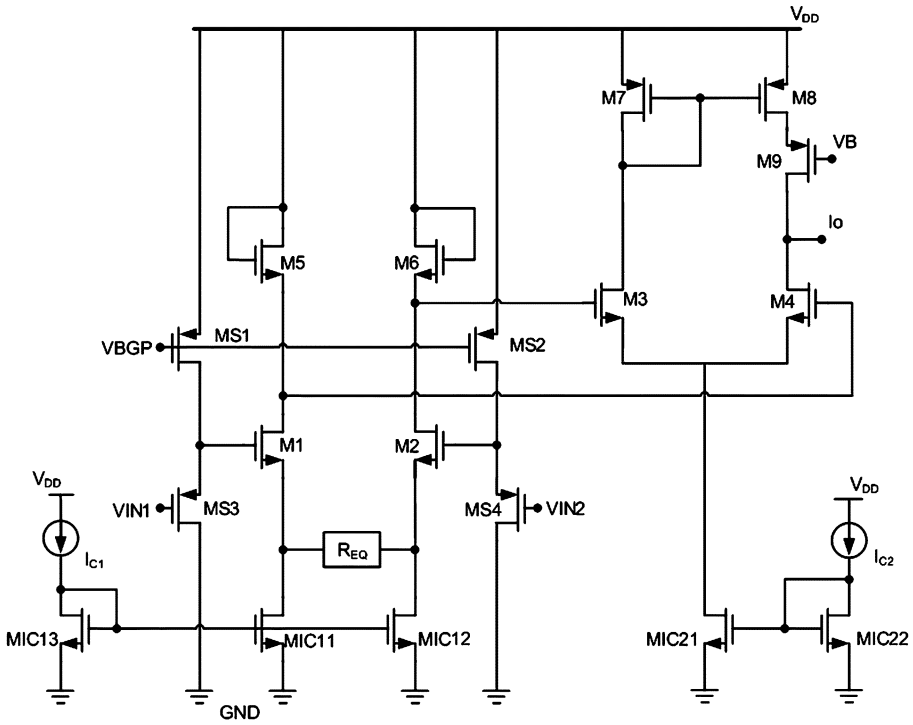

Fig. 3. Final implementation of the proposed transconductor circuit.

where $V_{\rm DS}$ is the drain–source bias voltage and E_a is the Early voltage. From the equation shown above, the resistance can be tuned by the bias current $I_{\rm ref}$. Moreover, in the sub-micron processes with small device length, the second term in (31) dominates the saturated conductance.

The conductance mismatch between bias transistors MR5 and MR6 only slightly affects the saturated resistor performance. The mismatch problem can be solved by choosing larger feature sizes of transistors and careful layout. For parasitic capacitance, analyses indicate that the effect caused by mismatch of gate–drain and drain–source capacitors between MR5 and MR6 can be reduced by a larger capacitor connected to the $V_{\rm bias}$ node. And for stability analyses, the gate–drain and drain–bulk capacitors will only induce a high-frequency pole for the structure. It has been shown by simulation that the pole appears at the gigahertz range, and thus the saturated resistor is suitable for our frequency range design.

As the MOS transistor is biased in the linear region, the conductance can be expressed as

$$\frac{1}{R_{\rm eq,small}} = K_r(V_{\rm mode} - V_T - V_{\rm cms}) \tag{33}$$

where V_T is the threshold voltage, $K_{\rm r}$ is the device parameter of MRS, and $V_{\rm cms} = ({\rm VS1} + {\rm VS2})/2$.

As it was mentioned in the previous section, in order to increase the tuning range of the transconductance, the largest transconductance in the weak inversion region should be larger than the smallest transconductance in the strong inversion region. That means that the output current in (27) should be larger than the current of (28). We can substitute the conductance obtained in (31) and (33) into (27) and (28) respectively, and we can find the following limitation:

$$\frac{\beta}{\alpha} < \frac{\sqrt{2K}(nU_T)^2}{\sigma\sqrt{K_R I_{\rm ref}}} \tag{34}$$

where

$$\alpha = \frac{I_{C2\_\rm strong}}{I^2_{C1\_\rm weak}} \tag{35}$$

$$\beta = \frac{\sqrt{2} + \frac{1}{K_r(V_{\rm mode}-V_T-V_{\rm cms})\sqrt{KI_{C2\_\rm weak}}}}{I_{C1\_\rm strong}} \tag{36}$$

α is defined when the input stage stays in the weak inversion region and the output stage enters the strong inversion region, as shown in (35), and β is also defined when the input stage stays in the strong inversion region and the output stage enters the weak inversion region, as shown in (36).

In addition, the working mode of the circuit can be selected by the gate voltage of MIC13 in Fig. 4. If the gate voltage of MIC13 is larger than the threshold voltage, $V_T, V_{\rm mode}$ will be set by series of inverters to supply voltage. Otherwise, if the gate voltage of MIC13 is smaller than $V_T, V_{\rm mode}$ will be set to ground voltage. It is known that the larger transconductance can induce higher cutoff frequency in analog low-pass filter design. In our scircuit, the transconductance in both inversion regions will be changed by I_{C1} and I_{C2}.

C. Linearity and Noise Analyses

Based on the non-ideal effect of the active device compared with the passive device, the linearity performance of active resistors should be taken into consideration. For the saturated resistor

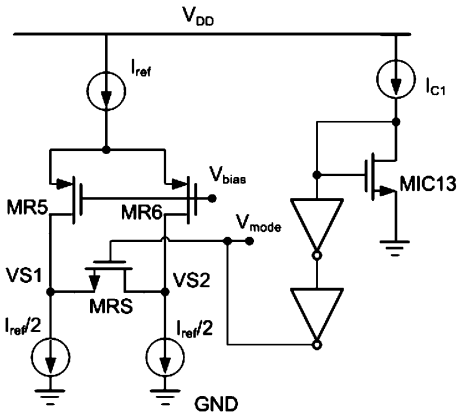

Fig. 4. $V_{\rm mode}$ switching circuit for the proposed transconductor.

structure, the even-order distortions are cancelled by the differential structure. Thus, third-order harmonic distortion dominates the linearity performance and can be further computed as [14]

$$\mathrm{HD}_{3\_R_{\mathrm{eq,large}}} = \frac{1}{16}\left(\frac{g_{\mathrm{oL}}}{g_{\mathrm{oL}}+\sigma\sqrt{K_R I_{\mathrm{ref}}}}\right)\left(\frac{V_{S1}-V_{S2}}{V_X}\right)^2 \tag{37}$$

where g_{oL} is the conductance expressed in the first term of (31). Therefore, the linearity performance can be improved by using larger feature size of the transistors MR5 and MR6.

On the other hand, the even-order distortion of the linear region MOS transistor based resistor would be canceled out. The third-order distortion can be demonstrated by taking body effects into consideration

$$\mathrm{HD}_{3\_R_{\mathrm{eq,small}}} = \frac{1}{(V_{\mathrm{mode}}-V_T-V_{\mathrm{cms}})(2\varphi_F-V_B+V_{\mathrm{cms}})^{\frac{3}{2}}} \times \frac{\gamma_b}{384}(V_{S1}-V_{S2})^2 \tag{38}$$

where γ_{b} is the body factor, ϕ_F is the Fermi level, and V_{B} is the bulk voltage. From (38), higher gate voltage or lower bulk voltage of the MOS resistor would result in better linearity. Fig. 5 shows the harmonic distortion for the linear region and the saturated MOS resistors. The dimensions of transistors MR5 and MR6 are $8\ \mu$m/$4\ \mu$m. For MRS, the dimension is $1\ \mu$m/$1\ \mu$m. A 2% mismatch for MR5 and MR6 has been included in the simulation. The distortion level below $-$ 40 dB of both resistors can be achieved for a 10-MHz $0.8\mathrm{V_{pp}}$ input signal. Besides, the short channel effect, due to the electrical and lateral electric fields, also limits the linearity performance. The noise produced by the equivalent resistor circuit will directly affect the noise performance from the analysis of (29) and (30). For the saturated resistor, the noise is contributed by the addition of transistors MR3, MR4, MR5, and MR6. Transistor MRS induces the linear region MOS resistor noise. Thus, the flicker and thermal noise PSD produced by both the large and small resistors can be given by

$$v^2_{R_{\mathrm{eq},f}} = \left(2g^2_{mR3}v^2_{MR3}+2v^2_{MR5}g^2_{mR5}\right)R^2_{\mathrm{eq}} \tag{39}$$

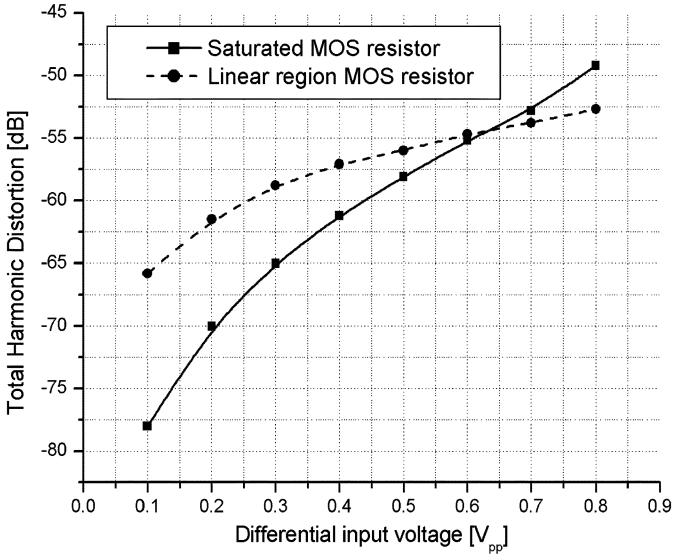

Fig. 5. Simulated linearity performance of the equivalent resistor.

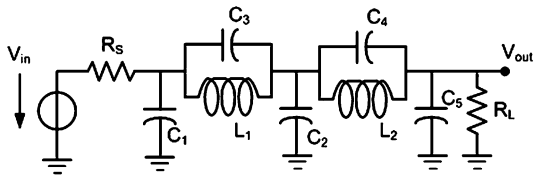

Fig. 6. Fifth-order elliptic *RLC* ladder network prototype.

$$I^2_{R_{\mathrm{eq,th}}} = 4kT[2\gamma_c(g_{mR3}+g_{mR5})+\gamma_d g_{\mathrm{mRS}}]. \tag{40}$$

Thus, the optimized values versus the noise and linearity performance would be chosen and adopted carefully from their performance tradeoff.

IV. Filter Architecture

To demonstrate the basic building block in a system level, a fifth-order Elliptic low-pass filter is implemented [15]. The fifth-order Elliptic low-pass filter design starts from a standard fifth-order Elliptic low-pass *LC*-ladder prototype, as shown in Fig. 6. A $-$6-dB dc gain can be easily obtained under very low frequency when resistor R_S equals to resistor R_L. From the *RLC*-ladder prototype, through the use of the signal-flow graph method [16], the fifth-order Elliptic low-pass G_m–C filter, which consists of seven identical OTAs and seven capacitors, including two floating capacitors, is obtained. The transconductance, which equals to the value of $1/R_S$ and $1/R_L$, is used for all OTAs. Q tuning circuits are not considered here with the intrinsic quality of the low Q structure. The final G_m–C filter implementation is shown in Fig. 7. The OTA introduced in the previous section is used here in the design of the fifth-order Elliptic low-pass G_m–C filter.

In low-pass filter design, the cutoff frequency of the filter is proportional to g_m/C, where g_m is the transconductance of the OTA and C is the capacitance. Low cutoff frequency filters are very important in the speech signal processing and medical hearing application. However, there are some problems encountered in these low frequency filter design. The main issues are

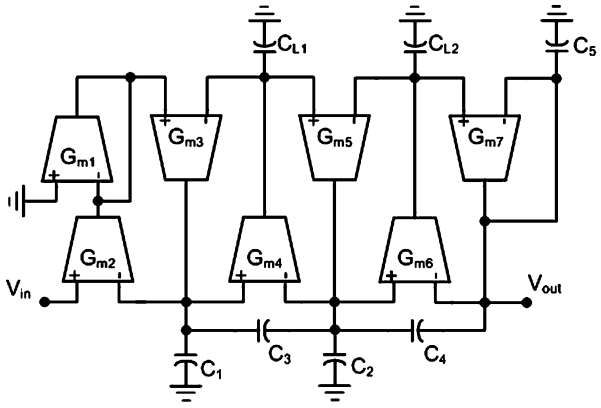

Fig. 7. Fifth-order elliptic low-pass G_m–C filter.

the large time constant involved and the values of the resistors and capacitance limited by the silicon area. In our circuit, when the transconductor works in the weak inversion region, a small value of capacitance will be enough to achieve the low cutoff frequency owing to the small transconductance in the nS order. On the other hand, the larger transconductance can also be obtained in the same filter architecture for higher cutoff frequency when the OTA works in the saturation region.

The cutoff frequency of the G_m–C filter is tuned by changing the dc bias current of the OTA. Because the transconductance range of the OTA is quite wide, the resultant filter also has a wide cutoff frequency range under suitable working mode selection. Tuning circuitry can be developed with digitally controlled circuits in a system-on-a-chip solution by choosing a number of current sources for G_m tuning. The maximum capacitance shown in Fig. 7 is only 3.6 pF, so it is easy to integrate with the other circuits.

V. Experimental Results

The OTA and the filter were fabricated in the TSMC 0.18-μm Deep N-WELL CMOS process. Body effects can be simply eliminated by connecting the source and the bulk terminals together in the process. The aspect ratio of 11.5 μm/2 μm is used for transistors M1, M2, M3, M4, M5, and M6, and 11.5 μm/0.2 μm is used for transistors M7, M8, and M9. The value of 8 μm/4 μm is used for MR5 and MR6, and $I_{\rm ref}$ is equal to 20 μA in the equivalent resistor circuit. 1 μm/1 μm is used for linear region MOS resistor MRS. Since the mismatches in transconductors and capacitors directly translate to the degradation of overall performance, such as nonlinear effects and errors of transformation, the filter has been laid out very carefully. Metal–insulator–metal capacitors were used in the circuit and the unit of the capacitor array is 0.1 pF. In this section, the experimental results are presented. All of the results were obtained with a single power supply of 1.8 V.

The measurement results of the OTA's transfer curves are shown in Fig. 8(a)–(d). In Fig. 8(a), the measurements of voltage-to-current transfer curves are obtained when both the input and output stages of the OTA operate in the weak inversion region as I_{C1} equals to 10 nA and I_{C2} changes from 10 to 80 nA. The saturated resistor circuit is selected here by setting $V_{\rm mode}$ to GND. The transfer curves in the weak inversion region follow the expected formula described previously. Also, the transconductance is changed from 2.5 to 16 nS, as shown in the figure. In Fig. 8(b), owing to the increment of I_{C2}, the output stage of the OTA extends the operation from the weak inversion region to the strong inversion region while the input stage and the equivalent resistor remain in the same previous condition, and thus achieves to a much larger transconductance. The measured transconductance could be tuned from 3 to 610 nS by increasing I_{C2} to the value of 10 μA.

In Fig. 8(c), the input and output stages of the OTA both operate in the strong inversion region to achieve a large transconductance, as compared with the weak inversion region operation. The linear region MOS resistor circuit is selected here by setting $V_{\rm mode}$ to VDD. The transconductance from 11 to 18 μS is obtained while the current I_{C1} equals to 1 μA and I_{C2} changes from 10 to 40 μA. We can find that the transconductance would be tuned proportional to the square root of I_{C2} as described in the formula above. In Fig. 8(d), the decreased I_{C2} results that the output stage of the OTA extends the operation from the strong inversion region to the weak inversion region while the input stage and the equivalent resistor remain in the same condition, and thus achieves to a much smaller transconductance. As shown in the figure, the transconductance could be tuned from 20.2 to 0.19 μS by decreasing I_{C2} to the value of 0.5 μA.

From the measurement results of Fig. 8(b) and (d), continuous tuning from weak inversion operation to strong inversion operation can be guaranteed and the OTA can be tuned for a very wide range. However, the linearity of the OTA should be maintained over the range because it will directly affect the linearity of the proposed G_m–C filter. For the linearity of this OTA, when both the input and output stages of the OTA operate in the weak inversion region, THD is about $-$ 56 dB with $I_{C1} = 10$ nA $I_{C2} = 10$ nA at 100 Hz 300 $\rm mV_{pp}$ input signal. As I_{C2} increases to 10 μA, the output stage will operate in the strong inversion region while the input stage stays in the weak inversion region, and THD is measured to be -44 dB. On the other hand, when the input and output stages of the OTA operate in the strong inversion region, THD of -43 dB is measured by giving $I_{C1} = 1$ μA and $I_{C2} = 40$ μA with 10-kHz 300-$\rm mV_{pp}$ input signal. Input signals with higher frequency are applied here owing to the fact that the large transconductance would be used for the filter with higher cutoff frequency. As I_{C2} decreases to 0.5 μA, the output stage of the OTA operates in the weak inversion region while the input stage stays in the same region, and THD of -42 dB is measured.

Fig. 9 illustrates the filter measurement results over the tuning range for different bias currents I_{C1} and I_{C2}. The cutoff frequency can be tuned from 250 Hz to 1 MHz, a tuning ratio of 4000. The third-order inter-modulation (IM3) distortion, which implies the linearity performance of the proposed filter, is measured at cutoff frequency. By using two sinusoidal tones with the amplitude of 300 $\rm mV_{pp}$, -53 dB is measured when the filter operates at low cutoff frequency of 250 Hz. On the other hand, when the cutoff frequency of the filter is tuned to 1 MHz, the IM3 is measured -41 dB. Fig. 10 shows the relationship of measured IM3 versus cutoff frequency for the proposed

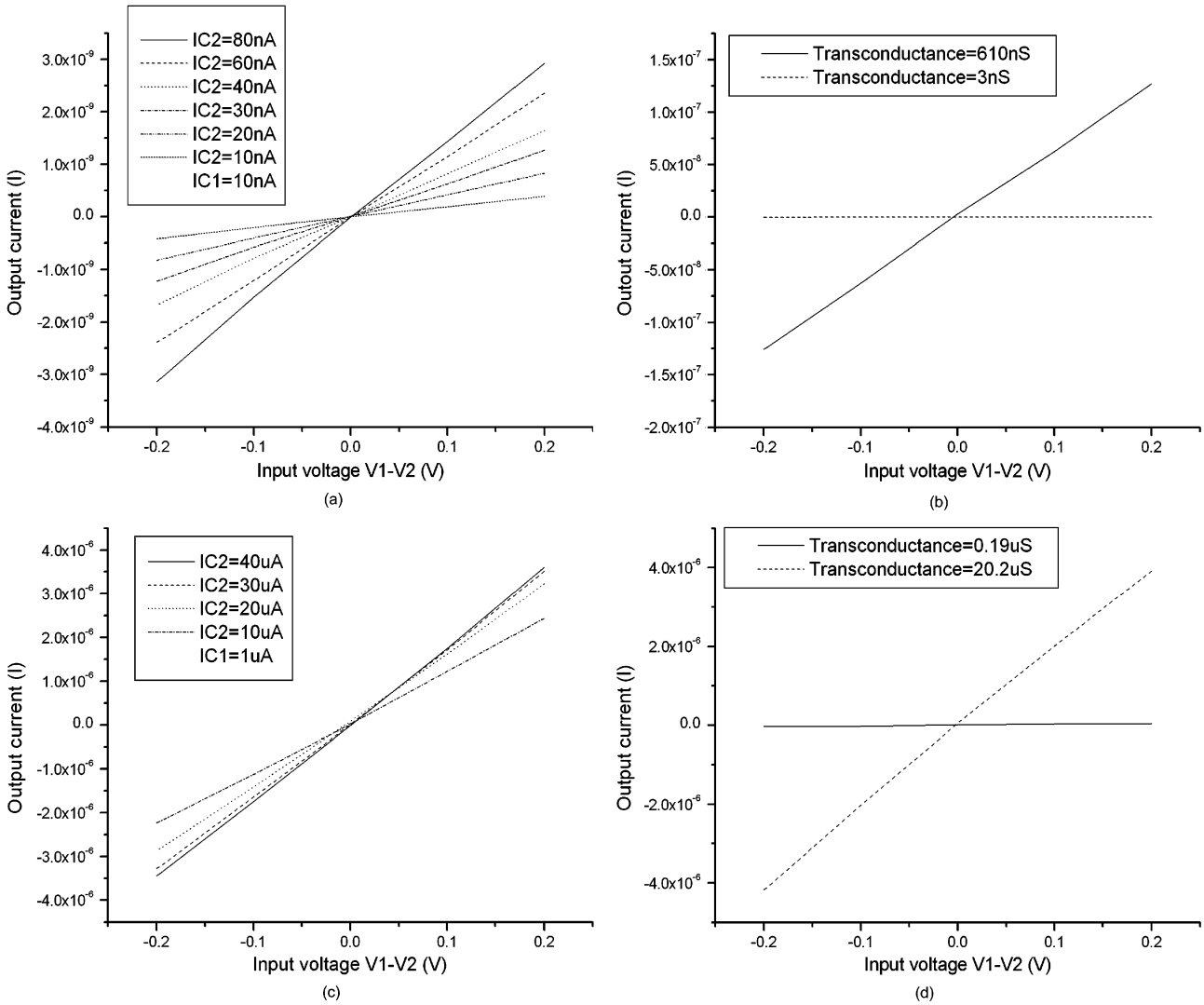

Fig. 8. Measurement results of the proposed transconductor circuit. (a) OTA in the weak inversion region. (b) OTA in the multi-inversion regions: the input stage stays in the weak inversion region while the output stage operates from the weak inversion region to the strong inversion region. (c) OTA in the strong inversion region. (d) OTA in the multi-inversion regions: the input stage stays in the strong inversion region while the output stage operates from the strong inversion region to the weak inversion region.

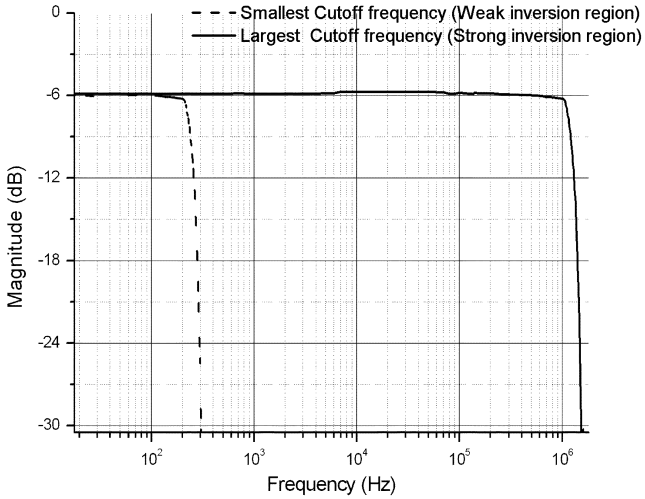

Fig. 9. Measured frequency responses over the tuning range.

wide tuning range filter. The worst case which happens in the middle band of the wide tunable filter is due to the multi-inversion operation.

When the cutoff frequency of the filter is 250 Hz, a dynamic range of 52 dB is measured with the 300-$\mathrm{mV_{pp}}$ input signal as V_{mode} is set to ground voltage. On the other hand, at the cutoff frequency of 1 MHz, a 48-dB dynamic range is measured as V_{mode} is set to VDD voltage. The measured PSRR at 100 Hz is 36 dB. The filter dissipates 0.2 and 0.8 mW for lowest and highest cutoff frequency setting, respectively, at 1.8-V supply voltage.

A die photo is shown in Fig. 11. The total active area is less than 0.3 $\mathrm{mm^2}$. In order to compare with different implementations of G_m–C low pass filters, the figure of merit (FOM) defined in [17], which takes the inter-modulation free dynamic range, speed of the implemented filter, tuning ratio, and normalized power consumption into account, is expressed as follows:

$$\mathrm{FoM} = 10\log\left(\frac{\mathrm{IMFDR_{linear}} \times f_o \times \mathrm{tuning}}{\mathrm{power}_N}\right) \tag{41}$$

where IMFDR is defined as the signal to noise ratio when the power of the third-order inter-modulation distortion term equals

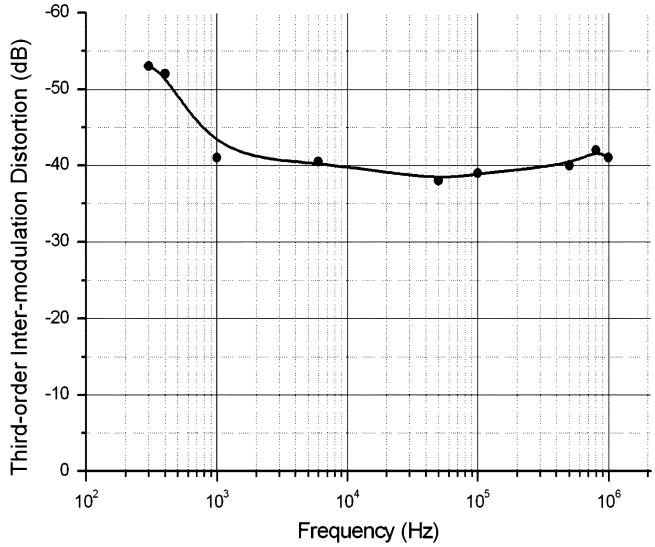

Fig. 10. Measured IM3 values at cutoff frequency.

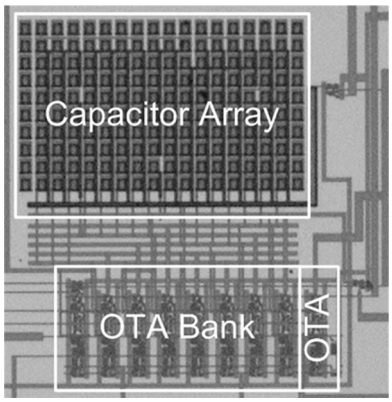

Fig. 11. Die microphotograph.

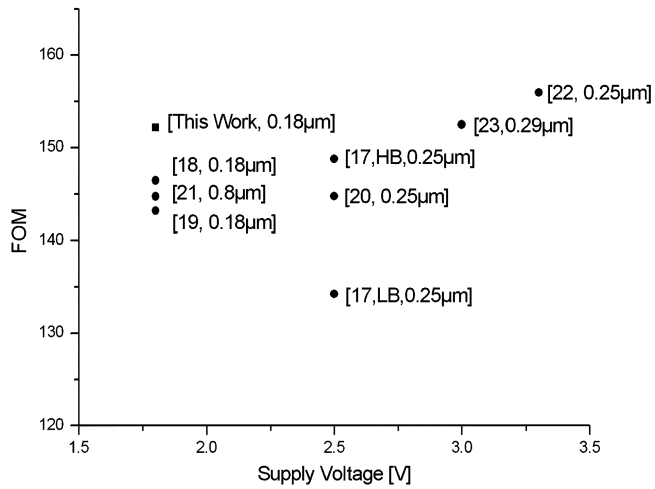

Fig. 12. FOM comparison with previously published filters.

to the noise power, f_o is the geometrical mean of the cutoff frequency in the unit of Hz, tuning is the tuning ratio of the low pass filter, and power_N is the geometrical mean of power per pole quantity in the unit of watt. The FOM of the filter is plotted versus power supply voltage and compared with the other previously published works. As shown in Fig. 12, our wide tuning range low pass filter compares favorably with the literature. Table I summarizes the experimental results of the proposed filter.

TABLE I
PERFORMANCE SUMMARY OF THE FABRICATED PROTOTYPE

Technology	TSMC 0.18-µm CMOS
Supply Voltage	1.8V
Filter type	Fifth-order Elliptic low-pass
Tuning range	250Hz-1MHz
IM3 for 300mV$_{pp}$ input signals over the tuning range	-40dB
Dynamic range	48 dB
Power consumption	0.8mW
Active area	0.3mm^2

VI. CONCLUSION

A CMOS implementation of a fifth-order Elliptic low-pass G_m–C filter with wide tuning range is presented. A complete set of experimental results are provided to demonstrate the validity of the proposed filter. The OTA used in the filter works in the weak inversion region to achieve micro-power consumption and works in the strong inversion region to extend its tuning range. The working mode of the OTA could be set and the transconductance could be continuously tuned by setting I_{C1} and I_{C2}. With the use of the OTA as a building block in the filter architecture, the cutoff frequency of the low pass filter is changed from 250 Hz to 1 MHz, which covers the range of some audio, speech, bio-medical, and wireless application, so it could be used in multi-mode applications of signal processing. Moreover, the silicon area is saved with less power consumption in the entire filter design. The minimum power supply needed is in the range of $2V_{\rm GS} + V_{\rm DSsat}$ which can be around 1.2 V or less depending on bias current levels. Measurement results demonstrate the potential of the technique to provide a system-on-a-chip design solution for low power dissipation and very wide tuning range applications.

ACKNOWLEDGMENT

The authors would like to thank the National Chip Implementation Center of Taiwan, R.O.C. for supporting the chip fabrication.

REFERENCES

[1] B. Razavi, *Design of Analog CMOS Integrated Circuit*. New York: McGraw-Hill, 2001.
[2] S. Chatterjee, Y. Tsividis, and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2373–2387, Dec. 2005.
[3] J. Silva-Martínez, J. Adut, J. M. Rocha-Perez, M. Robinson, and S. Rokhsaz, "A 60-mW 200-MHz continuous-time seventh-order linear phase filter with on-chip automatic tuning system," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 216–225, Feb. 2003.
[4] I. Mehr and D. R. Welland, "A CMOS continuous-time G_m–C filter for PRML read channel applications at 150 Mb/s and beyond," *IEEE J. Solid-State Circuits*, vol. 32, no. 4, pp. 499–531, Apr. 1997.

[5] F. Rezzi, A. Baschirotto, and R. Castello, "A 3 V 12–55-MHz BiCMOS pseudodifferential continuous-time filter," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 42, no. 11, pp. 896–903, Nov. 1995.
[6] H. Voorman and H. Veenstra, "Tunable high-frequency G_m–C filters," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1097–1108, Aug. 2000.
[7] A. N. Mohieldin, E. Sánchez-Sinencio, and J. Silva-Martínez, "A fully balanced pseudodifferential OTA with common-mode feedforward and inherent common-mode feedback detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 499–531, Apr. 2003.
[8] K. C. Kuo and A. Leuciuc, "A linear MOS transconductor using source degeneration and adaptive biasing," *IEEE Trans. Circuits Syst. II*, vol. 48, no. 10, pp. 937–943, Oct. 2001.
[9] C. C. Hung, M. Ismail, K. Halonen, and V. Porra, "A low-voltage rail-to-rail CMOS V-I converter," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 6, pp. 816–820, Jun. 1999.
[10] U. Chilakapati, T. S. Fiez, and A. Eshraghi, "A CMOS transconductor with 80-dB SFDR up to 10 MHz," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 365–370, Mar. 2002.
[11] S. R. Zarabadi, M. Ismail, and C.-C. Hung, "High performance analog VLSI computational circuits," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 644–649, Apr. 1998.
[12] A. J. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, and R. G. Carvajal, "Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 1068–1077, Mar. 2005.
[13] U. Yodprasit and C. C. Enz, "A 1.5-V 75-dB dyamic range third-order Gm-C filter integrated in a 0.18-μm standard digital CMOS process," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1189–1197, Jul. 2003.
[14] M. Steyaert, J. Silva-Martinez, and W. Sansen, "High-frequency saturated CMOS floating resistor for fully differential analogue signal processors," *Electron. Lett.*, pp. 1609–1611, Aug. 1991.
[15] L. P. Huelsman, *Active and Passive Analog Filter Design*. New York: McGraw-Hill, 1993.
[16] C. C. Hung, K. A. Halonen, M. Ismail, V. Porra, and A. Hyogo, "A low-voltage, low-power CMOS fifth-order ellipticG_m–C filter for baseband mobile, wireless communication," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 7, pp. 584–593, Aug. 1997.
[17] D. Chamla, A. Kaiser, A. Cathelin, and D. Belot, "A G_m–C low-pass filter for zero-IF mobile applications with a very wide tuning range," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1143–1450, Jul. 2005.
[18] S. Hori, T. Maeda, N. Matsuno, and H. Hida, "Low-power widely tunable Gm-C filter with an adaptive dc-blocking, triode-biased MOSFET transconductor," in *Proc. ESSCIRC*, 2004, pp. 99–102.
[19] S. Hori, T. Maeda, H. Yano, N. Matsuno, K. Numata, N. Yoshida, Y. Takahashi, T. Yamase, R. Walkington, and H. Hida, "A widely tunable CMOS Gm-C filter with a negative source degeneration resistor transconductor," in *Proc. ESSCIRC*, 2003, pp. 449–452.
[20] G. Bollati, S. Marchese, M. Demicheli, and R. Castello, "An eighth-order CMOS low-pass filter with 30–120-MHz tuning range and programmable boost," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1056–1066, Jul. 2001.
[21] J. A. De Lima and C. Dualibe, "A linearly tunable low voltage CMOS transconductor with improved common-mode stability and its application to gm-C filters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 7, pp. 649–660, Jul. 2001.
[22] S. Pavan, Y. P. Tsividis, and K. Nagaraj, "Widely programmable high-frequency continuous-time filters in digital CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 503–511, Apr. 2000.
[23] N. Rao, V. Balan, and R. Contreras, "A 3-V 10–100-MHz continuous-time seventh-order 0.05 equiripple linear phase filter," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1676–1682, Nov. 1999.

Tien-Yu Lo (S'06) was born in I-Lan, Taiwan, R.O.C., in 1979. He received the B.S. degree and the M.S. degree, both in communication engineering from National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 2001 and 2003, respectively. Since 2003, he has been working toward the Ph.D. degree at the same university.

His research interests include low voltage and low power analog integrated circuits.

Chung-Chih Hung (M'98) was born in Tainan, Taiwan, R.O.C. He received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 1989, and the M.S. and Ph.D. degrees in electrical engineering from The Ohio State University, Columbus, OH, in 1993 and 1997, respectively.

From 1989 to 1991, he served in the Taiwan Marine Corps as a Communication Officer. From 1997 to 2003, he worked for several IC design companies in San Jose, CA, and San Diego, CA, where he held analog circuit design manager and director positions. Since 2003, he has been an Assistant Professor of Communication Engineering at National Chiao Tung University, Hsinchu, Taiwan, R.O.C. His current research interests include the design of analog and mixed-signal integrated circuits for communication and high-speed applications.