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Investigation of analogue performance for process-induced-strained PMOSFETs

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Abstract
This paper investigates the analogue performance of process-induced-strained PMOSFETs for system-on-a chip applications. Through a comparison between co-processed strained and unstrained PMOSFETs regarding important analogue metrics such as transconductance to drain current ratio (g_m/I_d), output resistance, dc gain and the gain-bandwidth product, the impact of process-induced uniaxial strain on the analogue performance of MOS devices has been assessed and analysed. Our study may provide insights for analogue design using advanced strained devices.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

As conventional CMOS is reaching its scaling limits, mobility scaling has emerged as a key technology for improving device performance [1]. To enable the mobility scaling, process-induced-strained silicon has been widely used in state-of-the-art CMOS technologies [2–7].

Although the carrier mobility enhancement can help overcome the speed/power barrier for logic applications and enhance the cut-off frequency [8], the impact of strain on analogue performance is not well known [9]. This issue is especially important to mixed-mode integrated circuits for system-on-a-chip (SOC) [10, 11] and merits investigation.

Important metrics for analogue applications include transconductance to drain current ratio (g_m/I_d) [12], output resistance (R_{out}), dc gain ($g_m \times R_{out}$) and the gain-bandwidth product. Through a comparison between co-processed strained and unstrained PMOSFETs [4] with a sub-100 nm gate length, this work examines the analogue performance in uniaxial strained PMOSFETs.

2. Devices and intrinsic I_d extraction

The devices used in this study were fabricated by state-of-the-art process-induced uniaxial strained-Si technology [13]. The transistor gate length, L_{gate}, ranges from 1 μm to 50 nm. Since the source/drain series resistance (R_s/R_d) is crucial to device performance, an accurate determination of the source/drain series resistance has been carried out. The R_s/R_d values are 252 Ω μm and 118 Ω μm for the control and strained devices, respectively [13]. Once the source/drain series resistance is determined, the intrinsic drain current in the linear region ($I_{d,lin}$) and saturation region ($I_{d,sat}$) can be extracted by equations (1) and (2), respectively:

$$I_{d,lin}(\text{int}) = \frac{I_{d,lin}(\text{ext})}{1 - I_{d,lin}(\text{ext})(R_s + R_d)/V_d} \quad (1)$$

$$I_{d,sat}(\text{int}) = \frac{I_{d,sat}(\text{ext})}{1 - I_{d,sat}(\text{ext})R_s/V_{gst}}. \quad (2)$$

Note that in equations (1) and (2), V_d and V_{gst} ($=V_g - V_{th}$) denote drain bias and gate voltage overdrive, respectively.

3. Results and discussion

Figure 1 shows the intrinsic $I_{d,lin}$ and $I_{d,sat}$ enhancement of the strained devices. It can be seen that the intrinsic $I_{d,lin}$ and $I_{d,sat}$ are improved by about 100% and 50%, respectively. The PMOS drain currents are improved because the hole mobility is increased by the strain-induced valence band warping [3–5, 14]. The enhancement in $I_{d,sat}$ is less than $I_{d,lin}$ because of velocity saturation. It indicates that the enhancement in saturation velocity (v_{sat}) for strained devices is smaller than the mobility (μ_{eff}) improvement. Since the critical electric field at which the carrier velocity becomes saturated, $E_{sat} = 2v_{sat}/\mu_{eff}$ [15], we can expect a smaller E_{sat} in strained devices. In other words, the saturation drain voltage (V_{dsat}) for the strained device should be smaller than its control counterpart for a given gate voltage overdrive. From the output resistance (R_{out}) versus the V_d plot (figure 2), $V_{d,sat}$ can be extracted by linear

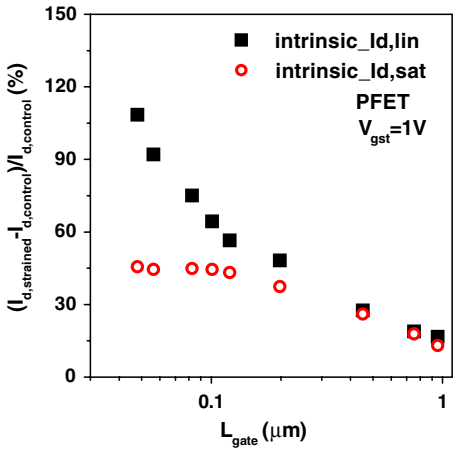

Figure 1. Intrinsic $I_{d,lin}$ and $I_{d,sat}$ enhancements for strained PMOS devices.

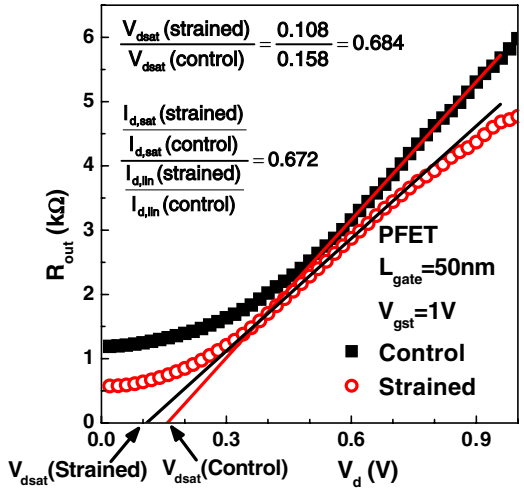

Figure 2. Output resistance versus V_d. The extracted V_{dsat} ratio corresponds to the E_{sat} ratio in the short channel device.

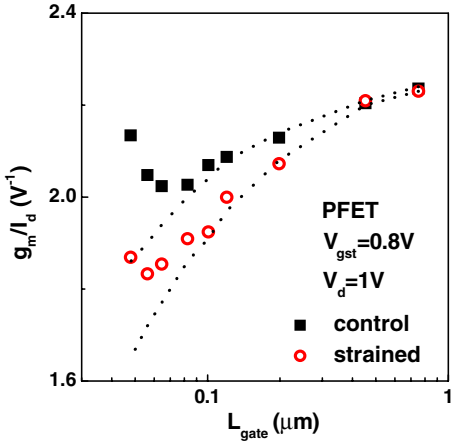

Figure 3. g_m/I_d versus L_{gate} at $V_{gst} = 0.8$ V.

extrapolation because R_{out} is proportional to $V_d - V_{d,sat}$ in the channel-length modulation region [15, 16]. It can be seen from figure 2 that the strained PFET indeed has a smaller $V_{d,sat}$ (∼0.11 V).

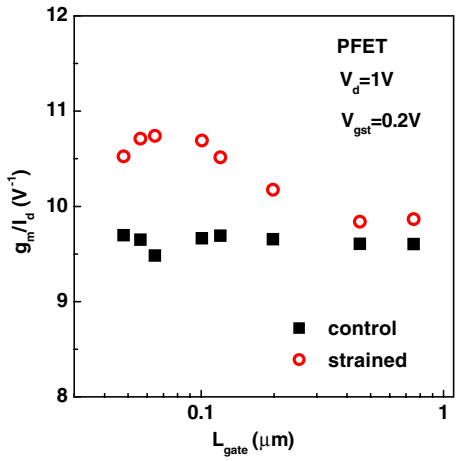

Figure 4. g_m/I_d versus L_{gate} at $V_{gst} = 0.2$ V.

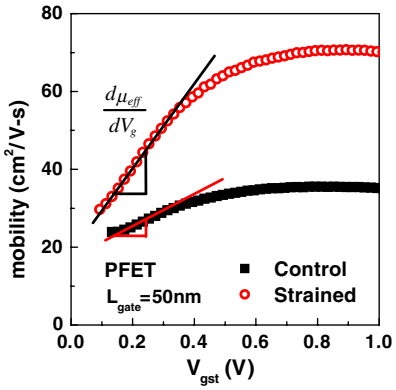

Figure 5. The extracted carrier mobility versus V_{gst} for devices with $L_{gate} = 50$ nm.

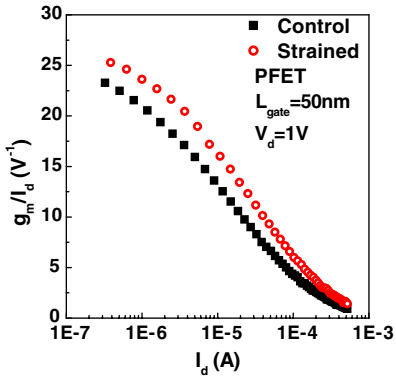

Figure 6. g_m/I_d versus I_d at $V_d = 1$ V for devices with $L_{gate} = 50$ nm.

The impact of E_{sat} on g_m/I_d, the transconductance efficiency of the device, is mainly in the high V_g regime. Figure 3 shows g_m/I_d versus L_{gate} at $V_{gst} = 0.8$ V. The roll-off of g_m/I_d as gate length decreases can be modelled by the following equation derived from BSIM [15]:

$$\frac{g_m}{I_d} = \frac{1}{V_{gst}}\left(\frac{V_{gst} + 2E_{sat}L_{eff}}{V_{gst} + E_{sat}L_{eff}}\right) + \left(\frac{E_{sat}L_{eff}}{E_{sat}L_{eff} + V_{gst}}\right)\frac{(\partial\mu_{eff}/\partial V_g)}{\mu_{eff}}, \quad (3)$$

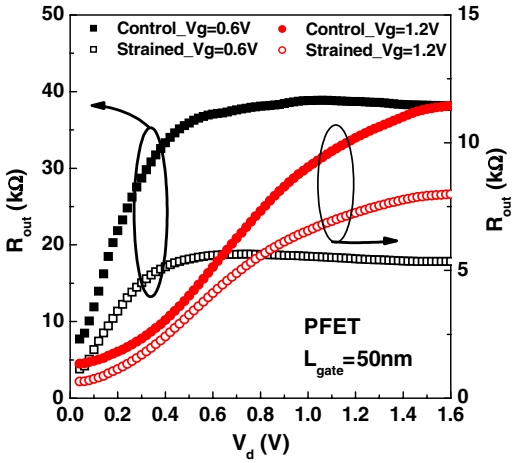

Figure 7. $R_{\rm out}$ versus $V_{\rm d}$ for devices with $L_{\rm gate} = 50$ nm.

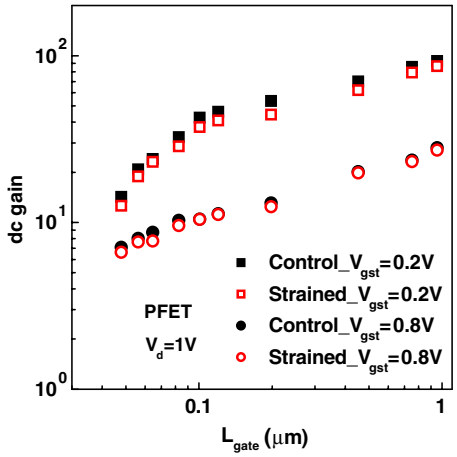

Figure 8. DC gain versus $L_{\rm gate}$ for $V_{\rm gst} = 0.2$ V and 0.8 V.

where the effective channel length $L_{\rm eff} = L_{\rm gate} - 2\Delta L$. ΔL is the gate-extension overlap distance and is calculated from the measurement of overlap capacitance. Note that the $g_{\rm m}/I_{\rm d}$ ratio shown in figure 3 is indeed bounded by $2/V_{\rm gst}$ and $1/V_{\rm gst}$ when the effective channel length decreases from the long channel limit ($L_{\rm eff} \to \infty$) to the short channel limit ($L_{\rm eff} \to 0$), as predicted by the first term in equation (3). The lower $g_{\rm m}/I_{\rm d}$ for strained devices can be attributed to the smaller $E_{\rm sat}$.

Figure 4 shows $g_{\rm m}/I_{\rm d}$ versus $L_{\rm gate}$ in the low $V_{\rm g}$ regime ($V_{\rm gst} = 0.2$ V). It can be seen that $g_{\rm m}/I_{\rm d}$ for the strained device rolls up as gate length decreases. Moreover, $g_{\rm m}/I_{\rm d}$ for the strained device is higher than its control counterpart, which can be attributed to the gate bias sensitivity of the mobility (i.e. the second term in equation (3)).

Figure 5 shows the extracted mobility [13] versus $V_{\rm gst}$. It can be seen that $\mu_{\rm eff}$ increases with $V_{\rm g}$ around $V_{\rm gst} = 0.2$ V. This is because in the low $V_{\rm g}$ regime, the mobility is mainly determined by Coulombic scattering. The mobile carrier screening makes $\mu_{\rm eff}$ increase with $V_{\rm g}$. The larger slope of the mobility for the strained device, which is consistent with the data in [17–19], may be attributed to the reduced effective mass [21] and is responsible for the higher $g_{\rm m}/I_{\rm d}$ observed in figure 4. Figure 6 shows $g_{\rm m}/I_{\rm d}$ versus drain current for strained and unstrained devices with $L_{\rm gate} =$ 50 nm. For analogue devices normally biased by constant drain currents, figure 6 indicates that the strained device has a superior transconductance efficiency [12] than its control counterpart.

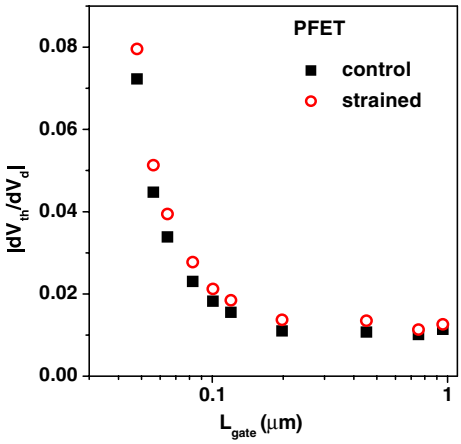

Figure 9. $|{\rm d}V_{\rm th}/{\rm d}V_{\rm d}|$ versus $L_{\rm gate}$.

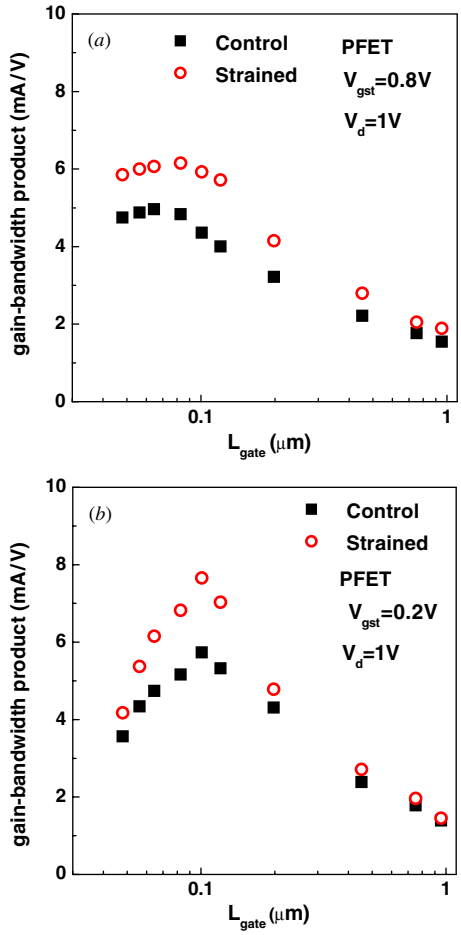

Figure 10. The gain-bandwidth product versus $L_{\rm gate}$ for (*a*) $V_{\rm gst} = 0.8$ V and (*b*) $V_{\rm gst} = 0.2$ V.

Figure 7 shows output resistance ($R_{\rm out}$) versus $V_{\rm d}$ for various $V_{\rm g}$. It can be seen that $R_{\rm out}$ for strained devices is significantly reduced. $R_{\rm out}$ in the high $V_{\rm d}$ regime (i.e. maximum

R_{out}) is mainly determined by drain-induced barrier lowering (DIBL) and can be modelled by [15, 16]

$$R_{out(DIBL)} = \frac{1}{-g_m \times (\partial V_{th}/\partial V_d)}. \quad (4)$$

The reduction in R_{out} for the strained device is mainly due to the enhanced g_m. Figure 8 compares the dc gain ($g_m \times R_{out}$) of the strained device with the control device at $V_d = 1$ V. It can be seen that the dc gain for the strained device (especially in the low V_g regime) is slightly less than its control counterpart. It indicates that, according to equation (4), the strained device has a higher V_d sensitivity of the threshold voltage, as verified by figure 9.

Figure 10 shows the comparison of the gain-bandwidth product in the high V_g regime and low V_g regime, respectively. The gain-bandwidth product is considered as the gain $\times g_m$ product because the bandwidth, $f_T = g_m/2\pi C_L$, is proportional to g_m for a given capacitive load at the transistor output [20]. Due to the enhancement in carrier mobility and g_m [4], the gain-bandwidth product is significantly improved for the strained device. It is worth noting that in figure 10(*b*), there is a significant lowering of gain-bandwidth product for $L_{gate} < 0.1$ μm. This can be attributed to the degraded carrier mobility caused by pocket implants, which is one main reason that strained silicon is needed for boosting the performance of state-of-the-art CMOS technologies.

4. Conclusions

We have investigated the impact of process-induced uniaxial strain on the analogue performance of MOS devices. In the high V_g regime, g_m/I_d for strained devices is reduced due to decreased E_{sat}. In the low V_g regime, nevertheless, g_m/I_d for the strained device is higher than its control counterpart because of the higher V_g sensitivity of the mobility present in the strained device. For analogue devices biased by constant drain currents, the strained device shows superior transconductance efficiency. Although the output resistance for strained devices is substantially reduced due to the g_m enhancement, the impact of strain on dc gain is not significant. Finally, substantially improved gain-bandwidth product has been observed for strained devices. This study may provide insights for analogue design using advanced strained devices.

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