Dependence of Device Structures on Latchup Immunity in a High-Voltage 40-V CMOS Process With Drain-Extended MOSFETs

Sheng-Fu Hsu, *Member, IEEE*, and Ming-Dou Ker, *Senior Member, IEEE*

***Abstract*—The dependence of device structures on latchup immunity in a 0.25-μm high-voltage (HV) 40-V CMOS process with drain-extended MOS (DEMOS) transistors has been verified with silicon test chips and investigated with device simulation. Layout parameters such as anode-to-cathode spacing and guard ring width are also investigated to find their impacts on latchup immunity. It was demonstrated that the drain-extended NMOS with a specific isolated device structure can greatly enhance the latchup immunity. The proposed test structures and simulation methodologies can be applied to extract safe and compact design rule for latchup prevention of DEMOS transistors in HV CMOS process.**

***Index Terms*—Drain-extended MOS (DEMOS), high-voltage (HV) CMOS process, latchup, silicon-controlled rectifier (SCR), transmission line pulsing (TLP).**

I. Introduction

HIGH-VOLTAGE (HV) drain-extended MOS (DEMOS) transistors are increasingly important in modern integrated circuit (IC) design because DEMOS can provide a cost-effective solution to integrate both low-voltage (LV) and HV devices into a single silicon chip [1]–[7]. DEMOS transistors have been widely used in HV ICs or power ICs such as driver circuits, telecommunication, power management switches, motor control systems, automotive electronics, medical applications, etc. Compared with the vertical HV MOSFET structures such as diffused MOSFET (DMOS) [3], [4] or vertical MOSFET (VMOS) [3], [4], which cannot be integrated with LV devices, DEMOS transistors have the primary advantage of easily being implemented in a standard LV CMOS process. In addition, DEMOS transistors can provide advantages such as high driving current and high junction breakdown voltage. As a result, DEMOS transistors can offer IC (system) designers a better design flexibility as well as cost-effective solution, hence leading DEMOS transistors to become a significant topic in system-on-chip design.

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When DEMOS transistors are used for products that require high reliability demand such as liquid crystal display (LCD) driver, automotive electronics, and medical applications, the detailed understanding of their reliability issues is necessary. In addition to the earlier researches of DEMOS transistors under hot-carrier [5], [6] and electrostatic discharge (ESD) [7] stresses, latchup characteristic in DEMOS transistors is also very critical and should be investigated. When DEMOS transistors are used in HV IC design, one tough challenge on their reliability issues is to eliminate the possible occurrence of latchup [8]–[12]. However, due to an ultrahigh circuit operating voltage in HV CMOS ICs, it is rather difficult to achieve the latchup-free purpose by raising the latchup holding voltage to exceed a high circuit operating voltage. In addition, latchup in HV CMOS ICs usually consumes much power in comparison with that in LV CMOS ICs [3]. Once latchup occurs, HV CMOS ICs are always inevitable to be damaged by latchup-generated high power. Thus, how to improve the latchup immunity in HV ICs is indeed a crucial reliability issue. Particular cares, such as DEMOS device structures and their layout styles, must be taken for latchup prevention. However, compared with the standard LV CMOS technology where many detailed process [13]–[16], layout [17], [18], and circuit [19] solutions have been proposed for latchup prevention, so far, there are no related researches to investigate the dependence of DEMOS device structures and their layout styles on latchup immunity in HV CMOS technology.

In this paper, HV latchup characteristics under JEDEC latchup current test are investigated. Two different latchup sensors, namely 1) HV silicon-controlled rectifier (SCR) and 2) LV SCR, are used to simulate the internal circuits for different voltage applications (2.5 V for LV SCR and 40 V for HV SCR) in real HV CMOS circuitry. In addition, the dependence of DEMOS device structures on latchup immunity is also investigated under three different HV latchup test structures [20]. These three latchup test structures can simulate each possible case of the parasitic SCR with different DEMOS device structures, including isolated, nonisolated, symmetric, and asymmetric device structures. In addition, layout parameters such as anode-to-cathode spacing and guard ring width are also investigated to find their impacts on latchup immunity. In order to avoid the HV latchup test structures being damaged so easily under the long-period (microseconds to milliseconds) latchup overstress of the continuous-type curve tracer, the transmission line pulsing (TLP) [21] generator with pulsewidth of 100 ns and limited energy is used instead in this paper for latchup

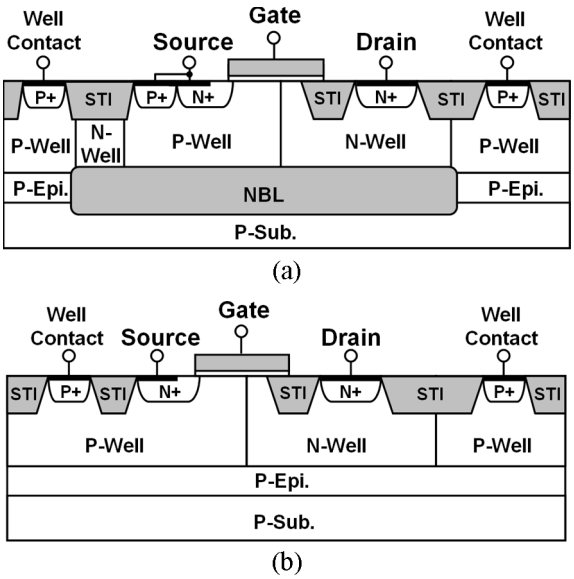

Fig. 1. Device cross-sectional views. (a) Isolated n-DEMOS. (b) Nonisolated n-DEMOS.

current–voltage $(I$–$V)$ measurements. All the TLP-measured latchup I–V characteristics on different HV latchup test structures can be qualitatively and quantitatively verified by the 2-D device simulation. All the silicon test chips are fabricated in a 0.25-μm 40-V CMOS technology.

II. Device Structures of DEMOS Transistors

The devices studied in this paper are implemented in a standard 0.25-μm 2.5-V/5-V CMOS technology. Both HV and LV MOSFETs are built on a high-resistance P-epitaxial (P-epi.) layer above the P-substrate. The device structures of DEMOS transistors can be classified into two major parts, namely 1) isolated or nonisolated device structures and 2) symmetric or asymmetric device structures.

A. Isolated and Nonisolated Device Structures

The device cross-sectional views of the isolated and nonisolated drain-extended NMOS (n-DEMOS) are depicted in Fig. 1(a) and (b), respectively. An N-well region enclosing the N^+ drain with some overlap of polygate is used as the drain drift region. This drain drift region (N-well) can sustain high voltage (+40 V) on drain terminal by increasing the drain junction breakdown voltage. In addition, it can lower the high electric field in channel region to suppress the short-channel effect [2]. The shallow trench isolation (STI) between the gate oxide and N^+ drain is used to lower the electric field in gate oxide far below the critical value of oxide breakdown $(10^6$ V $\cdot$ cm$)$. Thus, the gate-oxide breakdown near the drain side can be efficiently eliminated.

The term "isolated" means that there is an additional N^+ buried layer (NBL) beneath the N-well (P-well) region in the device active region. Thus, the NBL can combine its peripheral N-well regions to form the drain isolation region. The purpose of the drain isolation region is used to help isolate the device channel, source, and its body (P-well) region from the latchup-induced noise current outside the active region, as shown in Fig. 1(a). In contrast with the isolated n-DEMOS, there is no NBL in the nonisolated n-DEMOS. Instead, the whole device is fabricated on a thin P-epi. layer above the P-substrate, as shown in Fig. 1(b).

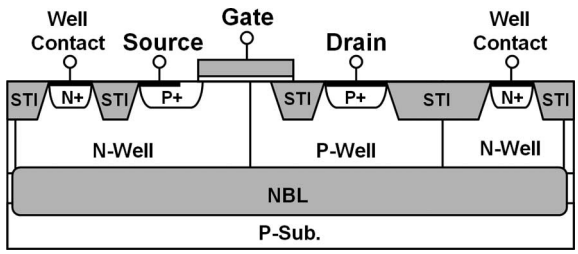

Fig. 2. Device cross-sectional view of the isolated p-DEMOS.

The device cross-sectional view of the isolated drain-extended PMOS (p-DEMOS) is depicted in Fig. 2. The isolation region consists of the NBL and its aforementioned peripheral N-well regions. If there is no isolation region in p-DEMOS, leakage current path (short-circuit path) can exist when p-DEMOS is turned on, as shown in Fig. 3(a). Holes can flow from the P^+ source (+40 V) of p-DEMOS, through the turn-on channel and P-epi. layer, and finally flow into the adjacent P^+ pickups (0 V). Thus, the isolated device structure is necessary for p-DEMOS to avoid such leakage path, as shown in Fig. 3(b). Similar to n-DEMOS, a P-well region enclosing the P^+ drain is used as the drain drift region to sustain high voltage on drain terminal. The STI between the gate oxide and P^+ drain is used to eliminate the gate-oxide breakdown near the drain side.

B. Symmetric and Asymmetric Device Structures

The device cross-sectional views of the nonisolated asymmetric and nonisolated symmetric n-DEMOS are depicted in Figs. 1(b) and 4, respectively. The term "symmetric" means that both drain and source N^+ diffusions are enclosed with the N-well regions, which are used as the drain and source drift regions to sustain high operating voltage, as shown in Fig. 4. For asymmetric n-DEMOS, however, such N-well region to sustain high voltage is only implemented on the drain side, as shown in Fig. 1(b). With a better design flexibility for IC designers, symmetric device has the advantage of HV sustainability on both drain and source sides. However, it must suffer larger turn-on resistance and larger layout area than the asymmetric device.

III. HV Latchup Characteristics

For very large scale integration design in HV CMOS process, foundries usually support latchup design rules or guidelines for latchup prevention. For example, the minimum spacing between NMOS and PMOS (maximum spacing from the substrate or well pickups to the device active region) is usually well defined to prevent the occurrence of latchup for I/O (internal) circuits. However, foundries usually do not support the explicit

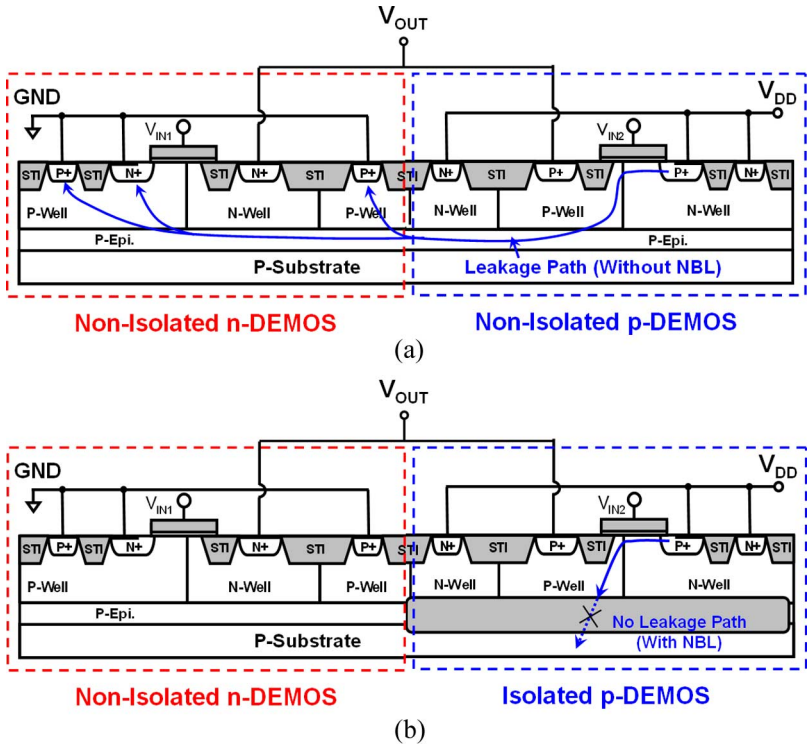

Fig. 3. (a) p-DEMOS without the NBL. (b) p-DEMOS with the NBL. p-DEMOS with isolated device structure is necessary to avoid short-circuit leakage path.

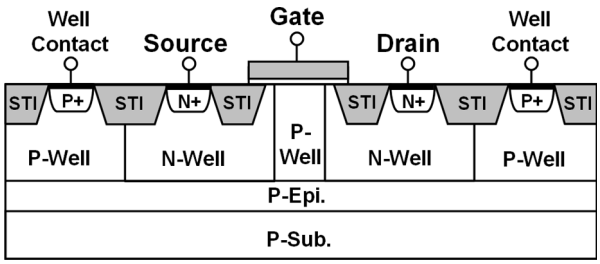

Fig. 4. Device cross-sectional view of the nonisolated symmetric n-DEMOS.

design guidelines to prevent latchup on internal circuits due to the noise current injection from I/O pins. In such latchup issue, one dominant layout rule is the minimum spacing between the I/O and internal circuits. If the spacing is not long enough, the noise current injecting into the I/O pins can easily trigger on latchup in its adjacent internal circuits. However, a too large spacing may lead to a larger chip area and fail to achieve the cost-down purpose, especially in high-pin-count ICs.

The JEDEC latchup current test [22] is widely adopted in IC industry to evaluate this latchup issue. In this test, a current pulse is injected into the I/O pins to see if latchup occurs in device under test (DUT). For LV CMOS circuits, most failure returns [18] reveal that latchup occurs in internal circuits rather than in I/O circuits, because the design rules for latchup prevention are often well defined in I/O circuits but not in between I/O and internal circuits. In addition, since the internal circuits are always highly integrated and hard to become latchup free (holding voltage larger than the normal circuit operating voltage), internal circuits are rather sensitive to latchup in comparison with I/O circuits. For HV CMOS circuits, however, few researches have been done on such latchup issue. Thus, it is significant to investigate the HV latchup characteristics under latchup current test.

In this paper, the relations between the latchup immunity of internal circuits (i.e., minimum trigger current injected from I/O pins to initiate latchup in internal circuits) and the layout spacing from I/O cells to internal circuits are investigated in HV CMOS process. Two different latchup sensors, namely 1) HV SCR and 2) LV SCR, are used to simulate the internal circuits for different voltage applications (2.5 V/40 V) in real HV CMOS circuitry, e.g., LCD driver circuits. All the test chips are fabricated in a 0.25-μm 2.5-V/40-V CMOS technology.

A. Test Structure

In HV CMOS ICs, latchup can be triggered on due to the inherent existence of the parasitic SCR between n-DEMOS and p-DEMOS. The device cross-sectional view of the inverter logic circuit, which consists of a nonisolated asymmetric n-DEMOS and an isolated asymmetric p-DEMOS, is shown in Fig. 5. The parasitic SCR composed of two cross-coupled bipolar junction transistors (BJTs) is also depicted in Fig. 5. Such an inverter circuit is the basic logic component in CMOS ICs. It is well known that the parasitic SCR within it, however, is the origin of latchup [13]. Once latchup is triggered on by large enough substrate or well current, a positive feedback mechanism will lead to a large current conducting through a low-impedance path from $V_{\rm DD}$ (source of p-DEMOS) to ground (GND; source of n-DEMOS). As a result, HV CMOS ICs will malfunction or even be burned out due to the latchup-generated high power.

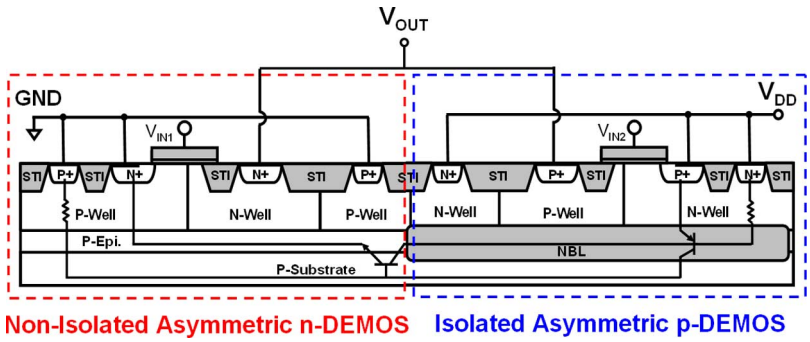

Fig. 5. Device cross-sectional view of the inverter logic circuit consisting of a nonisolated asymmetric n-DEMOS and an isolated asymmetric p-DEMOS.

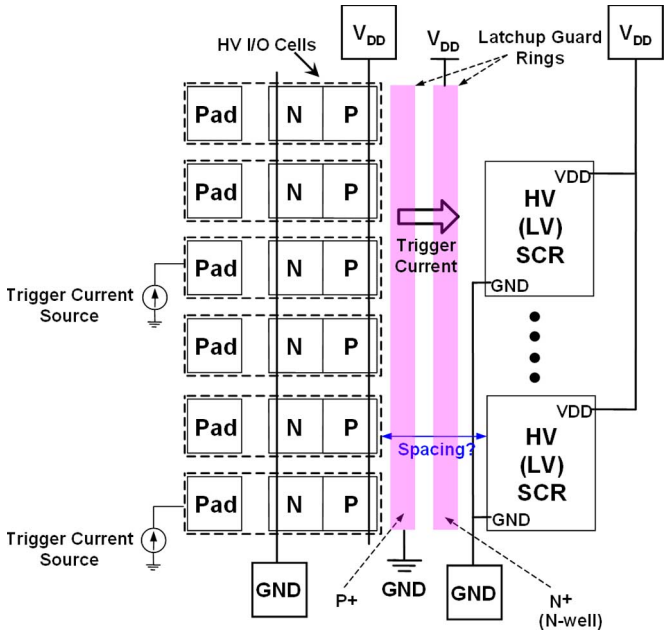

Fig. 6. Proposed test structure to investigate the relations between latchup immunity of internal circuits and the layout spacing from I/O cells to internal circuits.

The proposed test structure to investigate the HV latchup characteristics under latchup current test is shown in Fig. 6 [18]. This structure can be used to investigate the relations between latchup immunity of internal circuits and the layout spacing from I/O cells to internal circuits. Here, the inserted P^+/N^+ guard rings have a fixed width of 5 μm. By injecting the latchup trigger current into the I/O pins, the internal circuits (HV or LV SCR) can be triggered on to a latchup state. Meanwhile, large current will conduct through a low-impedance path from V_{DD} to GND within internal circuits, thus leading V_{DD} of HV (LV) SCR to be pulled down to a low latchup holding voltage.

The device cross-sectional view of the proposed test structure is shown in Fig. 7. The trigger current path to initiate latchup in HV SCR is also depicted. Each HV I/O cell is composed of nonisolated asymmetric n-DEMOS and isolated asymmetric p-DEMOS. To avoid latchup occurring in I/O circuits rather than in internal circuits, each HV I/O cell has a large anode-to-cathode spacing of 50 μm and is equipped with double guard rings to enhance its latchup immunity. The layout top view of Fig. 7 with HV (LV) SCR internal circuits is shown in Fig. 8(a) and (b). With the proposed latchup test structures, the safe and compact latchup design guidelines between HV I/O and HV (LV) internal circuits can be extracted.

B. Experimental Results

For internal circuits of HV and LV SCR, the relations between the minimum negative latchup trigger current on I/O pins and the layout spacing from I/O cells to internal circuits are shown in Fig. 9. For LV SCR, the minimum latchup trigger current increases with spacing from I/O cells to internal circuits, because a larger spacing can reduce more injection current that reaches the internal circuits through recombination. The spacing from I/O cells to internal circuits must be larger than 110 μm to pass the JEDEC latchup criterion ($> \pm 100$ mA). The experimental results are consistent with those in LV CMOS process [18].

For HV SCR, however, the minimum latchup trigger current is fixed at -150 mA and independent of the spacing from I/O cells to internal circuits. The same latchup trigger current dependence can be also observed under positive trigger current test. Failure analyses demonstrated that latchup occurs in HV I/O cells rather than in HV internal circuits (HV SCR), even for a very short distance of 50 μm from the I/O cells to internal circuits. In LV CMOS process, it is easy to design the latchup-free I/O cells by adding double guard rings or enlarging the distance between I/O PMOS and NMOS. However, it is very difficult to design the latchup-free HV I/O cells because of its high operating voltage. The experimental results show that the HV I/O cells are dominant to the latchup immunity in HV chips. It is different with the LV CMOS process where core circuits are the latchup dominant factors. Although HV core circuits can sustain higher injection current (< -150 mA) without latchup occurrence than LV core circuits (< -110 mA), the HV latchup immunity is limited to only -150 mA and cannot be enhanced anymore by enlarging the spacing from I/O to internal circuits. Thus, the dependences of HV device structures on latchup immunity should be investigated to further improve the latchup immunity in HV process. With the latchup-robust HV device structures, the area-efficient HV I/O cells can be designed without enlarging the distance between HV I/O PMOS and NMOS.

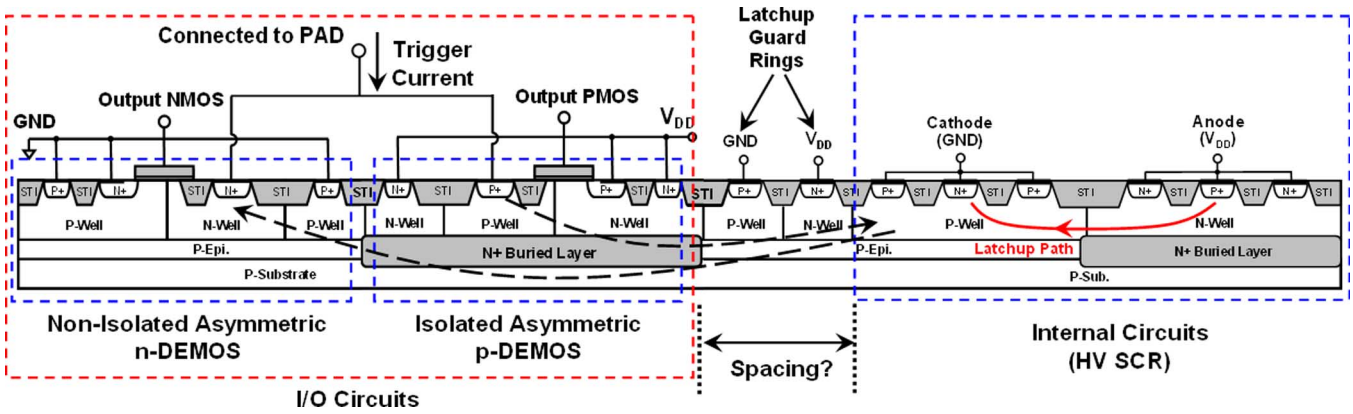

Fig. 7. Device cross-sectional view of the proposed test structure. The trigger current path to initiate latchup in HV SCR is also depicted.

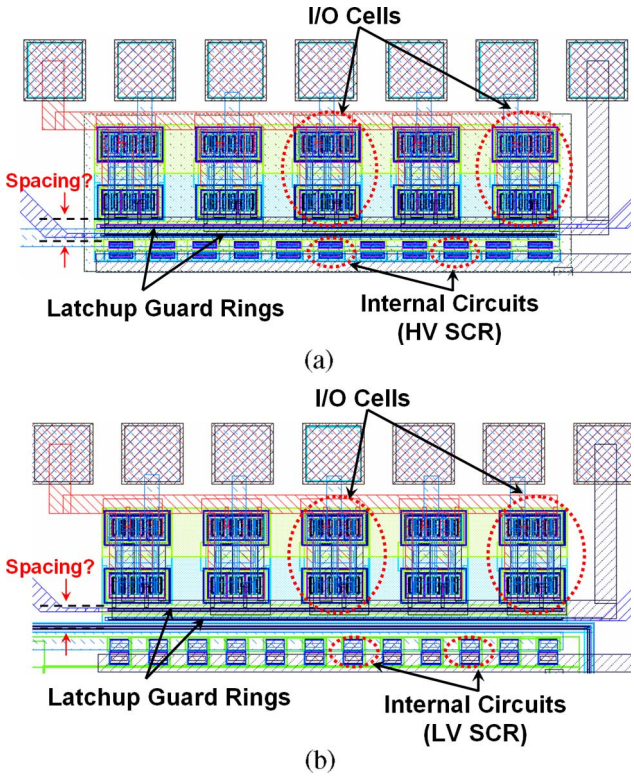

Fig. 8. Layout top views of test structure. (a) Internal circuits with HV SCR. (b) Internal circuits with LV SCR.

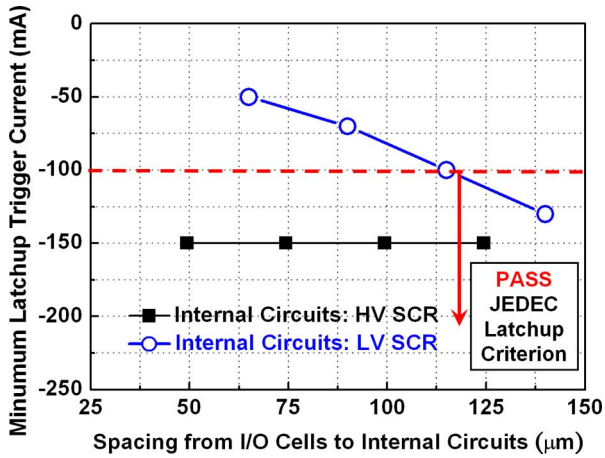

Fig. 9. For internal circuits with HV or LV SCR, the relations between the minimum negative latchup trigger current on I/O pins and the layout spacing from I/O cells to internal circuits.

TABLE I
SUMMARY OF THE DEVICE STRUCTURES OF DEMOS TRANSISTORS IN LATCHUP TEST STRUCTURES A, B, AND C

	n-DEMOS Type	p-DEMOS Type
Latchup Test Structure A (Fig. 10)	Non-Isolated Asymmetric	Isolated Asymmetric
Latchup Test Structure B (Fig. 11)	Non-Isolated Symmetric	Isolated Symmetric
Latchup Test Structure C (Fig. 12)	Isolated Asymmetric	Isolated Asymmetric

IV. Dependence of DEMOS Device Structures on Latchup Immunity

A. Test Structure

Three different HV SCR test structures (test structures A, B, and C) are used to investigate the dependence of DEMOS device structures on latchup immunity. These three latchup test structures can simulate each possible case of the parasitic SCR in HV CMOS ICs with different DEMOS device structures, including asymmetric, symmetric, nonisolated, and isolated device structures. Table I summarizes the device structures of DEMOS transistors in test structures A, B, and C. In addition, layout parameters such as anode-to-cathode spacing and guard ring width are also investigated to find their impacts on latchup immunity. All the latchup test structures are fabricated in a 0.25-μm 40-V CMOS process.

The device cross-sectional views and their layout top views of test structures A, B, and C are depicted in Figs. 10–12, respectively. The P^+ anode (N^+ cathode) is used to simulate the P^+ source of p-DEMOS (N^+ source of n-DEMOS). Once latchup occurs, huge current will conduct from the P^+ anode to the N^+ cathode. To gain a better latchup immunity, both anode and cathode in test structures A, B, and C are surrounded by their base guard rings for complying with foundry's design

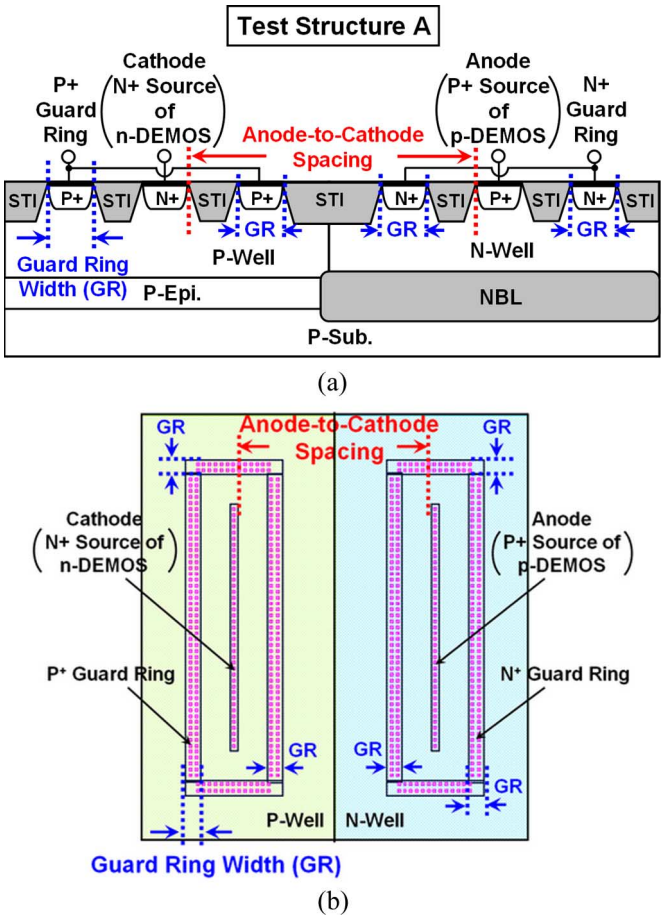

Fig. 10. (a) Device cross-sectional view of test structure A. (b) Layout top view of test structure A. Test structure A is used to simulate the parasitic SCR resulting from the nonisolated asymmetric n-DEMOS and isolated asymmetric p-DEMOS.

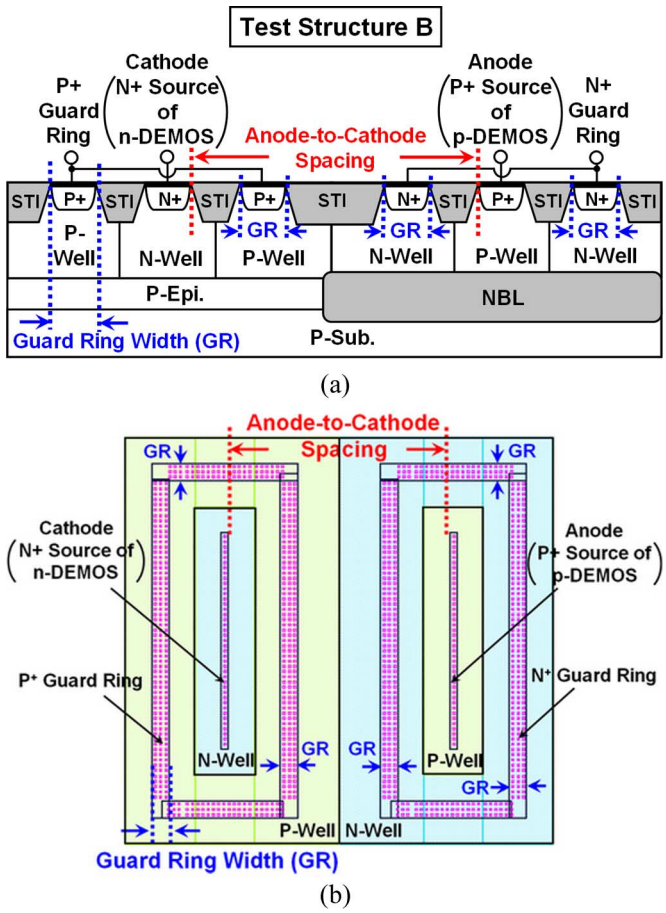

Fig. 11. (a) Device cross-sectional view of test structure B. (b) Layout top view of test structure B. Test structure B is used to simulate the parasitic SCR resulting from the nonisolated symmetric n-DEMOS and isolated symmetric p-DEMOS.

rules, as shown in Figs. 10(b), 11(b), and 12(b). In addition, the spacing from anode (cathode) to its surrounding guard ring in each test structure is kept at its minimum allowable distance according to foundry's design rules.

Test structure A is used to simulate the parasitic SCR resulting from the nonisolated asymmetric n-DEMOS and isolated asymmetric p-DEMOS. Due to the "asymmetric" device structures in both p- and n-DEMOS, there is no P-well (N-well) region enclosing the P^+ anode (N^+ cathode) for source-extended region. In addition, due to the "isolated" device structure in the p-DEMOS, the P^+ anode and N^+ guard rings are fabricated on the NBL above the P-substrate. However, because of the "nonisolated" device structure in the n-DEMOS, the N^+ cathode and P^+ guard rings are fabricated on the P-epi. layer instead of NBL. Test structure B is used to simulate the parasitic SCR resulting from the nonisolated symmetric n-DEMOS and isolated symmetric p-DEMOS. Due to the "symmetric" device structures in both p- and n-DEMOS, the P^+ anode and N^+ cathode are enclosed with the P-well and N-well regions, respectively, for the source-extended regions. Test structure C is used to simulate the parasitic SCR resulting from the isolated asymmetric p-DEMOS and n-DEMOS. Compared with test structures A and B where the n-DEMOS has the "nonisolated" device structure, the n-DEMOS in test structure C has the "isolated" device structure. Thus, the N^+ cathode in test structure C is enclosed (i.e., isolated) by the NBL and its peripheral N-well regions but is not only fabricated on the P-epi. layer as in test structures A and B.

B. Experimental Results

To investigate the latchup characteristics of DEMOS transistors in HV CMOS ICs, the latchup I–V curves are measured in three different latchup test structures A, B, and C, with various layout parameters. In these test structures, P^+ anode and N^+ guard rings are connected to $V_{\rm DD}$, whereas N^+ cathode and P^+ guard rings are connected to GND. By extracting the two dominant parameters of the latchup robustness, namely 1) latchup trigger voltage and 2) latchup holding voltage, from the measured latchup I–V curves, the dependence of DEMOS device structures and their layout styles on latchup immunity can be well evaluated. Latchup trigger voltage represents the minimum applied voltage that can "trigger" the DUT into a latchup state. Latchup holding voltage represents the minimum applied voltage needed for the DUT to "hold" a latchup state. Thus, a higher latchup trigger or holding voltage means a better latchup robustness for the DUT. All the latchup measurements are performed at the room temperature of 25 °C.

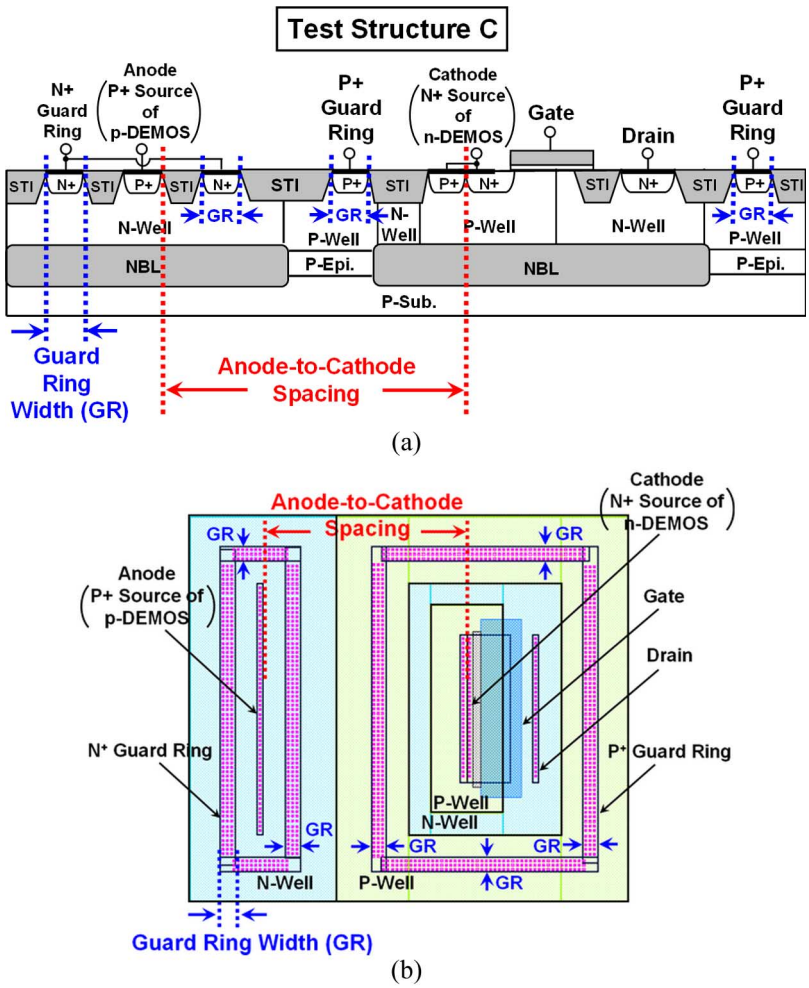

Fig. 12. (a) Device cross-sectional view of test structure C. (b) Layout top view of test structure C. Test structure C is used to simulate the parasitic SCR resulting from the isolated asymmetric n-DEMOS and p-DEMOS.

Compared with the LV devices, HV devices usually require a much larger minimum allowable spacing between the adjacent n-DEMOS and p-DEMOS (i.e., much larger anode-to-cathode spacing) because of the ultrahigh circuit operating voltage. According to foundry's design rule, guard ring structures are also forced for each DEMOS transistor to enhance its latchup robustness. As a result, latchup I–V curves in HV CMOS ICs usually have a much higher holding voltage and holding current (i.e., much higher latchup holding power) than those in LV CMOS ICs. Due to such high latchup power in HV ICs, when the continuous-type curve tracer (e.g., Tektronix 370 A) is used to measure the latchup I–V curves in HV ICs, HV devices are usually damaged before the latchup I–V curves are certainly observed or extracted. In order to avoid the HV devices being damaged so easily under the long-period (microseconds to milliseconds) latchup overstress of continuous-type curve tracer, the TLP generator [21] with a pulsewidth (rise time) of 100 ns ($\sim$10 ns) is used instead in this paper to measure latchup I–V curves of HV latchup test structures. Such 100-ns TLP generator is commonly used for ESD characterization. Compared with the general continuous-type curve tracer whose stress time approximates to the microsecond to millisecond range, the TLP generator has much shorter stress time of 100 ns and limited energy. Thus, by using the TLP generator for latchup I–V characterizations, the HV devices will not be damaged so easily under a latchup state; thus, the latchup trigger and holding voltages can be certainly extracted.

1) Relationships Between Latchup Trigger (Holding) Voltage and Anode-to-Cathode Spacing: The relationships between TLP-measured latchup trigger (holding) voltage and anode-to-cathode spacing for test structures A, B, and C are shown in Fig. 13. Obviously, test structure C (considering the parasitic SCR resulting from isolated asymmetric n-DEMOS and p-DEMOS) has the best latchup immunity due to its highest latchup trigger and holding voltages. For example, latchup trigger voltage (holding voltage) can be as high as 97 V (48 V) for test structure C, although the anode-to-cathode spacing is only as short as 27.5 μm, as its TLP-measured latchup I–V curve shown in Fig. 14. Because of a high latchup holding voltage of 48 V, which is higher than 40 V of the normal circuit operating voltage, test structure C can be latchup free. However, latchup trigger voltage (holding voltage) can be only enhanced up to 71 V (36 V) for test structure A and up to 70 V (37 V) for test structure B, although the anode-to-cathode spacing is as long as 31.6 μm, as their TLP-measured latchup I–V curves shown in Figs. 15 and 16. For test structures A, B, and C,

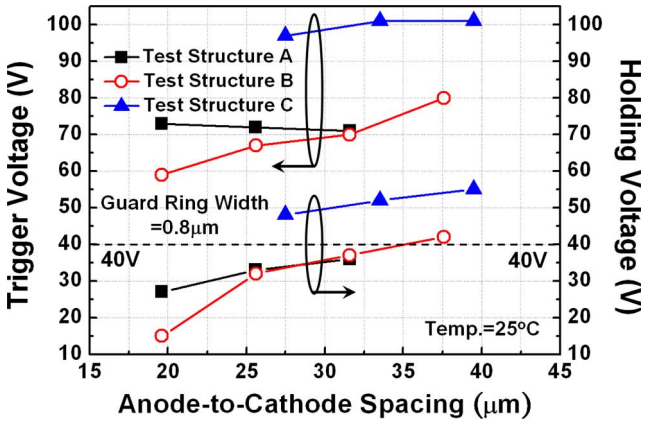

Fig. 13. Relationships between TLP-measured latchup trigger (holding) voltage and anode-to-cathode spacing for test structures A, B, and C.

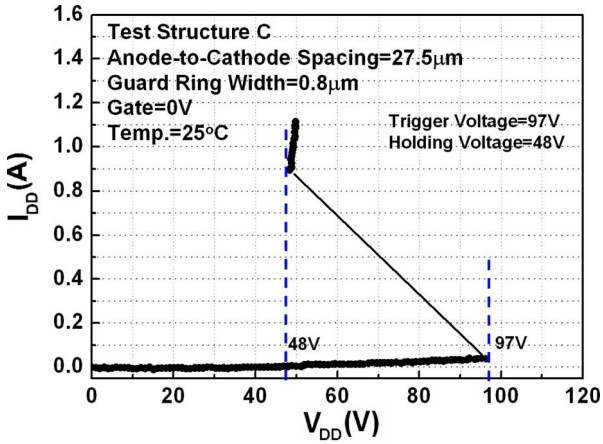

Fig. 14. TLP-measured latchup I–V characteristics of test structure C with anode-to-cathode spacing of 27.5 μm.

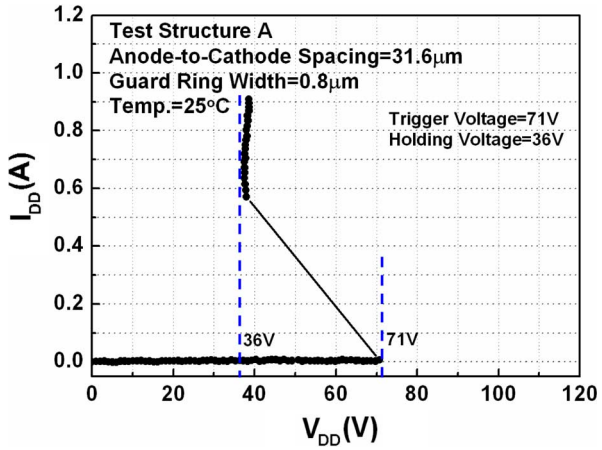

Fig. 15. TLP-measured latchup I–V characteristics of test structure A with anode-to-cathode spacing of 31.6 μm.

increasing anode-to-cathode spacing can improve the latchup immunity. However, it cannot help test structures A and B to gain a good latchup immunity as in test structure C.

Compared with test structures A and B, which have the traditional four-layer p-n-p-n latchup path, test structure C has a six-layer p-n-p-n-p-n latchup path due to the isolation region in isolated n-DEMOS. This six-layer latchup path consists of

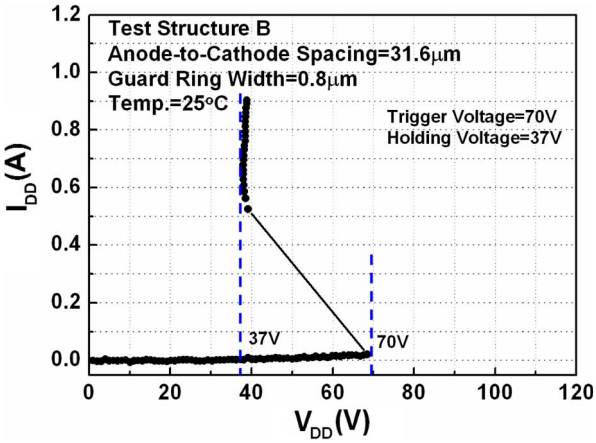

Fig. 16. TLP-measured latchup I–V characteristics of test structure B with anode-to-cathode spacing of 31.6 μm.

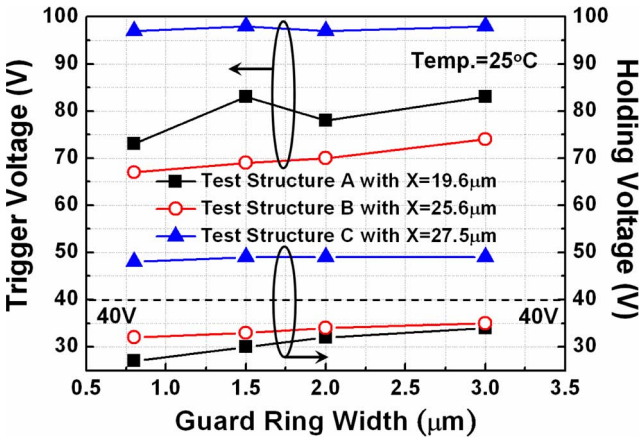

Fig. 17. Relationships between TLP-measured latchup trigger (holding) voltage and guard ring width for test structures A, B, and C with anode-to-cathode spacing (parameter X) of 19.6, 25.6, and 27.5 μm, respectively.

P$^+$ anode, N-well, P-well, NBL, P-well, and N$^+$ cathode, in sequence. Due to the isolation region in isolated n-DEMOS, both holes and electrons need to overcome an additional NBL/P-well junction barrier to initiate a positive feedback latchup event. Such unique characteristics will lead to a prominent latchup immunity, i.e., high latchup trigger and holding voltages, in test structure C. In addition, compared with test structure A, test structure B has a shorter basewidth in its parasitic vertical p-n-p and lateral n-p-n BJTs because of the additional source drift region (i.e., longer emitter width). A shorter basewidth will lead to a higher current gain of the parasitic BJTs, hence degrading the latchup robustness [13] (i.e., lower latchup trigger and holding voltages) in test structure B. In test structures A and B, however, such difference of the basewidth is not obvious under a larger anode-to-cathode spacing. As a result, test structure A has a better latchup immunity (i.e., higher latchup trigger and holding voltages) than test structure B under a shorter anode-to-cathode spacing of < 25.6 μm, as shown in Fig. 13. For a larger anode-to-cathode spacing of > 25.6 μm, however, both test structures A and B have almost the same latchup trigger and holding voltages.

2) Relationships Between Latchup Trigger (Holding) Voltage and Guard Ring Width: Fig. 17 shows the relationships

TABLE II
SUMMARY OF THE DEPENDENCE OF DEMOS DEVICE STRUCTURES ON LATCHUP ROBUSTNESS

	n-DEMOS Type	p-DEMOS Type	Latchup Robustness
Latchup Test Structure A (Fig. 10)	Non-Isolated Asymmetric	Isolated Asymmetric	Poor
Latchup Test Structure B (Fig. 11)	Non-Isolated Symmetric	Isolated Symmetric	Poor
Latchup Test Structure C (Fig. 12)	Isolated Asymmetric	Isolated Asymmetric	Good

between TLP-measured latchup trigger (holding) voltage and guard ring width for test structures A, B, and C with anode-to-cathode spacing (parameter X) of 19.6, 25.6, and 27.5 μm, respectively. For test structures A and B, increasing guard ring width can moderately improve the latchup immunity. For example, when guard ring width increases from 0.8 to 3 μm, latchup trigger voltage (holding voltage) can be enhanced from 73 V (26 V) to 83 V (34 V) in test structure A and from 67 V (32 V) to 74 V (35 V) in test structure B. For test structure C, however, increasing guard ring width only has little improvement on latchup immunity. Thus, in test structure C, the dominant factor to gain a good latchup immunity is the isolation region of isolated n-DEMOS, but not the guard ring structure.

From the comprehensive experimental results in Figs. 13 and 17, Table II summarizes the dependence of DEMOS device structures on latchup robustness. HV ICs with isolated n-DEMOS (test structure C) have much better latchup immunity than those with nonisolated n-DEMOS (test structures A and B). Thus, the isolated n-DEMOS in test structure C is the dominant factor to enhance the latchup robustness in HV ICs. However, symmetric or asymmetric DEMOS in test structures A and B has no great impact to improve the latchup immunity, although asymmetric DEMOS has better latchup immunity than symmetric DEMOS under a shorter (< 25.6 μm) anode-to-cathode spacing, as shown in Fig. 13. In addition, increasing both anode-to-cathode spacing and guard ring width can enhance the latchup immunity. However, continuously increasing anode-to-cathode spacing or guard ring width will lead to a larger layout area and higher cost. More importantly, using the isolated n-DEMOS in HV ICs can gain much better latchup robustness than only increasing anode-to-cathode spacing or guard ring width in layout schemes. Thus, using the isolated n-DEMOS in HV ICs not only can gain a good latchup immunity but also can save the total chip layout area.

V. DEVICE SIMULATION

The experimental measured latchup characteristics of different HV latchup test structures can be verified with 2-D device simulation. The device structures used in 2-D device simulation for test structures A, B, and C are shown in Fig. 18(a)–(c), respectively. To accurately verify the experimental results, these device structures in device simulation have the same layout parameters as the silicon test chips. For example, the anode-to-cathode spacing in device simulation of test structures A, B, and C are 31.6, 31.6, and 27.5 μm, respectively, which are the same as silicon test chips in Figs. 14–16. Guard ring width in test structures A, B, and C is a fixed value of 0.8 μm in device simulation. With the aid of 2-D device simulation, latchup I–V curves and their 2-D current flow lines can be clearly observed to determine which device structure will be dominant to enhance the latchup robustness in HV ICs.

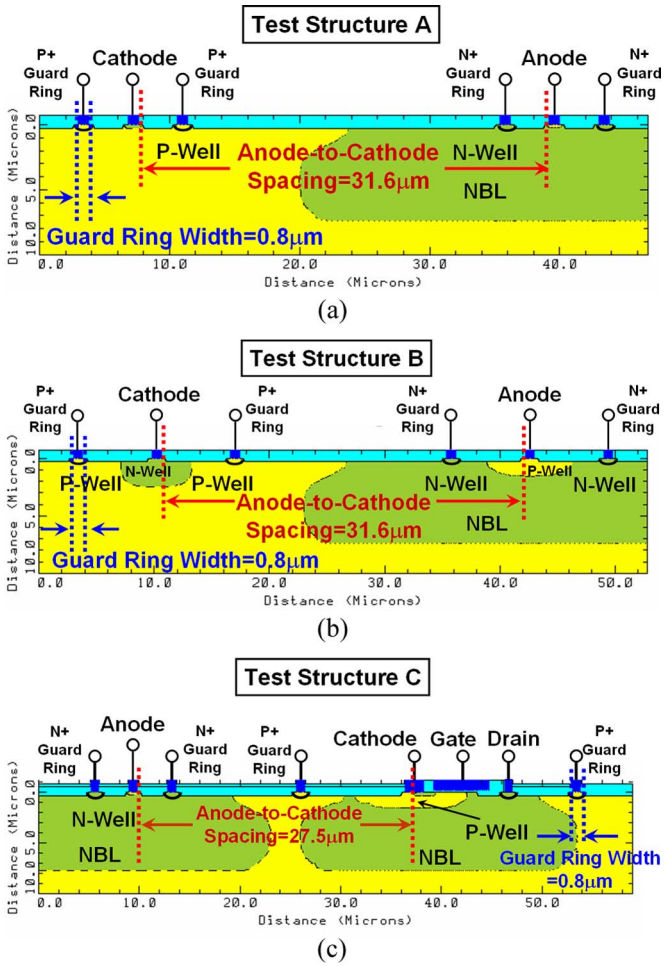

Fig. 18. Device structures used in the 2-D device simulation. (a) Test structure A. (b) Test structure B. (c) Test structure C. These device structures have the same layout parameters as the silicon test chips.

The simulated latchup I–V curves of test structures A, B, and C are shown in Fig. 19. These simulated I–V curves are performed by connecting P^+ anode and N^+ guard rings to V_{DD} while connecting N^+ cathode and P^+ guard rings to GND. The simulation results in Fig. 19 are consistent with the measured results in Fig. 13, where test structure C has the best latchup immunity because of its highest latchup trigger and holding voltages. For example, latchup trigger (holding) voltage can be as high as 94 V (41 V) for test structure C, although the anode-to-cathode spacing is only as short as 27.5 μm. However, latchup trigger (holding) voltage can be only enhanced up to 72 V (27 V) for test structure A and up to 62 V (26 V) for test structure B, although they have a larger anode-to-cathode spacing of 31.6 μm. The simulated holding voltage of 41 V (> 40 V) in test structure C is consistent with the experimental

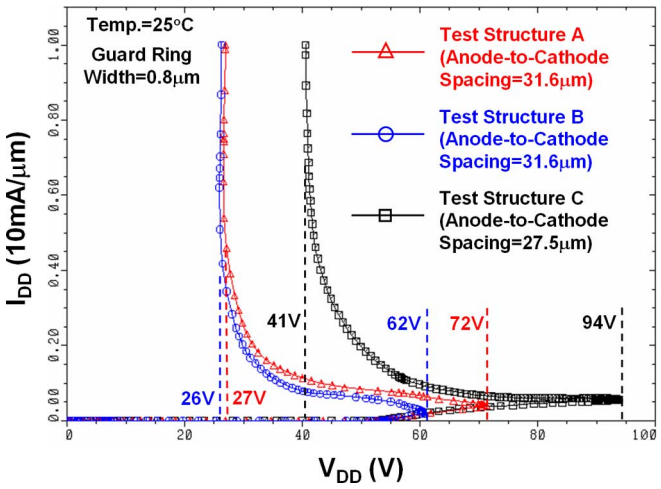

Fig. 19. Simulated latchup I–V characteristics for test structures A and B with anode-to-cathode spacing of 31.6 μm and for test structure C with anode-to-cathode spacing of 27.5 μm. All these test structures have the same guard ring width of 0.8 μm.

result in Fig. 14 that test structure C can be latchup free. In addition, the simulation results are also consistent with the experimental result in Figs. 15 and 16 that both test structures A and B have almost the same latchup holding voltage ($\sim$27 V). The only difference between the experimental and simulated results is that both test structures A and B have almost the same latchup trigger voltage ($\sim$71 V) in the experimental result, but test structure A has a larger one (72 V) than test structure B (62 V) in device simulation.

The simulated 2-D current flow lines under latchup condition for test structures A, B, and C are shown in Fig. 20(a)–(c), respectively. Clearly, concentrated current flow lines will conduct from P^+ anode (V_{DD}) to N^+ cathode (GND) under latchup condition. Compared with test structures A and B, which have the traditional four-layer p-n-p-n latchup path, test structure C has a unique six-layer p-n-p-n-p-n latchup path because of the isolated region in n-DEMOS, as shown in Fig. 20(c). Thus, it will lead test structure C to have much better latchup robustness than test structure A or B.

VI. Discussions

Both experimental results and device simulation show that the additional isolation region in isolated n-DEMOS is the major reason to make better latchup immunity in structure C. This phenomenon can be reasonably explained by the concept of potential energy barrier. This concept can clearly explain that such isolation region can generate an additional P-substrate/NBL (P-well/N-well) junction barrier, greatly reducing the electron or hole current that can initiate latchup.

A. Reducing Hole Current to Initiate Latchup

The device structure C and the energy band diagram along the A$-$A$'$ (B$-$B$'$) direction are shown in Fig. 21(a) and (b), respectively. To turn on the emitter–base junction of the parasitic n-p-n BJT, the hole current needs to be collected by the cathode

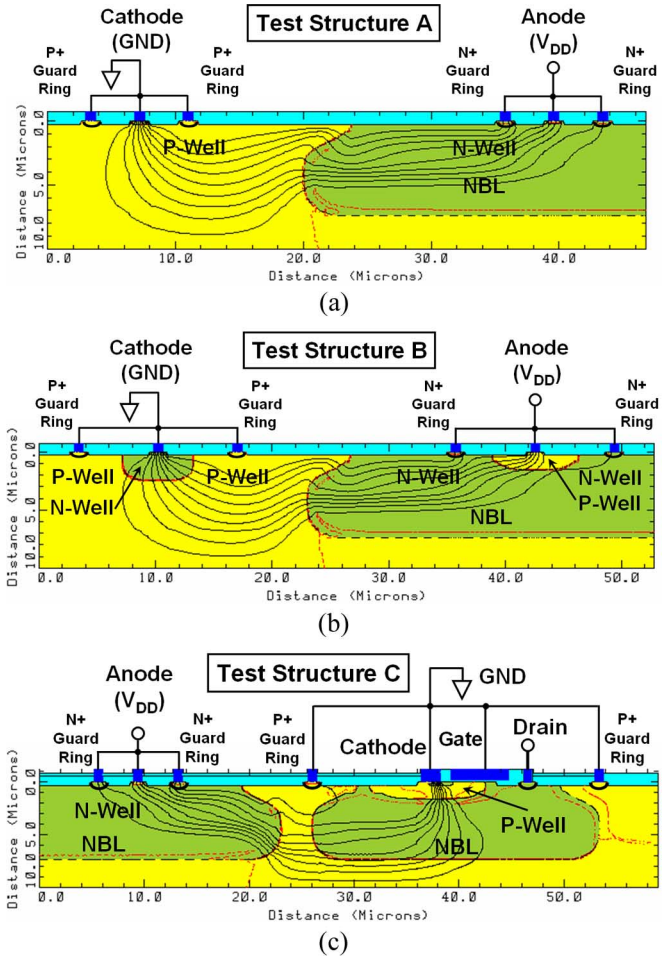

Fig. 20. Simulated 2-D current flow lines under latchup condition. (a) Test structure A. (b) Test structure B. (c) Test structure C.

(P^+ well contact tied to N^+ source of n-DEMOS). Thus, the hole current needs to flow from the outside of n-DEMOS to the cathode along the A$-$A$'$ (B$-$B$'$) direction. However, due to the isolation region of isolated n-DEMOS, the majority holes need to overcome an additional P-substrate/NBL (P-well/N-well) junction barrier to be collected by the cathode. As a result, larger hole current is necessary to turn on the parasitic n-p-n BJT in the isolated n-DEMOS, leading to a better latchup robustness in test structure C.

B. Reducing Electron Current to Initiate Latchup

Although the parasitic n-p-n BJT is turned on, its injection electrons also face the same P-substrate/NBL (P-well/N-well) junction barrier due to the isolation region of isolated n-DEMOS, as shown in Fig. 21(c). Such junction barrier can reduce the numbers of electrons that may escape the isolation region along the A$-$A$'$ (B$-$B$'$) direction. These escaping electrons can be subsequently collected by the anode (tied to N^+ well contact with V_{DD} potential) outside the isolation region, forming the electron current to turn on the parasitic p-n-p BJT. Thus, the electron current contributing to turning on the parasitic p-n-p BJT can be reduced, leading to a better latchup robustness in test structure C.

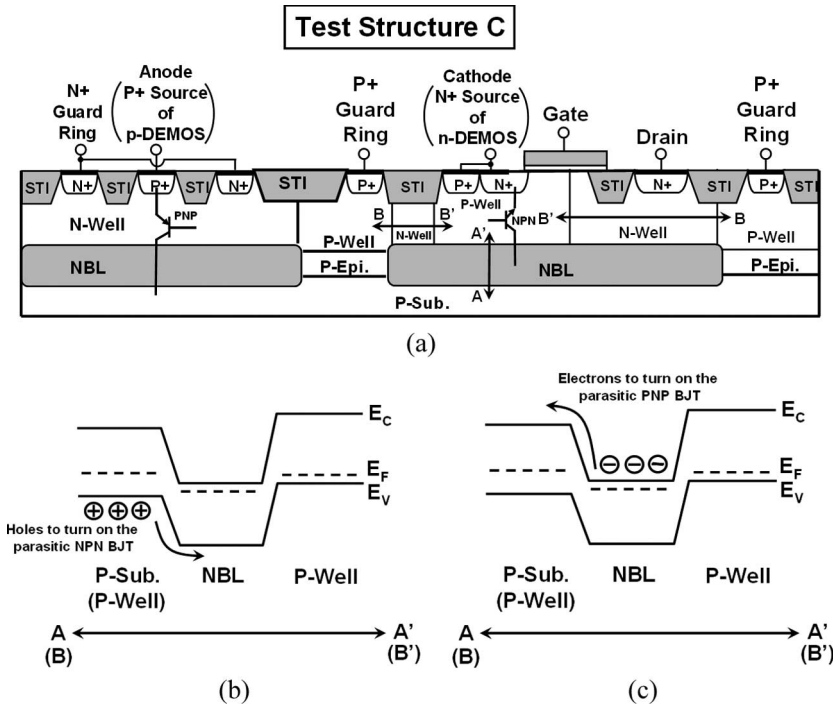

Fig. 21. (a) Device structure of test structure C. (b) Energy barrier seen by the holes along the A−A′ (B−B′) direction. (c) Energy barrier seen by the electrons along the A−A′ (B−B′) direction.

The concept of potential energy barrier can reasonably explain why the isolated n-DEMOS can greatly enhance the HV latchup immunity. In addition, combing with the experimental results and device simulation, the concept of potential energy barrier can help investigate the HV latchup characteristics more comprehensively.

VII. Conclusion

HV latchup characteristics are investigated in a 0.25-μm 2.5-V/40-V CMOS process. Different with the LV CMOS process where core circuits are the latchup dominant factors, HV I/O cells are dominant to the latchup immunity in HV chips. Thus, HV latchup immunity cannot be improved anymore by enlarging the spacing from I/O to internal circuits. To further improve the latchup immunity in HV chips, three latchup test structures are used to evaluate the latchup-robust HV device structures. Furthermore, layout parameters such as anode-to-cathode spacing and guard ring width are also investigated to find their impacts on latchup immunity. In order to avoid the HV latchup test structures being damaged so easily under the long-period (microseconds to milliseconds) latchup overstress of continuous-type curve tracer, the TLP generator with pulsewidth of 100 ns and limited energy is used in this paper for latchup I–V measurements. With the TLP-measured latchup I–V curves of different latchup test structures, it was demonstrated that HV ICs with isolated n-DEMOS (test structure C) can gain much better latchup immunity than those with nonisolated n-DEMOS (test structures A and B). However, symmetric or asymmetric DEMOS has no great impact to improve the latchup robustness in HV ICs. The concept of potential energy barrier can reasonably explain why the HV ICs with isolated n-DEMOS can gain the good latchup robustness. All the TLP-measured latchup I–V characteristics on different HV latchup test structures can be qualitatively and quantitatively verified with 2-D device simulation. Both the proposed latchup test structures and simulation methodologies can be further applied to extract safe and compact design rule for latchup prevention in HV CMOS ICs.

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