Impact of Channel Dangling Bonds on Reliability Characteristics of Flash Memory on Poly-Si Thin Films

Yu-Hsien Lin, *Student Member, IEEE*, Chao-Hsin Chien, *Associate Member, IEEE*, Tung-Huan Chou, Tien-Sheng Chao, *Senior Member, IEEE*, and Tan-Fu Lei, *Member, IEEE*

***Abstract*—In this letter, we fabricated the poly-Si–oxide–nitride–oxide–silicon (SONOS)-type Flash memories on polycrystalline-silicon thin films and found that dangling bonds presented along the grain boundaries in the channel significantly influence their reliability characteristics in the aspects of charge storage, drain disturbance, and gate disturbance. Employing a powerful defect passivation technique, i.e., NH_3 plasma treatment, the charge storage capability was clearly observed to be remarkably improved. Even so, the hydrogenated polycrystalline-silicon thin-film transistors (poly-Si-TFTs) still suffered from serious drain and gate disturbances, which exhibited behaviors that are quite specific and undoubtedly distinct from those observed in the conventional SONOS-type memories on single crystalline substrates.**

***Index Terms*—Dangling bonds, Flash memories, polycrystalline-silicon thin-film transistor (poly-Si-TFT), poly-Si–oxide–nitride–oxide–silicon (SONOS)-type memories.**

I. Introduction

POLYCRYSTALLINE-SILICON thin-film transistors (poly-Si-TFTs) have been widely used for the application of active-matrix liquid-crystal display [1]. Owing to their high mobility characteristic, poly-Si-TFTs have great capability to serve as the building block for the high-speed driving circuit in the liquid-crystal display. Nowadays, prompted by continuously progressive manufacturing technologies, people are rigorously considering the feasibility of integrating an entire system on top of the panel [2]. Of course, the poly-Si-TFTs have the niche because of their superior performance than their counterparts. Since a system shall include the functionality of memory, efforts shall be paid in order to successfully integrate memories, such as electrically erasable programmable read-only memory and Flash memory, directly on the panel [3], [4]. Poly-Si–oxide–nitride–oxide–silicon (SONOS)-type nonvolatile memory based on discrete storage nodes possesses great potential for the application of the poly-Si-TFT memories with their reported superior characteristics [5].

In our previous work [6], we found that their long-term reliability characteristics, including retention, drain disturbance, and gate disturbance, displayed distinct behaviors from those observed in the conventional SONOS-type Flash memories. We speculated that these specific characteristics are intimately linked to the presence of the inherent defects along the grain boundaries [7], [8]. Extracting trap state density in the channel and comparing the samples with and without NH_3 plasma treatment [9], [10], we thought that these specific drain and gate disturbances do arise from the breaking of the weak Si–H bonds induced by the acting stresses, and the filling of these unpassivated traps by the gate-bias-induced electrons, in turn, leads to the increased threshold voltage over stress time.

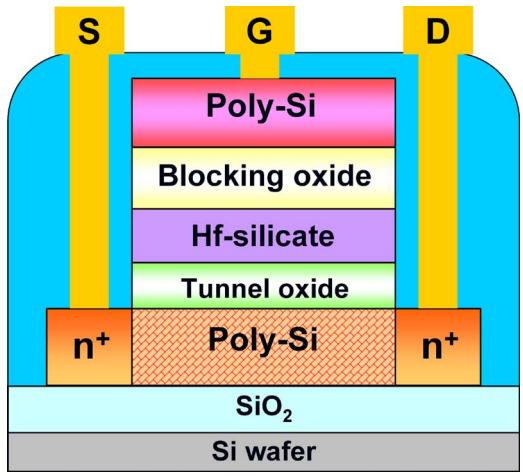

Fig. 1. Illustrative structure of the poly-Si-TFT memory device.

II. Device Fabrication

Fig. 1 shows the illustrative structure of the poly-Si-TFT memory device. First, 500-nm-thick thermal oxide was grown on the Si wafers by furnace system to simulate the glass substrate. All the experimental devices in this study were fabricated on the thermally oxidized Si wafers subsequently. Then, a 100-nm-thick amorphous-silicon layer was deposited on the thermally oxidized Si wafers by dissociation of SiH_4 gas in low-pressure chemical vapor deposition (LPCVD) at 550 °C.

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Y.-H. Lin and T.-F. Lei are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 30050, Taiwan, R.O.C.

C.-H. Chien is with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 30050, Taiwan, R.O.C, and also with the National Nano Device Laboratory, Hsinchu 30050, Taiwan, R.O.C. (e-mail: chchien@mail.ndl.org.tw; chchien@faculty.nctu.edu.tw).

T.-H. Chou and T.-S. Chao are with the Institute of Electrophysics, National Chiao Tung University, Hsinchu 30050, Taiwan, R.O.C.

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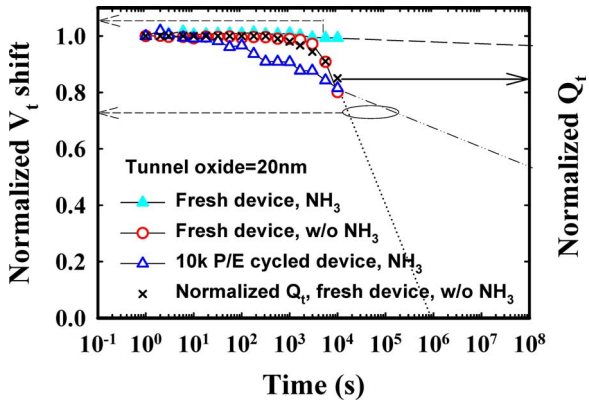

Fig. 2. Retention characteristics of the nonhydrogenated, fresh, and 10 000 P/E cycled hydrogenated poly-Si-TFT memories at $T = 25$ °C. Trap state densities Q_T of the samples were extracted by Levinson *et al.* [11] and Proano *et al.* [12].

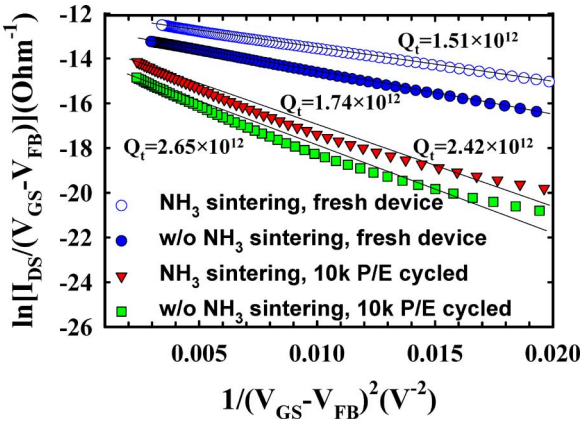

Fig. 3. $\ln[I_D/(V_{\rm GS} - V_{\rm FB})]$ versus $1/(V_{\rm GS} - V_{\rm FB})^2$ curves at $V_{\rm DS} = 0.1$ V, and high $V_{\rm GS}$ for the three kinds of poly-Si-TFT memories.

Subsequently, solid-phase crystallization was performed at 600 °C for 24 h in N_2 ambient to induce phase transformation. Individual active regions were then patterned and defined. After a standard RCA cleaning, the tunneling oxides with two different thicknesses were deposited by plasma-enhanced chemical vapor deposition (PECVD) with tetraethyloxysilane precursor at 350 °C: One was of 9 nm, and the other was of 20 nm. The following deposition of 20-nm-thick hafnium silicate thin films was conducted by cosputtering method. A blocking oxide of about 33 nm was again deposited by PECVD. A 200-nm-thick poly-Si was deposited to serve as the gate electrode by LPCVD. Then, gate electrode was patterned, and the regions of source, drain, and gate were doped by a self-aligned phosphorous ion implantation at the dosage and energy of 5×10^{15} ions/cm^2 and 40 keV, respectively. After source/drain formation, which was activated at 600 °C for 24-h passivation, and metallization, NH_3 plasma sintering was performed to complete the fabrication of the poly-Si-TFT memories. For comparison, some of them were not subjected to plasma treatment.

III. Results and Discussion

Fig. 2 shows the retention behaviors of the poly-Si-TFT Flash memories with and without NH_3 plasma treatment. We could clearly see that the memory device with NH_3 plasma treatment depicted a better room-temperature retention performance than that without NH_3 plasma treatment. This result implies that the hydrogenation by NH_3 plasma treatment is closely related to the charge storage capability of the poly-Si-TFT Flash memories. The retention characteristic of a 10 000 program/erase (P/E) cycled hydrogenated memory device is also shown for comparison. For the P/E cycling, the programming was conducted with the condition of $V_g = V_d = 12$ V for 1 ms, and the erasing condition was set at $V_g = -10$ V and $V_d = +10$ V, respectively, for 10 ms. The charge loss undoubtedly became worse and started only after a few tenths of seconds due to the induced defects after cycling. This behavioral feature was obviously different from that in the case without NH_3 treatment.

In order to clarify the mechanism responsible for this phenomenon, trap state densities Q_T of the samples were extracted. Fig. 3 exhibits the plots of $\ln[I_D/(V_{\rm GS} - V_{\rm FB})]$ versus $1/(V_{\rm GS} - V_{\rm FB})^2$ curves at low $V_{\rm DS}$ and high $V_{\rm GS}$. The Q_T values for the poly-Si-TFTs were estimated by Levinson *et al.* [11] and Proano *et al.* [12] from the slopes of these curves. The hydrogenated poly-Si-TFT exhibits a Q_T value of 1.51×10^{12} cm^{-2}, whereas the nonhydrogenated poly-Si-TFT has a value of 1.74×10^{12} cm^{-2}. To further study the hydrogenated passivation effect near the interface, the effective interface trap states densities N_T near the SiO_2/poly-Si interface were also calculated. From the subthreshold swing (S.S.), by neglecting the depletion capacitance, N_T can be expressed as [13]

$$N_T = [(\text{S.S.}/\ln 10)(q/kT) - 1)]\,(C_{\rm ox}/q)$$

where $C_{\rm ox}$ is the capacitance of the gate oxide. The N_T values of the nonhydrogenated and hydrogenated poly-Si-TFTs are 1.82×10^{12} and 1.63×10^{12} cm^{-2}, respectively. After 10 000 P/E cycling, the extracted Q_T values and the N_T values are 2.42×10^{12} and 2.68×10^{12} cm^{-2}, respectively, for the hydrogenated sample, and 2.65×10^{12} and 2.91×10^{12} cm^{-2}, respectively, for the unpassivated sample. In Fig. 2, the evolution of the Q_T value as a function of time for the sample without NH_3 treatment is also plotted. We found that the tendency traced well with the charge loss behavior. In contrast, the Q_T value remains unchanged for the P/E cycled hydrogenated memory device (not shown). These results explain why two different charge loss trends were observed between the nonhydrogenated and the cycled hydrogenated ones. In other words, we believe that the surprisingly steep charge loss in the case without NH_3 treatment is caused by the defects at the grain boundaries, whereas the smooth and early retention degradation of the 10 000 P/E cycled memory device arises from the combining effects of the generated traps in the bulk of the tunnel oxide and those traps produced near the interface during cycling.

Disturbance is a very important reliability concern for the Flash memories. It often takes place during programming a specific cell in the NOR Flash memory, which operation leads to the unwanted electrical stress acting on those neighboring cells connected to the same bitline, i.e., drain disturbance, and to the same wordline, i.e., gate disturbance. Fig. 4 shows the drain disturb characteristics of the poly-Si-TFT Flash memories in the programmed state. Two different drain voltages were applied, i.e., $V_d = 10$ and 12 V, with the other terminals grounded. For the hydrogenated samples, we observed that a

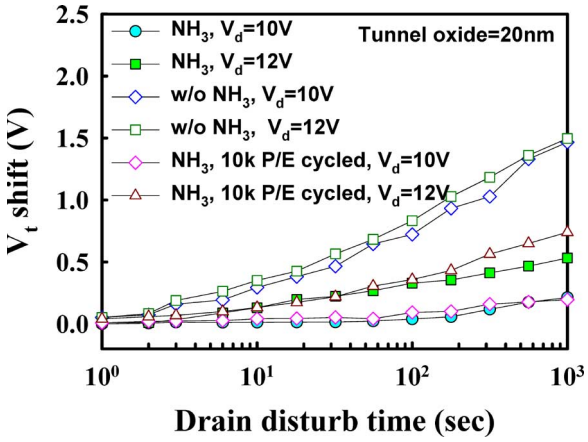

Fig. 4. Drain disturb characteristics of the nonhydrogenated, fresh, and 10 000 P/E cycled hydrogenated poly-Si-TFT memories.

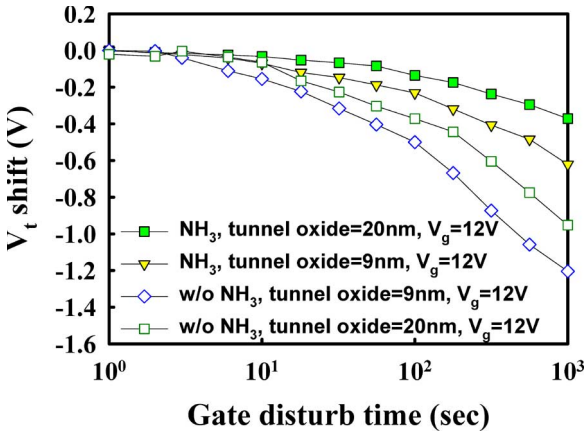

Fig. 5. Gate disturb characteristics of the nonhydrogenated, fresh, and 10 000 P/E cycled hydrogenated poly-Si-TFT memories.

drain disturb ($\Delta V_t \sim 0.7$ V) existed for the cycled memory device under a drain disturb of 12 V for 1000 s. However, for the nonhydrogenated device, the degradation was quite severe. This result is believed to be due to the presence of the localized traps along the grain boundaries in the channel, which can significantly affect the V_t shift through drain bias stressing [14], [15]. Here, we can confirm our former speculation—the generated traps after cycling locate mostly near the Si/SiO_2 interface rather than at the grain boundaries deep inside the channel [16]—since the cycled hydrogenated device depicts higher Q_T value but less significant disturbance. Fig. 5 shows the gate disturb characteristics of both fresh hydrogenated and nonhydrogenated memory devices in the erased state with two different tunnel oxide thicknesses ($t = 9$ and 20 nm). The applied gate voltage was 12 V, with the other terminals grounded. Although the nonhydrogenated devices again exhibited poorer gate disturb results, the V_t shift decreased rather than increased as the stressing time is increased, which is in strong contrast to the situation in the conventional SONOS-type memories [17]. Since no cycling had been done for the fresh devices, the decrease in V_t seems unlikely to be caused by the electron detrapping. Thus, we thought that this phenomenon is ascribed to the filling of the traps at the grain boundaries by the induced electrons by the applied gate voltage. Moreover, the larger V_t shift in the thinner oxide case is due to the more induced electrons by the higher electric field. These results mean that the defects in the channel significantly influence not only the data retention but also the drain and gate disturbances of the poly-Si-TFT Flash memories.

IV. Conclusion

In this letter, we demonstrated that the reliability characteristics of a poly-Si-TFT memory device in terms of retention, drain disturbance, and gate disturbance are closely related to the defects along the grain boundaries in the channel. The NH_3 plasma treatment is a useful method that can improve the qualities of both the SiO_2/poly-Si-channel interface and the channel and, in turn, lead to better long-term stability of the poly-Si-TFT memories.

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