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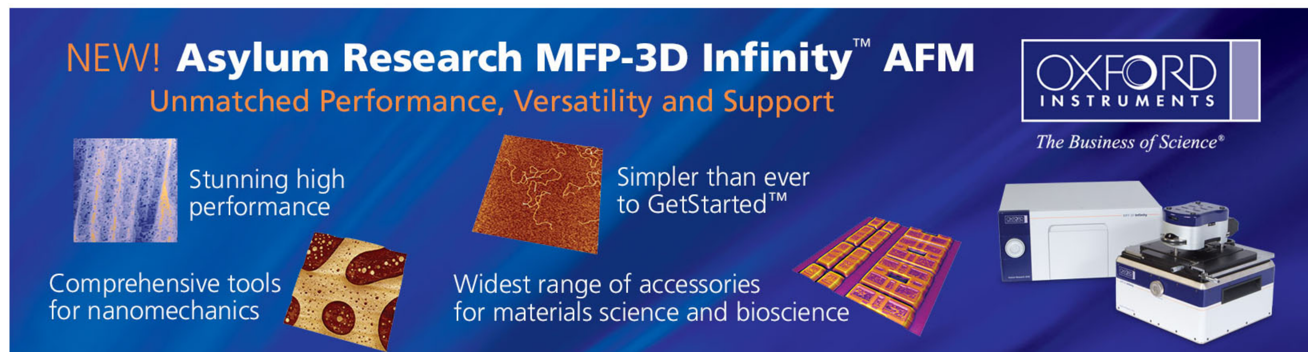

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Impacts of a polycrystalline-silicon buffer layer on the performance and reliability of strained *n*-channel metal-oxide-semiconductor field-effect transistors with SiN capping

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Characteristics of *n*-channel metal-oxide-semiconductor field-effect transistors with SiN capping were investigated in this work. Although the SiN capping could dramatically enhance the carrier mobility and thus the device drive current, the resistance to hot-carrier degradation is compromised as well, owing to the large amount of hydrogen contained in the SiN layer which may diffuse into the channel region during the process. To eliminate this shortcoming, the insertion of an ultrathin (10 nm) polycrystalline-silicon buffer layer between the gate and the SiN capping was proposed and demonstrated to restore the hot-carrier reliability of the devices without compromising the current enhancement due to the SiN capping. © *2007 American Institute of Physics*.
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Channel-strain engineering has emerged as one of the most effective remedies to boost the drive current in the scaled devices.[1–5] This could be done by either applying a high biaxial tensile strain to the channel region with a SiGe virtual substrate,[1] or uniaxially straining the channel with strain boosters, such as stress liner,[2] embedded SiC in the source/drain (S/D) region,[3] and shallow trench isolation.[4] Among these approaches, a SiN capping layer over the gate of *n*-channel metal-oxide-semiconductor field-effect-transistors (NMOSFETs) serving as the contact etch-stop layer has demonstrated its potential for large performance gains.[5] Such scheme is attractive and practical because it can be easily implemented using integrated circuit processing. Nevertheless, attentions should now be focused on the associated reliability issues for practical applications. Currently, device degradation caused by hot carriers represents one of the most critical reliability issues in strain-channel NMOSFETs.[6,7] Although the physical mechanisms and characteristics of hot electron degradation have been extensively examined,[8,9] there seems to be very few works that investigate the impact of SiN capping. Furthermore, the deposition of a buffer layer prior to the SiN capping on the hot-carrier reliability of the strained devices has not been reported in literature. In this work, we clearly demonstrated that the insertion of an undoped ultrathin polycrystalline silicon (poly-Si) is useful in relieving the aggravated hot-carrier degradation caused by the SiN capping layer.

NMOSFETs characterized in this study were with 3 nm thermal oxide grown in a vertical furnace in O_2 at 800 °C, and 150-nm-thick n^+ poly-Si layer as the gate electrode. After the gate formation, most samples were capped with a SiN layer of 300 nm, deposited by a low-pressure chemical vapor deposition (LPCVD) system (denoted as the SiN-capped split); the SiN deposition step was deliberately skipped for some wafers to serve as the controls (denoted as the control split). For some SiN-capped samples, a thin undoped poly-Si buffer layer of 10 nm was capped prior to the SiN deposition (denoted as the BL-POLY split). The SiN deposition was performed at 780 °C with SiH_2Cl_2 and NH_3 as the reaction precursors. For some of the SiN-capped wafers, the SiN layer was deliberately removed after deposition in order to evaluate the impact of SiN deposition process itself on the device performance (denoted as SiN-removal split). The topmast passivation layer of all wafers is a 300-nm-thick tetraethoxysilane layer, followed by contact holes and metallization processes. To clarify the effect associated with the thermal budget of SiN deposition, the control split received a placebo annealing in N_2 ambient at the same temperature and duration as those of SiN deposition process. Finally, the processing steps were completed with a forming gas annealing at 400 °C. Electrical characterizations were performed using an HP 4156 system.

The stress induced by LPCVD-SiN layer with and without 10-nm-thick poly-Si buffer layer was first examined by probing the blanket films deposited on bare Si wafers. We confirmed that the stresses are tensile in nature with a magnitude of around 300 MPa for all samples, irrespective of poly-Si presence. Figure 1 shows the percentage increase of transconductance with respect to the control samples for SiN-capped, BL-POLY, and SiN-removal samples, as a function of channel length. We can see that the transconductance enhancement reaches about 33% at a channel length of 0.4 μm for SiN-capped and BL-POLY samples. When SiN

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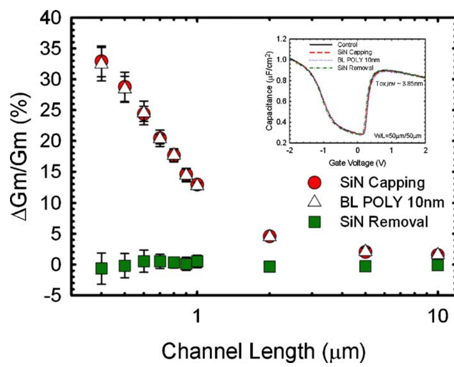

FIG. 1. (Color online) Percentage increase of transconductance vs channel length for different splits of samples with respect to the control ones. Each datum point represents the mean measurement value from six devices. Inset: capacitance-voltage (*C-V*) characteristics for all splits. Basically all *C-V* curves are identical, indicating the transconductance increase is not caused by the oxide thickness difference among all splits.

capping is removed, the enhancement diminishes. These observations demonstrate the following. (1) The transconductance enhancement is indeed due to the uniaxial tensile strain by SiN capping which increases with decreasing channel length. (2) The insertion of 10-nm-thick poly-Si between the gate and the SiN capping does not compromise such performance enhancement. These electrical results are consistent with the film stress measurements. The inset in Fig. 1 shows the capacitance-voltage (*C-V*) characteristics for all samples. Basically all *C-V* curves are identical, indicating that the above observations are not caused by the oxide thickness difference among all splits.

Next we shift our attention to the hot-carrier characterization and study the effectiveness of using poly-Si buffer layer in improving the hot-carrier resistance. Figure 2 shows the substrate current (I_{sub}) versus gate voltage for all splits of devices. It can be seen that the substrate currents of the SiN-capped samples and the BL-POLY samples depict similar trends, and both are larger than that of the control counterparts. When SiN is removed, the substrate current becomes comparable to that of the control devices. These results indicate that the channel strain plays an important role in affecting the generation of channel hot electrons and the associated impact ionization process. In addition, a thin poly-Si buffer layer of 10 nm does not seem to release the stress induced by the SiN capping because of the similar maximum substrate current ($I_{sub,max}$), and is consistent with the inference deduced from Fig. 1. Origins for the increase in substrate current for the strained samples are ascribed to the band gap

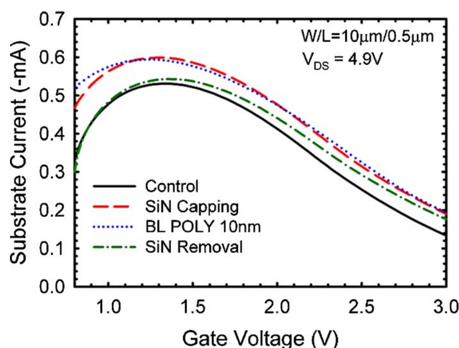

FIG. 2. (Color online) Substrate current vs gate voltage for different splits with channel width/length of 10/0.5 μm.

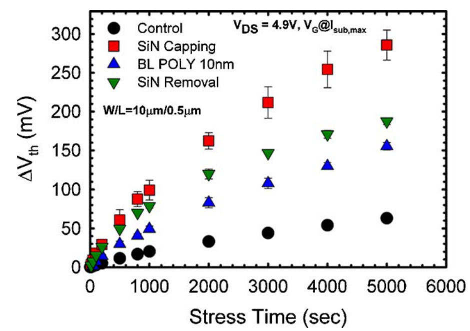

FIG. 3. (Color online) V_{th} shift as a function of stress time. Devices with channel width/length of 10/0.5 μm were stressed at V_{DS}=4.9 V, and V_G of maximum substrate current. Each datum point represents the mean measurement value from three devices.

narrowing effect induced by the channel strain as well as the increased mobility, both tend to enhance the impact ionization rate.[10,11]

Hot-carrier stressing for all splits of samples were performed at V_{DS}=4.9 V and V_{GS} at the maximum substrate current. Channel length and width of the test devices are 0.5 and 10 μm, respectively. Figure 3 shows threshold voltage shift as a function of stress time. We can see that the SiN-capped samples depict the worst degradation in terms of the largest threshold voltage shift, while samples with a thin poly-Si buffer layer apparently show improvement in hot-carrier degradation. It is speculated that the increased carrier mobility in strained channel devices and abundant hydrogen contained in SiN capping are the two primary culprits for the aggravated hot-carrier degradation.[11,12] The increased carrier mobility may increase the device substrate current, as evidenced in Fig. 2, leading to higher degradation. On the other hand, the deposited SiN contains a large amount of hydrogen species which may diffuse into the gate oxide and channel region. It is well known that the breaking of Si–H bonds is one of the major origins responsible for the hot-carrier damage,[8,9] the voluminous hydrogen species definitely aggravate the reliability. This is evidenced in the figure as the SiN-removal devices depict much severe degradation than the control and BL-POLY ones, even though the channel strain has been eliminated by the SiN removal. The phenomenon clearly indicates that the SiN deposition process itself may result in the enhanced damage effect in the short-channel devices.

Figure 4(a) shows several possible pathways for hydrogen diffusion in SiN-capped samples, namely, through the gate electrode (path A1) or oxide spacer (path A2) into the gate oxide and channel region, or through the S/D contacts into the Si substrate and diffuse laterally into the channel region (path A3). The results shown in Fig. 3 for SiN-removal samples imply that such diffusion processes occur during the SiN deposition. It has been previously pointed out that the grain boundaries in poly-Si films act as efficient traps for hydrogen,[13,14] explaining the observation that the diffusivity of hydrogen is significantly reduced as compared with that in oxide[13] and in monocrystalline Si.[13,14] This indicates the A1 path is not preferred for hydrogen diffusion. Similarly, samples with the deposition of a poly-Si buffer layer prior to the SiN capping can effectively suppress the diffusion of hydrogen species into these regions from the pathways mentioned above, as shown in Fig. 4(b). As a result, less broken Si–H bonds and thus less generated inter-

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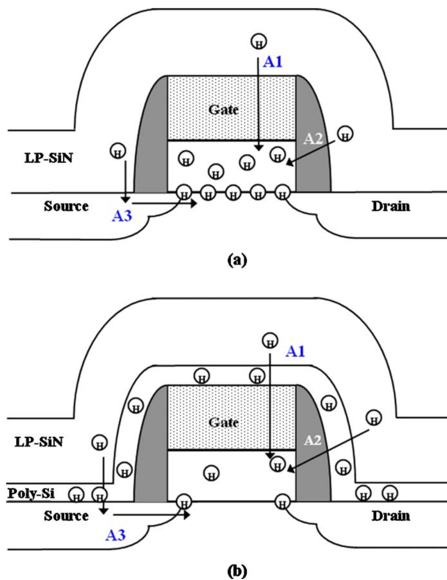

FIG. 4. (Color online) (a) In SiN-capped devices, a large amount of hydrogen species from the SiN layer diffuse to the gate oxide layer and the channel region through three possible pathways denoted as A1, A2, and A3. (b) In BL-POLY devices, the diffusion of hydrogen species from SiN is suppressed by the poly-Si buffer layer.

face state compared with the SiN-capped samples without buffer are observed. As a consequence, BL-POLY samples show better reliability characteristics than SiN-capped ones.

In summary, this work shows convincing evidence that the diffusion of hydrogen during the deposition of SiN layer is mainly responsible for the worsened hot-carrier damage in strained-channel NMOSFETs. Since the grain boundaries in poly-Si can effectively suppress the hydrogen diffusion,[13,14] the use of an ultrathin undoped poly-Si buffer layer prior to the SiN capping can effectively improve hot-carrier reliability of the devices without compromising device performance enhancement.

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