High-Performance Poly-Si Nanowire NMOS Transistors

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***Abstract*—A novel field-effect transistor with Si nanowire (NW) channels is developed and characterized. To enhance the film crystallinity, metal-induced lateral crystallization (MILC) and/or rapid thermal annealing (RTA) techniques are adopted in the fabrication. In the implementation of MILC process, it is shown that the arrangement of seeding window plays an important role in affecting the resulting film structure. In this regard, asymmetric window arrangement, i.e., with the window locating on only one of the two channel sides is preferred. When MILC and RTA techniques are combined, it is found that single-crystal-like NWs are achieved, leading to significant performance improvement as compared with the control with channels made up of fine-grain structures by the conventional solid-phase crystallized (SPC) approach. Field-effect mobility up to 550 $\mathrm{cm}^2/\mathrm{V\text{-}s}$ is recorded in this study.**

***Index Terms*—Field-effect transistor, metal-induced lateral crystallization (MILC), mobility, rapid thermal annealing (RTA), Si nanowire.**

I. Introduction

RECENTLY, Si nanowires (NWs) have drawn much attention due to their great potential in a number of applications. Here, the NW is referred to the stripe structure with its cross-sectional dimensions smaller than 100 nm. For nanoscale CMOS manufacturing, the NW could be employed as the channel and enable the fabrication of nearly or all-around gate configuration to improve the control over the short-channel effects [1]. The NW is also a potential candidate for chemical or biological sensing applications [2], [3]. In this regard, the device operation depends on the modulation of NW conductivity by the amount of charges attached to the surface, which in turn depends on the concentration of detection species in the test solutions. Besides, the NW could also be applied for building high-performance thin-film transistors on glass or plastic substrates [4], light-emitting devices [5], and memory devices [6].

For practical manufacturing and application, precise positioning and alignment of the NW structures on a chip are essential. This could of course be easily achieved using advanced lithography techniques. However, the manufacturing cost is high since expensive tools are involved in the fabrication. To address this issue, we have recently proposed a novel Si NW device [7], [8] with structure similar to that shown in Fig. 1. The device fabrication is simple and does not require costly lithography tools. Thus, it represents a promising approach for fabricating NW devices on a working chip.

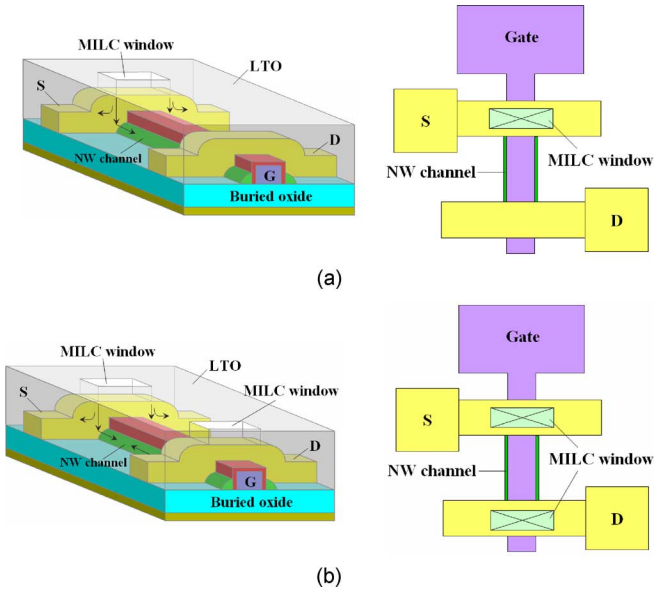

Fig. 1. Top and side views of the MILC devices with: (a) ASW and (b) SSW configuration. Note that NW spacers actually remain on the sidewall of the gate pad and gate-end regions, but are not shown in the top views of the devices for simplicity.

In our previous work, the Si NW is annealed at a low temperature to convert the as-deposited amorphous silicon layer into polycrystalline silicon. The so-called solid-phase crystallization (SPC) technique has been widely used in the fabrication of poly-Si thin-film transistors (TFTs). The device performance, however, is degraded by the large amount of defects contained in the materials, owing to the rather small grain size (i.e., typically, less than 50 nm). To improve the film crystallinity, we have successfully developed an improved process implemented with the metal-induced lateral crystallization (MILC) technique, and the preliminary results are reported in recent publications [9], [10]. In this work, we present the material characterization results to examine the effect of the MILC treatment on the film crystallinity and to understand its impact on the device performance. Special attention is also paid to the effect of seeding window arrangement. In addition, rapid thermal annealing (RTA) is performed on the NWs to further improve the device characteristics. It is found that more than an order of magnitude of improve-

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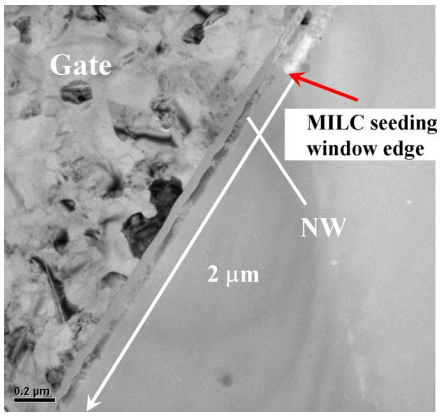

Fig. 2. TEM image of an MILC Si NW.

ment on the filed-effect mobility of electrons relative to the SPC counterpart is achievable when both treatments are combined.

II. Device Structure and Fabrication

The devices featuring Si NW channels, as shown in Fig. 1, were fabricated with similar process sequence as described in our previous work [7], except for the different treatments used for enhancing the film crystallization. Briefly, the fabrication of n-channel devices was started with an n^+-poly-Si gate deposited and patterned on an oxidized Si substrate. Then, a 40 nm-thick TEOS serving as the gate oxide was deposited by a low-pressure chemical vapor deposition (LPCVD) system, followed by the deposition of a 100 nm-thick amorphous Si (a-Si) layer. Afterwards, source/drain (S/D) dopants were implanted with P_{31}^+ ion beam with a dose of 10^{15} cm^{-2} at 15 keV. Subsequently, S/D photoresist patterns were generated using a g-line stepper and the regions were subsequently patterned by an anisotropic dry etching step. During the etching process the NW channels were simultaneously formed on the sidewalls of the gate structure, similar to the formation of sidewall spacers used in standard CMOS manufacturing. Note that the NW channels were accomplished in a self-aligned manner with respect to the S/D and remained undoped because the aforementioned implant was done at a low energy so that the implanted dopants do not reach the channel. A 100 nm-thick low-temperature oxide (LTO) was then deposited by a plasma-enhanced (PE) CVD. For MILC purpose, the seeding windows were opened in the LTO layer. In this work, two splits of samples were exploited, as illustrated in Fig. 1. In one split, denoted as the asymmetric seeding window (ASW) split, as shown in Fig. 1(a), only a single window was opened on the source region. (Here, the source region is defined as the terminal that serves as the grounded source during normal device characterization.) In the other split, two windows symmetrical to the channel center were opened on both the source and drain regions, and denoted as the symmetric seeding window (SSW) split Fig. 1(b). After opening the seeding windows, a 5 nm-thick Ni layer was deposited to serve as the seeding layer. The lateral crystallization was carried out at 550 °C for 16 hr in N_2 ambient. The arrows illustrated in Fig. 1 depict the crystallization paths in the ASW split. The MILC step also serves the dual purpose of dopant activation. Next, the unreacted Ni was disposed off in an H_2SO_4/H_2O_2 solution at 120 °C for 10 min. Afterwards, some samples were treated with an additional rapid-thermal annealing (RTA) step at 900 °C for 30 s to further enhance the crystallinity of poly-Si NWs. This condition was chosen since it was reported that the second grain growth of recrystallization took place at around 800 °C for MILC poly-Si [11]. After depositing a 200 nm passivation oxide layer and opening contact holes, a standard metallization step was performed to complete the device fabrication. It is evident that the overall process flow is quite simple and straightforward. On the other hand, control samples with SPC channels crystallized at 600 °C for 24 hr were also fabricated as a reference for comparison.

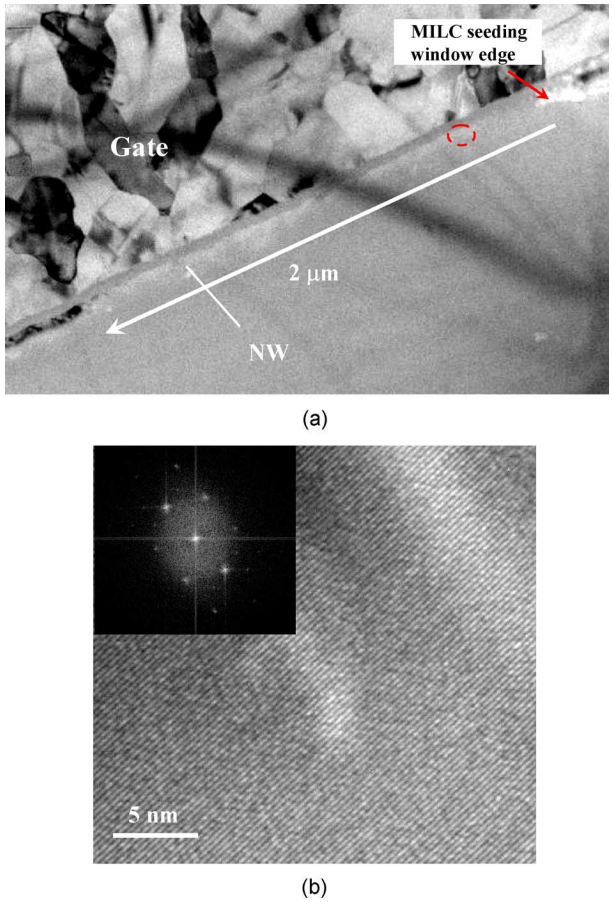

Fig. 3. (a) TEM image of an MILC Si NW received with RTA treatment. (b) A high-resolution view of the NW channel [the circled region in (a)] and the associated diffraction pattern.

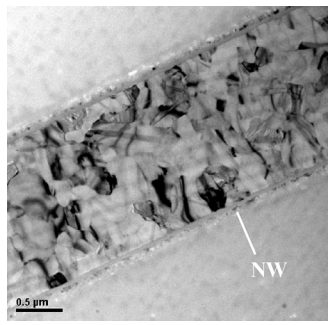

Fig. 4. TEM image of an SPC Si NW after receiving with RTA treatment.

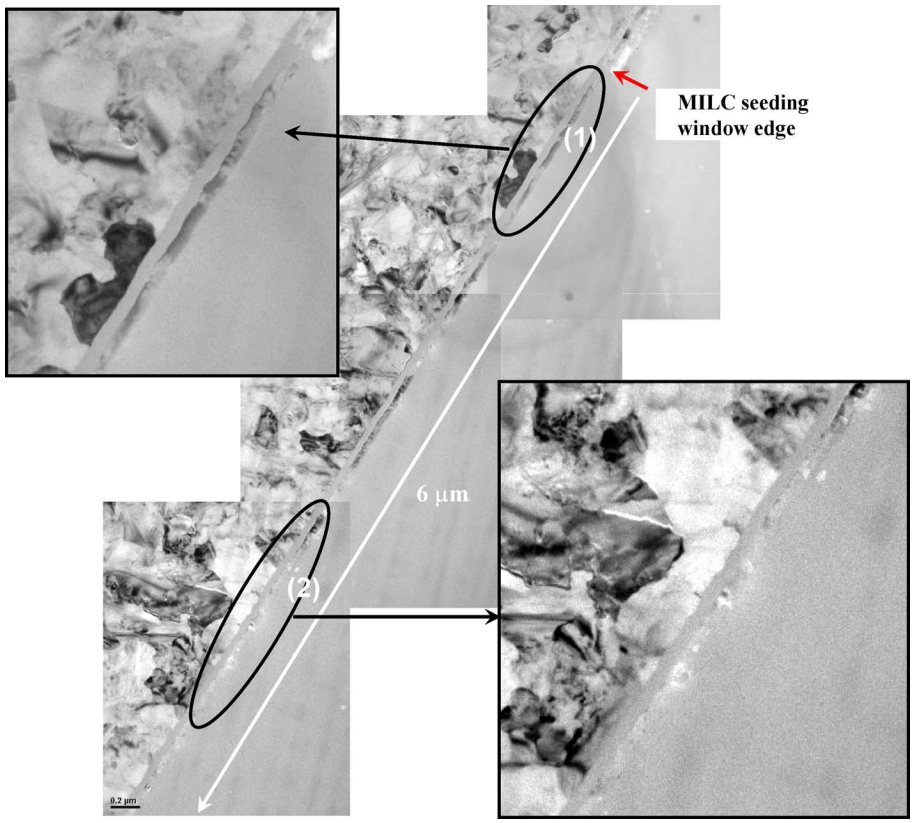

Fig. 5. An overview on the crystallization region of an MILC Si NW. The inset pictures are enlarged view of region 1 (close to the seeding window) and region 2 (about 5 μm away from the seeding window) in the characterization region. Due to the distance effect, SPC mechanism also proceeds in region 2 and leads to a smaller grain structure as compared with region 1.

III. Material Characterization

It is well known that needle-like grains formed by MILC are large in length and the "needle" direction could be deliberately arranged to be parallel to the channel direction [12]. Once the NW feature size is shrunk to less than the lateral size of the needle grain, it becomes feasible to achieve a single-crystal NW structure. In this work, we characterized the crystallinity of the NWs with transmission electron microscopy (TEM) technique performed on test bar structures. Fig. 2 shows the plane-view TEM image of an NW channel abutting the poly-Si gate and the seeding window after the MILC process. As shown in the picture, the MILC NW shows a "bamboo" structure. In contrast to the fine-grain structure of the SPC NW, the film crystallinity of the MILC sample is dramatically improved and the length of the grains could be of several tens of nanometers.

To further enlarge the grain size and eliminate defects like stacking faults and microtwins in the MILC films, it is necessary to perform post-annealing treatment. Previously, excimer laser annealing (ELA) [13], [14], and high-temperature annealing [15] have been proposed for this purpose. In this study, some samples received an additional RTA step at 900 °C for 30 s. The TEM picture of a RTA-treated sample is shown in Fig. 3. It can be seen that the crystallinity of the annealed NW is significantly improved and a monocrystalline structure is achieved. The length of a single grain is about 2 μm in this region. Diffraction pattern obtained by performing the fast Fourier transform (FFT) technique on the HRTEM image Fig. 3(b) indicates that the single-crystal Si exhibits $\langle 110 \rangle$ orientation. For comparison, the TEM image of a SPC poly-Si NWs that also received the RTA treatment is shown in Fig. 4. The image reveals that the SPC poly-Si contains a number of microstructural defects, while the crystalline orientation of the grains is random.

Film crystallinity of the NW is also expected to show dependence on the distance from the MILC seeding window. To confirm this point, the TEM images taken at different locations in the NWs are presented in Figs. 5 and 6 for the MILC samples without and with RTA, respectively. Fig. 5 shows the overview of the characterization region. The results show that the crystalline quality is poorer in the area located about 5 μm away from the seeding window (region 2) than in the area near the window (region1). The trend that the grain size becomes smaller as the region is farther from the window is reasonable, since the grain growth due to heterogeneous nucleation of SPC process are apt to compete with MILC grain growth. Such mechanism needs a period to trigger and, thus, is not important as the crystallization region is near the seeding window.

The MILC NW with RTA also possesses this feature, as shown in Fig. 6. However, it should be noted the crystallinity is much improved than that without RTA (Fig. 5), especially for the region closer to the seeding window. From the TEM results, we conclude that the combination of MILC and RTA treatments together with suitable control over the NW length from the seeding window (say, < 5 μm in the present process conditions), single-crystal NW structure could be obtained and excellent device performance is achievable.

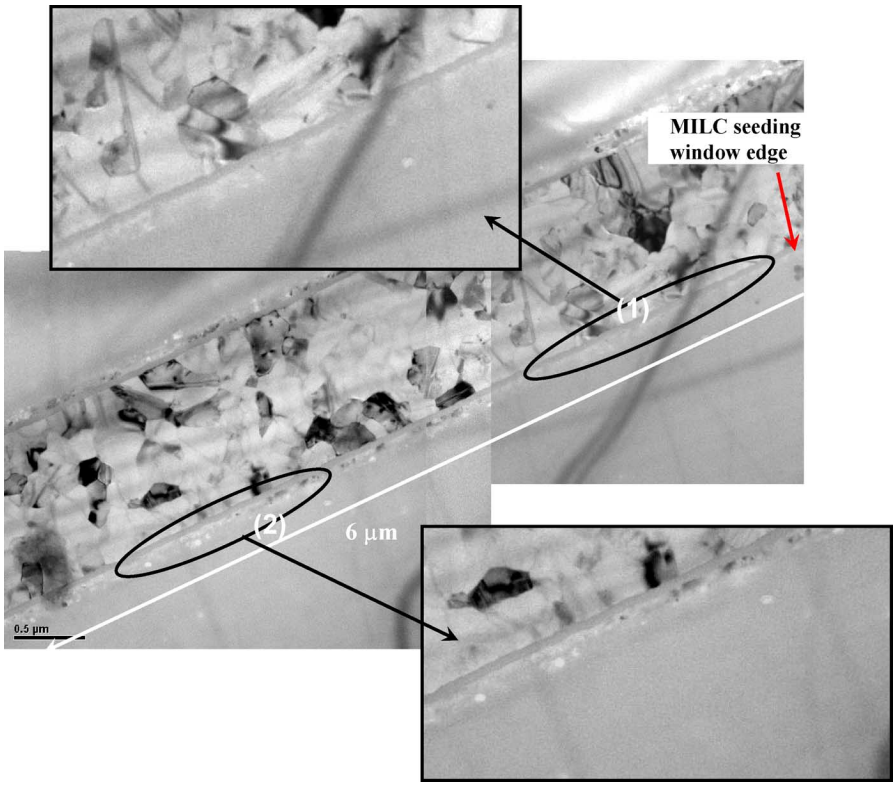

Fig. 6. An overview on the crystallization region of an MILC Si NW received with RTA treatments. The inset pictures are enlarged view of regions 1 and 2 in the characterization region. Note that the grain structure in region 2 is not significantly affected by the RTA treatment.

IV. Electrical Characteristics of the Fabricated Devices

A. Effect of Seeding Window Arrangement

Fig. 7 compares the subthreshold and output characteristics between MILC and SPC splits. As shown in the figures, the two MILC splits show much improved characteristics in terms of higher drive current and carrier mobility, as well as reduced threshold voltage and subthreshold slopes as compared with the SPC device. This confirms the effectiveness of this technique in improving the film crystallinity. The extracted performance parameters are summarized in Table I. The mobility values are 252 and 169 $\mathrm{cm}^2/\mathrm{V\text{-}s}$ for ASW and SSW samples, respectively. The improvement is more significant for the ASW configuration. This trend is consistent with that reported in the previous work [16] and the TEM results presented in previous section. Note that in the MILC process, the crystallization proceeds radially from the seeding window. In the symmetric case, the fronts of crystallization from the opposite sides confront each other at the central region of the channel. Trace amount of metallic species may be left inside the channel and lead to the degraded on-state performance as compared with the asymmetric case.

In the aspect of off-state leakage, however, the results indicate that it is not effectively suppressed when MILC is implemented. The situation becomes even worse when SSW is implemented. In one of our previous studies, we have identified that the magnitude of leakage current is closely related to the dimension of the top gate-to-drain overlap region [8]. When drain voltage is high, the strong electric field together with the defects at grain boundaries triggers the anomalously high leakage current. In the MILC sample with SSW configuration, one of the seeding windows is located in the drain region, and it is expected that a considerable amount of metallic species remain within the window. In line with the analysis in the previous report [8], it is believed that those defect sites are responsible for the excess leakage current. In the ASW case, the window is opened only on the source side in which the electric field strength is low during operation. The ASW sample thus depicts much lower off-sate leakage than the SSW one. This also implies that the characteristics of the devices with ASW configuration depend on the electrodes where source and drain biases are assigned. This issue will be addressed later.

B. Impacts of RTA on Device Performance

Next, we examine the effect of RTA. Results for the three splits of samples are shown in Fig. 8 and Table II. In the SPC sample, although the characteristics improve after the RTA treatment, the mobility value (80 $\mathrm{cm}^2/\mathrm{V\text{-}s}$) is still far behind that of MILC samples either with or without RTA treatment. This indicates that the fine-grain structure of the channels set a limit for the performance improvement eventually.

On the other hand, the RTA treatment could further promote the device characteristics of the MILC devices. For the ASW sample, mobility up to 550 $\mathrm{cm}^2/\mathrm{V\text{-}s}$ is recorded. This value is among the best results reported in the literature [15], [17]. It is suspected that the RTA treatment help remove the weak or strained bonds contained in the grains and lead to a better film crystallinity, and is evidenced by the enhanced contrast of the diffraction patterns mentioned above. Also noted is the reduction of parasitic source/drain resistance due to the

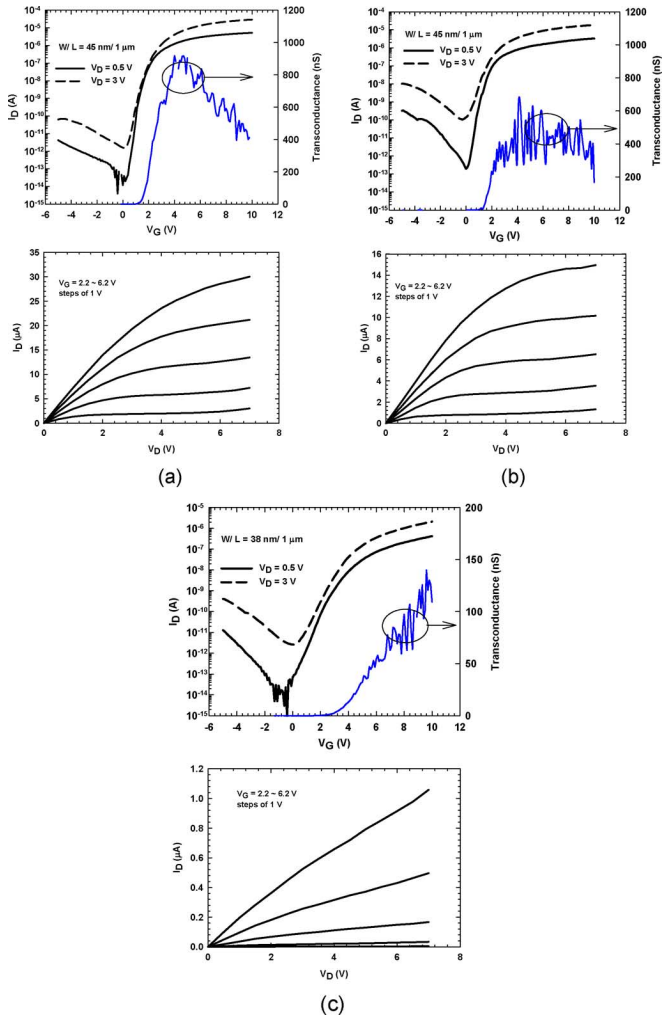

Fig. 7. Transfer and output characteristics of MILC devices with: (a) ASW configuration, (b) SSW configuration, and (c) a SPC device.

TABLE I
COMPARISON OF THE DEVICE PARAMETERS FOR SPC, ASW MILC, AND SSW MILC TFTS

	SPC	ASW MILC	SSW MILC
V_{th} (V)	4.12	1.62	1.50
S.S. (V/dec)	0.86	0.29	0.40
Mobility (cm^2/V-s)	41	252	169
ON/OFF ratio	7.95×10^5	1.89×10^7	1.81×10^5

All parameters were extracted at $V_D = 0.5$ V except for the off-state current, I_{off}, and ON/OFF ratio, I_{on}/I_{off}, which were extracted at $V_D = 3$ V.

activation of dopants by RTA which is also beneficial for device characteristics. For the MILC samples, the sheet resistance of the S/D doping regions is found to reduce from 360 Ω^2 to 250 Ω^2 after RTA. Series resistance of the fabricated devices is extracted based on a method reported previously [18]. Typical values for MILC devices are around 7×10^4 Ω, and reduce to around 2×10^4 Ω after RTA. Note the mobility data shown in Table II are extracted from the maximum transconductance at $V_D = 0.5$ V without considering the effect of series resistance. When the series resistance is taken into account,

TABLE II
COMPARISON OF THE DEVICE PARAMETERS FOR SPC, ASW MILC, AND SSW MILC TFTS AFTER RTA TREATMENT

	SPC(RTA)	ASW (RTA)	SSW (RTA)
V_{th} (V)	2.35	0.03	0.44
S.S.(V/dec)	0.60	0.16	0.19
Mobility (cm^2/V-s)	82	550	313
ON/OFF ratio	1.52×10^6	5.29×10^7	1.87×10^7

All parameters were extracted at $V_D = 0.5$ V except for the off-state current, I_{off}, and ON/OFF ratio, I_{on}/I_{off}, which were extracted at $V_D = 3$ V.

the intrinsic mobility can be obtained, and the values are 324 and 591 $cm^2/V\text{-}s$ for MILC devices without and with RTA, respectively. Impact of RTA on the mobility enhancement is still significant.

The off-state leakage is also suppressed for the SSW split, as shown in Fig. 8(b). These findings are consistent with the TEM characterization results presented in the previous section. In Fig. 8(a), it is seen that the off-state leakage does not seem to be dramatically affected by the RTA treatment. We have checked the fabricated devices about this phenomenon and found that the impact of RTA on the OFF leakage current of the ASW devices is actually similar to that of SPC sample shown in Fig. 8(c). Based on this finding, we suggest that the drain region of the ASW samples is crystallized mainly via the SPC process. This is reasonable since the drain region is away from and separated by the NW channel. The SPC regions are with fine grains, while the grain size is not dramatically affected by the RTA treatment. Detailed mechanism about the leakage mechanism is addressed in another publication [8].

C. Forward and Reverse Modes of Operation in ASW Devices

For the ASW devices, it is interesting to investigate the impact of reversing the S/D assignment during operation on the device characteristics. The results are illustrated in Fig. 9(a) and (b) for devices without and with RTA treatment, respectively. Here, the "forward mode" means the drain bias is applied to the electrode having no seeding window [i.e., the same situation as in Figs. 7(a) and 8(a)], while the other electrode with seeding window is grounded and serves as the source electrode. For "reverse mode" of operation, the source and drain electrodes are simply exchanged. Obviously, the change of operation modes may result in a different outcome. As shown in Fig. 9(a), the reverse mode of operation draws a high off-state and sub-threshold leakage. The excessive defects originating from the seeding window located at the gate-to-drain overlap region are responsible for the leakage. Residual Ni contamination is mainly responsible for this phenomenon [16], [19]. Also noted is the large fluctuation of such a leakage [19], explaining why the leakage shown in Fig. 9(a) under reverse-mode operation is even higher than that shown in Fig. 7(b) for the SSW device. Such asymmetry in device characteristics is greatly diminished as the RTA is applied, as shown in Fig. 9(b). After the RTA, the grains are enlarged and most of the defects are eliminated or driven away from the region that the leakage takes place.

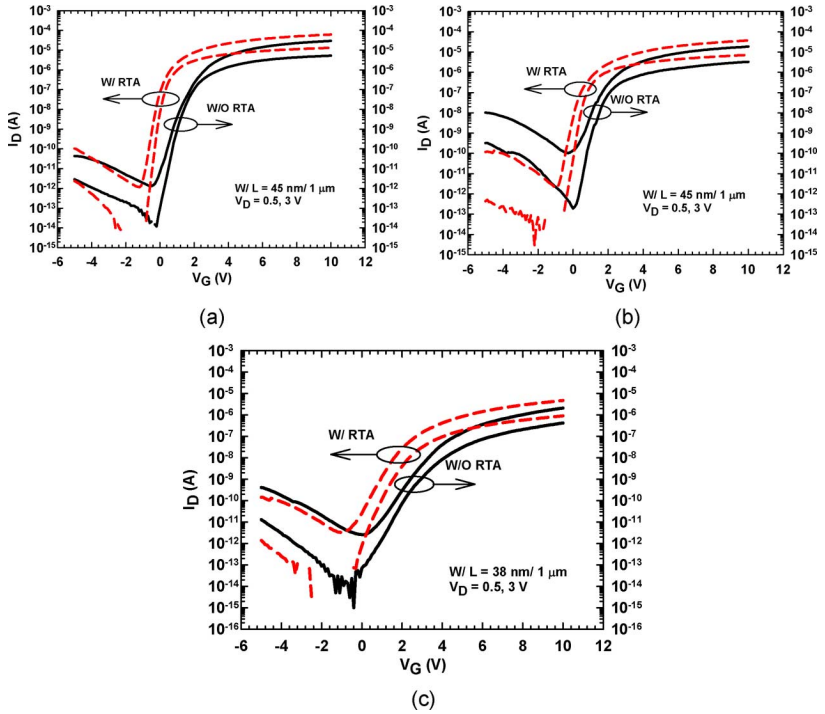

Fig. 8. Transfer and output characteristics of MILC devices with (a) ASW configuration, (b) SSW configuration, and (c) a SPC device with and without RTA treatment.

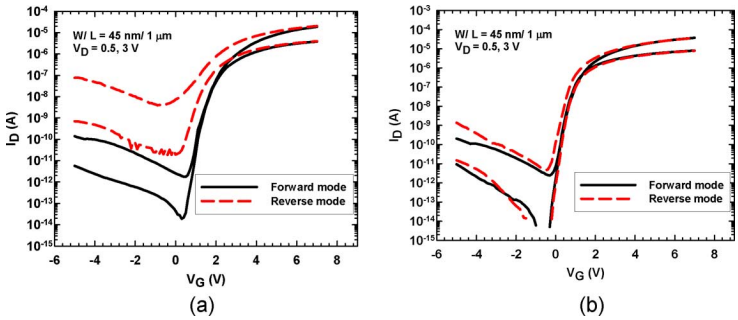

Fig. 9. Transfer characteristics of ASW MILC devices: (a) without and (b) with RTA treatment under forward and reverse modes of operation.

V. Conclusion

In this work, we have successfully implemented the MILC process to enhance the film crystallinity of Si NW channels in a novel NW FET device. With such a scheme, significant improvement in device performance is achieved. The TEM analysis indicates that "bamboo" structure is formed in the NW near the seeding window. Combined with an additional RTA treatment, the single-crystal NW structure becomes feasible. In the region of NW farther away from the seeding window, the SPC mechanism may compete with the MILC during crystallization process, and leads to poorer film crystallinity.

The performance of the fabricated devices is dramatically improved as compared with the counterparts implemented with SPC scheme. We also found that the seeding widow arrangement is important in affecting the film quality and the resultant device performance. In this regard, ASW configuration is demonstrated to be a better choice. The device characteristics could be further improved with an additional RTA step. Together with the asymmetric seeding window configuration, effective electron mobility up to 550 $\mathrm{cm}^2/\mathrm{V}\text{-s}$ could be achieved.

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References

[1] F. L. Yang *et al.*, "5 nm-gate nanowire finFET," in *Proc. Symp. VLSI Tech. Dig.*, 2004, pp. 196–197.

[2] Y. Cui, Q. Wei, H. Park, and C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science*, vol. 293, pp. 1289–1292, 2001.

[3] Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka, and R. S. Williams, "Sequence-specific label-free DNA sensors based on silicon nanowires," *Nano Lett.*, vol. 4, pp. 245–247, 2004.

[4] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, and J. L. Goldma, "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *Nature*, vol. 425, pp. 274–278, 2003.
[5] X. Duan, Y. Huang, Y. Cui, J. Wang, and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature*, vol. 409, pp. 66–69, 2001.
[6] X. Duan, Y. Huang, and C. M. Lieber, "Nonvolatile memory and programmable logic from molecule-gated nanowires," *Nano Lett.*, vol. 2, no. 5, pp. 487–490, 2002.
[7] H. C. Lin, M. H. Lee, C. J. Su, T. Y. Huang, C. C. Lee, and Y. S. Yang, "A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel," *IEEE Electron Device Lett.*, vol. 26, pp. 643–645, Sep. 2005.
[8] H. C. Lin, M. H. Lee, C. J. Su, and S. W. Shen, "Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels," *IEEE Trans. Electron Devices*, vol. 53, pp. 2471–2477, Oct. 2006.
[9] C. J. Su, H. C. Lin, and T. Y. Huang, "High performance TFTs with Si nanowire channels enhanced by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 27, pp. 582–584, Jul. 2006.
[10] C.-J. Su, H.-C. Lin, M.-H. Lee, H.-H. Tsai, R. C.-T. Lin, S.-W. Shen, C.-C. Lee, T.-Y. Huang, and Y.-S. Yang, "Effects of seeding window arrangement on the performance of Si nanowire transistors with MILC channels," in *Reported in the 2006 Si Nanotechnology*, Honolulu, HI, Jun. 11–12, 2006.
[11] G. Liu and S. J. Fonash, "Polycrystalline silicon thin film transistors on Corning 7059 glass substrates using short time, low-temperature processing," *Appl. Phys. Lett.*, vol. 62, pp. 2554–2556, May 1993.
[12] S. Jagar, H. Wang, and M. Chan, "Effects of longitudinal and latitudinal grain boundaries on the performance of large-grain polysilicon MOSFET," *IEEE Electron Device Lett.*, vol. 22, May 2001.
[13] D. Murley, N. Young, M. Trainor, and D. McCulloch, "An investigation of laser annealed and metal-induced crystallized polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 48, pp. 1145–1151, Jun. 2001.
[14] G. Hu, Y. S. Wu, C. Chao, and H. Shih, "Growth mechanism of laser annealing of nickel-induced lateral crystallized silicon films," *Jpn. J. Appl. Phys.*, vol. 45, pp. 21–27, Jan. 2006.
[15] H. Wang, M. Chan, S. Jagar, Poon, M. C. Vincent, M. Qin, Y. Wang, and P. K. Ko, "Super thin-film transistor with SOI CMOS performance formed by a novel grain enhancement method," *IEEE Trans. Electron Devices*, vol. 47, pp. 1580–1586, Aug. 2000.
[16] M. Wong, Z. Jin, G. A. Bhat, P. C. Wong, and H. S. Kwok, "Characterization of the MIC/MILC interface and its effects on the performance of MILC thin-film transistors," *IEEE Trans. Electron Devices*, vol. 47, pp. 1061–1067, May 2000.
[17] C. Hou and Y. S. Wu, "Comparison of TFTs made by IMPRINT and IMPRINT-ELA methods," *Electrochem. Solid-State Lett.*, vol. 9, pp. H71–H73, May 2006.
[18] K. Terada and H. Muta, "A new method to determine effective MOSFET channel length," *Jpn. J. Appl. Phys.*, vol. 18, pp. 953–959, May 1979.
[19] Z. Meng, M. Wang, and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications," *IEEE Trans. Electron Devices*, vol. 47, pp. 404–409, Feb. 2000.

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