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Investigation of source-follower type analog buffer using low temperature poly-Si TFTs

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Abstract

A new source follower circuit using low-temperature polycrystalline silicon thin film transistors (LTPS-TFTs) as analog buffer for the integrated data driver circuit of active matrix liquid crystal displays (AMLCDs) and active matrix light emitting diodes (AMOLEDs) is proposed and measured. Threshold voltage compensation circuit with two n-type thin film transistors, a capacitor, and four switches structure is used to enhance image quality for the display. The threshold voltage difference of driving TFTs and the unsaturated of output voltage are eliminated in this circuit. An active load is added and a calibration operation is applied to study the effects on the source follower circuit, the transistor operation mode region is also discussed. The proposed circuit is capable of minimizing the variation from both the signal timing and the device characteristics through the simulation and measured results.

Keywords: Source follower; LTPS-TFTs (low-temperature polycrystalline silicon thin film transistors); AMLCDs (active matrix liquid crystal displays); AMOLEDs (active matrix light emitting diodes)

1. Introduction

Low temperature poly-Si (LTPS) TFTs have attracted much attention in the application on the pixel circuits and integrated peripheral circuits of active matrix liquid crystal displays (AMLCDs) and active matrix light emitting diodes (AMOLEDs) [1–18]. In a poly-Si TFT-LCD, poly-Si TFT is not only used to implement pixel circuit but also the driving circuit on a single glass substrate to reduce system cost and possess compact module which a-Si TFT is hard to achieve.

Although LTPS-TFTs have superior electrical characteristics compared with a-Si TFTs, the inevitable non-uniformity issue is encountered because of process variation such as toughly controllable grain size of poly-Si and gate oxide/poly-Si varied interface trap density.

Among the many data driving circuits employing LTPS TFTs, the output buffer is indispensable to drive the large load capacitance of the data bus. There are several requirements for the output buffer for a flat panel display data driver [9]. For instance, as resolution getting higher and higher, more analog buffers are needed. Therefore, its layout area must be reduced as possible to fit the pitch size. In addition, displays toward portable applications so that power dissipation must be minimized to extend the battery lifetime. However, comparing to the MOSFETs, the LTPS

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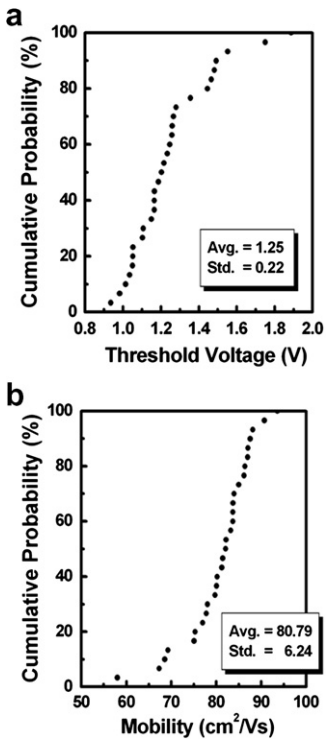

Fig. 1. Thirty low-temperature poly-Si transistors of (a) threshold voltage variation, and (b) field-effect mobility variation.

TFTs suffer from poor electrical characteristics and huge device-to-device variations mainly due to the non-uniform grain structure and grain size across the whole glass substrate. Fig. 1a shows the threshold voltage variation of thirty poly-Si transistors fabricated in the factory and Fig. 1b shows the field-effect mobility variation. It is obvious that even though in the factory, the LTPS TFTs still have 1 V threshold voltage maximum difference and 36 cm^2/v s field-effect mobility maximum differences. Since thousands of output buffers are necessary for a poly-Si TFT-LCD, it is very essential to develop novel analog buffers dealing with the device non-uniformity. Electrical characteristic variations of LTPS-TFTs will cause the real output voltage not the target value and lead to the wrong image data through the analog buffer which leads poor image quality. Therefore, compensation circuit is essential for highly integrated panel. The output deviation depends on product specification must be decreased as possible conforming to high degree of matching among the data lines.

Among output buffer circuits for displays, source follower is considered an excellent candidate for the output buffer circuit for the "System on Panel" application because of its simple schematic and low power dissipation [10–18].

2. Proposed analog buffer and its driving schemes

We have proposed a new type analog buffer for the compensation of the device variation and signal timing before

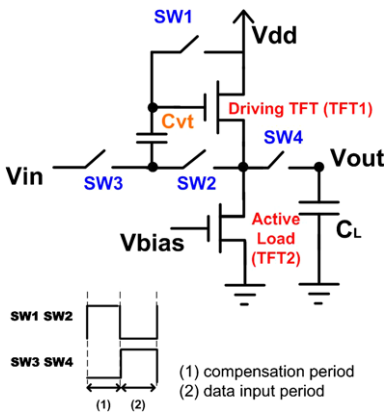

Fig. 2. The proposed analog buffer and its timing diagram of signal lines.

[17,18]. Fig. 2 shows a schematic and the timing diagram of the proposed analog buffer which consisting of two n-type thin film transistors, one capacitor, and four switches. The gate voltage of the TFT as the active load is biased at Vbias. The driving schemes are as described follows:

2.1. Compensation period

During first operating period, SW1 and SW2 are turned on, and SW3 and SW4 are turned off. Thereby, a voltage corresponding to the threshold voltage of driving TFT, the threshold voltage of the active load and the bias voltage is stored in Cvt.

2.2. Data input period

After sampling period, SW3 and SW4 are turned on and SW1 and SW2 are turned off, then the voltage at the gate of the driving TFT is hold. Thus, the output voltage is compensated by the voltage stored in Cvt.

In order to investigate the output performance of the proposed analog buffer, HSPICE circuit simulator was introduced. In this work, the typical model of the poly-Si TFTs for simulation is expressed by the PRI parameters. The load capacitance of data line is assumed 20 pF which corresponds to a 2-inch QVGA LCD. Monte Carlo simulation with an assumption of normal distribution is executed to study the effect of the device variation on the circuit performance, where the mean value and the deviation of the threshold voltage and mobility are 1.45 V, 0.5 V and 65.69 cm^2/v s, 15 cm^2/v s, respectively. Table 1 shows the dynamic performance of settling time of the

Table 1
The output settling time of the proposed analog buffer with input voltage 1–5 V

Input voltage V_{in} (V)	1	2	3	4	5
Settling time (μs)	13.08	20.42	27.43	36.34	47.1

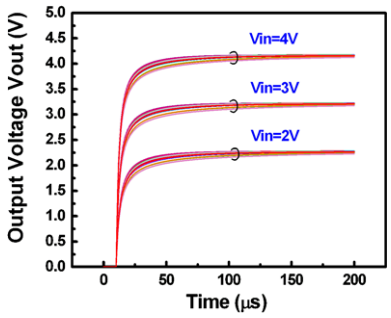

Fig. 3. Twenty times of Monte Carlo simulation results of the proposed analog buffer when input voltages are 2–4 V.

proposed analog buffer as input voltage 1–5 V. Fig. 3 shows the twenty times of Monte Carlo simulation results of the proposed analog buffer when input voltages are 2–4 V. The variations of the driving TFT and the active load are both taken into consideration in the Monte Carlo simulation. The output voltage variation of the proposed analog buffer is about 50 mV, which is much smaller than that of conventional source follower type analog buffer (~550 mV). The output voltage variation decreases drastically.

3. Analog buffer circuit fabrication and measured results

After analog buffer circuit design finished, testing analog buffer circuits were fabricated and measured. The circuit fabrication processes are described as follows. First, a buffer oxide and 500 Å-thick a-Si thin film was deposited on glass substrate. Then, the amorphous Si thin film was crystallized by KrF excimer laser annealing at room temperature. After defining the active layer, a 1000 Å-thick gate oxide was deposited by plasma-enhanced chemical vapor deposition. A 3000 Å-thick Cr film was then deposited for gate electrode. Then, the Cr thin film and gate oxide were etched to form gate electrodes. After N^+ and P^+ ion implantation, a 4000 Å-thick SiNx was deposited by PECVD as interlayer. TFT testing analog buffer circuits were formed after contact-hole formation and 4000 Å-thick Cr metallization. The image of optical micrograph of the proposed analog buffer circuit is shown in Fig. 4. The cross-section of TFTs is inserted in Fig. 4. In the design, the W/L ratio of the driving TFT, the active load and the switching TFTs are 100 μm/8 μm, 8 μm/50 μm and 8 μm/8 μm, respectively.

After probing system ready for measuring, several proposed and conventional analog buffer circuits were measured and gathered statistics. The conventional analog buffer is a simple source follower configuration consists of a driving TFT connected a capacitor in serial. Fig. 5 shows comparison of the offset voltage with various input voltages between the conventional and proposed analog buffers. It is observed that the output voltage of proposed analog buffer is closely equal to the actual input voltage.

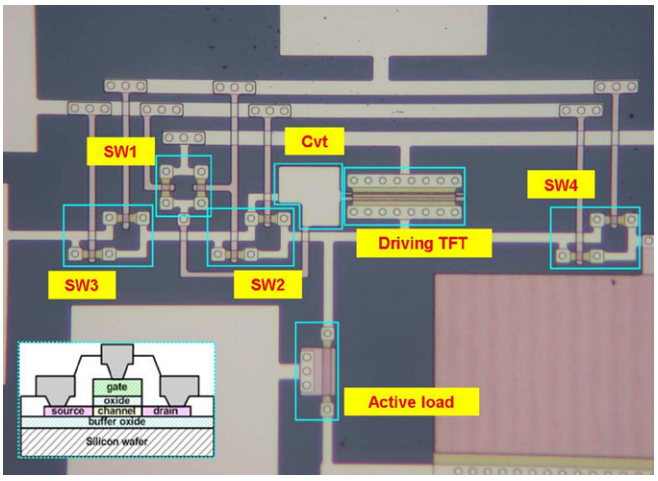

Fig. 4. Optical micrograph of the proposed analog buffer circuit. (Inset): Cross-section view of the driving TFTs.

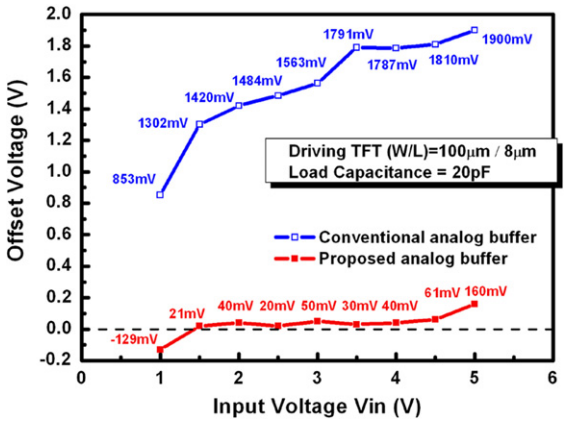

Fig. 5. Comparison of the offset voltage versus input voltage curve of the conventional and proposed analog buffers measured results.

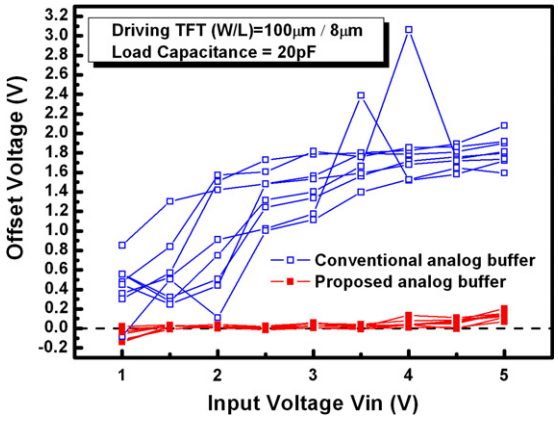

Fig. 6. Offset voltage variation of eight sets of analog buffer circuits are compared between the conventional and proposed analog buffer circuits with different input voltages measured results.

On the other hand, the offset voltage of conventional analog is mostly above 1 V which is large compared with proposed analog buffers. Output deviation of the proposed

analog buffer is controlled under 50 mV regardless of threshold voltage variation showing extremely good results. We also measured five sets data in each source follower circuits shown in Fig. 6. The figure shows that offset voltage of conventional analog buffer suffers huge variations and the proposed analog buffer has small output variability and better uniformity after threshold voltage calibration.

4. Bias voltage effect of active load

In this section, the operation of the driving TFT and the active load will be discussed in detail. During the first operation period, the driving TFT and the active load are both working in the saturation region since the V_{DD} power line compensation. Nevertheless, during the second operation period, the active load operates in linear or saturation region depending on input data voltage while the driving TFT still works in the saturation region. We divide it into two conditions for discussing.

4.1. A. Driving TFT in saturation region, active load in saturation region

These results can be expressed by formula as follows: (We assumed that the driving TFT as TFT1 and the active load as TFT2 here for convenience)

(1) *Compensation period:*

$$\begin{aligned} I_D &= K_1(V_{GS1}-V_{TH1})^2 = K_2(V_{GS2}-V_{TH2})^2 \\ &\rightarrow K_1(V_{DD}-V_{out}-V_{TH1})^2 = K_2(V_{bias}-V_{TH2})^2 \\ &\rightarrow a = \sqrt{K_1/K_2} = \frac{V_{bias}-V_{TH2}}{V_{DD}-V_{out}-V_{TH1}} \\ aV_{DD} &- aV_{out} - aV_{TH1} = V_{bias} - V_{TH2} \\ V_{out} &= V_{DD} - V_{TH1} + \frac{1}{a}V_{TH2} - \frac{1}{a}V_{bias} \\ \therefore Cvt\_storage\_\Delta V &= V_{DD} - V_{out} = V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias}. \end{aligned} \tag{1}$$

(2) *Data input period:*

$$\begin{aligned} I_D &= K_1(V_{in}+\Delta V - V_{out} - V_{TH1})^2 \\ &= K_2(V_{bias}-V_{TH2})^2 \rightarrow a = \sqrt{K_1/K_2} \\ &= \frac{V_{bias}-V_{TH2}}{V_{in}+(V_{TH1}-\frac{1}{a}V_{TH2}+\frac{1}{a}V_{bias})-V_{out}-V_{TH1}} \\ &\rightarrow aV_{in} - V_{TH2} + V_{bias} - aV_{out} = V_{bias} - V_{TH2} \\ &\Rightarrow V_{out} = V_{in} \end{aligned} \tag{2}$$

The Eq. (1) indicates that the variations of driving TFT and the active load both can be stored for the compensation during the operation period. Therefore, the Eq. (2) shows the output voltage equal to the input voltage theoretically.

4.2. B. Driving TFT in saturation region, active load in linear region

(1) *Compensation period:*
During the first operation period, the situation is the same as described previously which the voltage stored in the capacitor depending on the threshold voltage, bias voltage and the K_1/K_2 ratio.

(2) *Data input period:*

$$\begin{aligned} I_D &= K_1(V_{in}+\Delta V - V_{out} - V_{TH1})^2 \\ &= K_2[(V_{bias}-V_{TH2})V_{out} - \frac{1}{2}V_{out}^2] \\ &\rightarrow a^2[V_{in}+\Delta V - V_{out} - V_{TH1}]^2 \\ &= (V_{bias}-V_{TH2})V_{out} - \frac{1}{2}V_{out}^2 \end{aligned}$$

from Eq. (1):

$$\Delta V = V_{DD} - V_{out} = V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias} \rightarrow a^2\left[V_{in} + \left(V_{TH1} - \frac{1}{a}V_{TH2} + \frac{1}{a}V_{bias}\right) - V_{out} - V_{TH1}\right]^2$$

$$= (V_{bias}-V_{TH2})V_{out} - \frac{1}{2}V_{out}^2 \Rightarrow V_{out} = \underbrace{\frac{2(V_{bias}-V_{TH2}) + 4a(V_{bias}-V_{TH2}) + 4a^2V_{in}}{2(1+2a^2)}}_{A}$$

$$+ \underbrace{\frac{\sqrt{[(4a+2)(V_{bias}-V_{TH2}) + 4aV_{in}]^2 - 4(2a^2+1)[2(V_b^2+V_t^2)] + 4aV_{in}(V_{bias}-V_{TH2}) + 2a^2V_{in}^2 - 4V_{bias}V_{TH2}}}{2(2a^2+1)}}_{B}$$

We assume that $2a^2 \gg 1$, $4a \gg 2$

(A) term can be simplified to $V_{in} + \frac{(V_{bias}-V_{TH2})}{a} + \frac{(V_{bias}-V_{TH2})}{2a^2}$

(B) term:

$$\frac{\sqrt{[(4a+2)(V_{bias}-V_{TH2})+4aV_{in}]^2-4(2a^2+1)[2(V_b^2+V_t^2)]+4aV_{in}(V_{bias}-V_{TH2})+2a^2V_{in}^2-4V_{bias}V_{TH2}}}{2(2a^2+1)}$$

$$\approx \frac{\sqrt{[(4a)(V_{bias}-V_{TH2})+4aV_{in}]^2-4(2a^2)[2(V_b^2+V_t^2)]+4aV_{in}(V_{bias}-V_{TH2})+2a^2V_{in}^2-4V_{bias}V_{TH2}}}{4a^2}$$

$$\rightarrow \frac{\sqrt{0}}{4a^2}$$

Therefore, the output voltage can be simplified as

$$V_{out} = V_{in} + \frac{(V_{bias}-V_{TH2})}{a} + \frac{(V_{bias}-V_{TH2})}{2a^2}, \quad (3)$$

where $a^2 = K_1/K_2$.

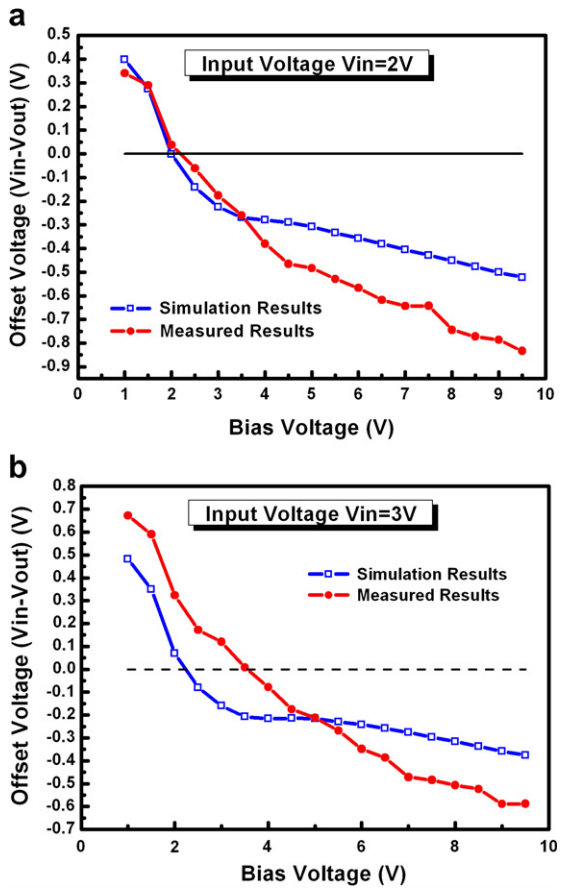

Fig. 7. (a) Comparison of the offset voltage versus bias voltage curve of the simulation and measured results when input voltage 2 V. (b) Comparison of the offset voltage versus bias voltage curve of the simulation and measured results when input voltage 3 V.

According to the Eq. (3) proved, the output voltage will be larger than the input voltage because that the bias voltage must be higher than the threshold voltage of the active load to turn on the active load. Therefore, we know that if the active load works in the linear region at the data input period, the output voltage will exceed the input data and thus a negative offset voltage is obtained. This situation will happen when the bias voltage is higher than the input voltage. Furthermore, from the Eq. (3), we know that the output voltage almost equal to the input voltage when the factor a large in design theoretically. The mobility of the driving TFT and the active load are assumed equal. Therefore, the driving TFT is designed larger W/L ratio and the active load is designed smaller W/L ratio to possess large factor a. The larger factor a, the output voltage is more accurate.

Fig. 7a shows the comparison of the offset voltage versus bias voltage curve of the simulation and measured results when input voltage 2 V. It is shown that the offset voltage has optimum value around 2 V which the active load just nearly turns on and leads to the saturation region. The simulation and measured results of input voltage 3 V also shown in Fig. 7b. It is observed that the measured result trend is close to the simulation results. The larger bias voltage is the larger offset voltage is. Proper design of the bias voltage is required to achieve total performance.

5. Summary and conclusions

A novel source follower type analog buffer have been presented and measured, where the driving circuit is formed by only two n-type thin film transistors, one capacitor, and four switches. The large mismatch of LTPS-TFTs in threshold voltage is compensated and output voltage come very close to the actual input voltage. Much improved output voltage stability and simple configuration are achieved by adding the bias circuit and the compensation operation. The operation of the driving TFT and the active load related to bias voltage are also discussed in detail. Through the simulation and measured results, the proposed source follower type analog buffer is capable of minimizing the variations from signal timing and the device varied characteristics. Proper design of the bias voltage

applied to the active load is required to achieve excellent performance.

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