is close to about 1.2 ($\Delta r_1/\Delta r_2$), the best CP operation can be obtained. Axial ratio is 0.68 dB at 2540 MHz centered. The measured axial ratio and gain for the proposed antenna are shown in Figure 3 and the design dimensions and CP performance are also summarized in Table 1.

4. CONCLUSION

A design of circularly polarized microstrip antenna with asymmetric ring-sector two-pair slots embedded on the ground plane for increasing antenna gain is presented. The embedded ring-sector slots on the ground plane can increase the radiation efficiency by decreasing quality factor of proposed antenna. Also, the CP performance can be easily adjusted by selecting proper slot length ratio of the asymmetric ring-sector slots. The measured peak gains of the proposed antenna and the reference antenna are 5.0 and 2.2 dBi, respectively. The radiation patterns of proposed antenna measured at 2540 MHz are plotted in Figure 4 and the broadside radiation patterns with good axial ratio are found at the two orthogonal planes.

REFERENCES

1. J.R. James, P.S. Hall, and C. Wood, Microstrip antenna theory and design, vol. 1, Peter Peregrinus, London, 1981.
2. J.R. Row and C.Y. Ai, Compact design of single-feed circularly polarized microstrip antenna, Electron Lett 40 (2004), 1093–1094.
3. J.S. Row and K.W. Lin, Design of an annular-ring microstrip antenna for circular polarization, Microwave Opt Technol Lett 37 (2001), 934–936.
4. E. Nishiyama, M. Aikawa, and S. Egashira, Stacked microstrip antenna for wideband and high gain, IEE Proc Microwave Antennas Propagat 151 (2004), 143–148.
5. T.H. Liu, W.X. Zhang, M. Zhang, and K.F. Tsang, Low profile spiral antenna with PBG substrate, Electron Lett 36 (2000), 779–780.
6. J.S. Kuo and G.B. Hsieh, Gain enhancement of a circularly polarized equilateral-triangular microstrip antenna with a slotted ground plane, IEEE Trans Antennas propagat 51 (2003), 1652–1656.

CALIBRATION 90 nm NODE RF MOSFETS, INCLUDING STRESS DEGRADATION

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ABSTRACT: *Using a microstrip line layout, a low minimum noise figure (NF_{min}) of 0.51 dB, at 10 GHz, was directly measured for 90 nm node NMOSFETs (65 nm physical gate length). The NF_{min} was located at the peak f_T of 152 GHz, coinciding with the peak transconductance (g_m). On the basis of these measurements, a self-consistent model of the DC I-V, S-parameters, and NF_{min} results was developed, including the changes after hot-carrier stress.* © 2007 Wiley Periodicals, Inc. Microwave Opt Technol Lett 49: 604–607, 2007; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop. 22209

1. INTRODUCTION

As silicon technology has evolved, the device performance has improved to the point where Si RF MOSFETs [1–8] are now widely used in wireless communication ICs. RF transistors, when compared with their digital and low frequency analog counterparts, require more accurate device models and supporting measurements. This arises from the tight specifications for impedance matching, low RF noise, and high gain. In addition, the modeling of the RF performance degradation of transistors under continuous operation is vital for RF IC design [8–10]. Here, we have modeled multiple-gate-fingered [5, 6] 90 nm node MOSFETs to obtain self-consistent DC, RF, and NF_{min} parameters, close to the measured data. To obtain accurate as-measured NF_{min}, a microstrip transmission line layout [7, 8] was used to shield the RF noise generated in the lossy Si substrate [5, 6]. We obtained NF_{min} of 0.51 dB at 10 GHz for 90 nm node RF MOSFETs (65 nm physical gate length) without any de-embedding. This is one of the lowest reported NF_{min} in CMOS [1–3], and it is due to the successful shielding of the noise arising from the low resistivity Si substrate. The degradation caused by hot-carrier-induced stress was determined after 5000 s at $V_{gs} = 1.4$ V and $V_{d\,s} = 2.1$ V, and gave a 10% drive current reduction [8–10]. We obtained a good match between the measured and modeled DC I-V, S-parameters, and NF_{min} once the current degradation was included. Our self-consistent model can be used in circuit design as a tool for predicting the performance before and during continuous operation.

2. EXPERIMENTAL PROCEDURES

The multiple-fingered 90 nm node CMOS technology used in this study has a 65 nm physical gate length. We used the multiple 16-gate-finger layout to reduce the gate-resistance-generated thermal noise [5, 6]. To screen out the dominant thermal noise (from the parasitic substrate resistance) of the RF probing pads and the CPW line, the 65 nm devices were designed in a microstrip line layout [7, 8] instead of conventional CPW layout [5, 6]. In this way accurate intrinsic MOSFET NF_{min} measurements can be obtained directly [8]. This also permits an accurate determination of the degradation of NF_{min} following electrical stress. The device char-
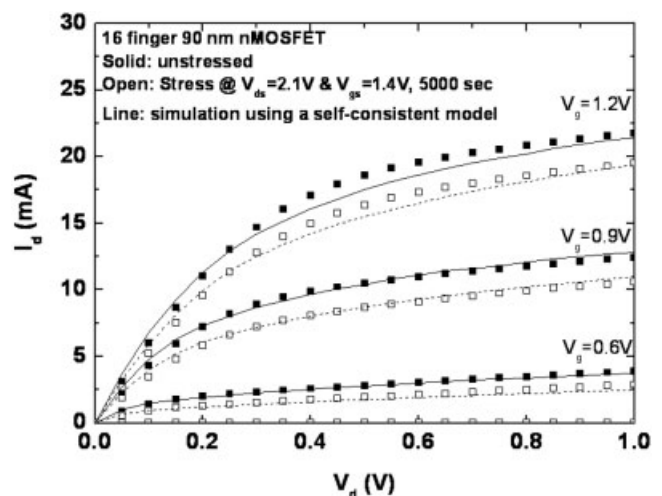

Figure 1 The measured and modeled $I_d - V_d$ characteristics for 16-gate-finger RF MOSFETs, before (solid symbols) and after (open symbols) hot-carrier stress. The lines represent simulation data using a self-consistent model
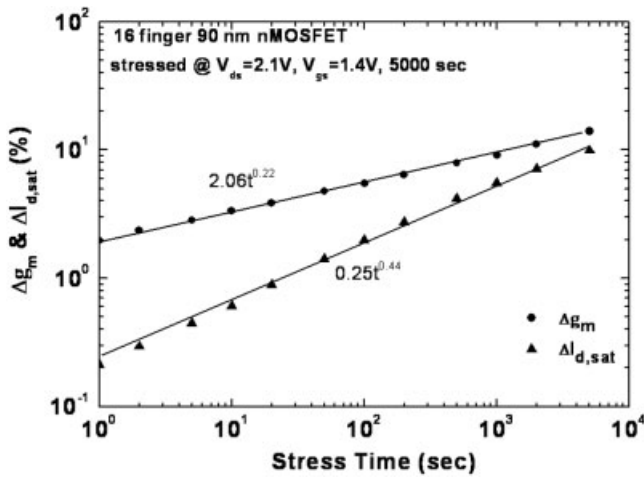
Figure 2 Time dependence of the g_m and $I_{d,sat}$ degradation for 90 nm RF MOSFETs. The degradation rates follow a power law

acteristics were measured by using an HP 4155C for DC *I-V*, an HP 8510C network analyzer for *S*-parameters and ATN-NP5B for noise parameter measurements [5–8]. The devices were stressed electrically at $V_{ds} = 2.1$ V and $V_{gs} = 1.4$ V for 5000 s, and then re-measured. A self-consistent DC to RF model was developed, which had a BSIM core and had parasitic RC elements to the gate, drain, and body to simulate the device characteristics before and after stress.

3. RESULTS AND DISCUSSION

Figure 1 shows the $I_d - V_d$ characteristics for a 16-gate-finger 90 nm NMOSFET, before and after stress. A high drive current of 22.5 mA is observed because of the small gate length and multiple parallel gate fingers. After hot-carrier stress, the saturation drain current $I_{d,sat}$ decreased to 20.4 mA. The drain current decrease is
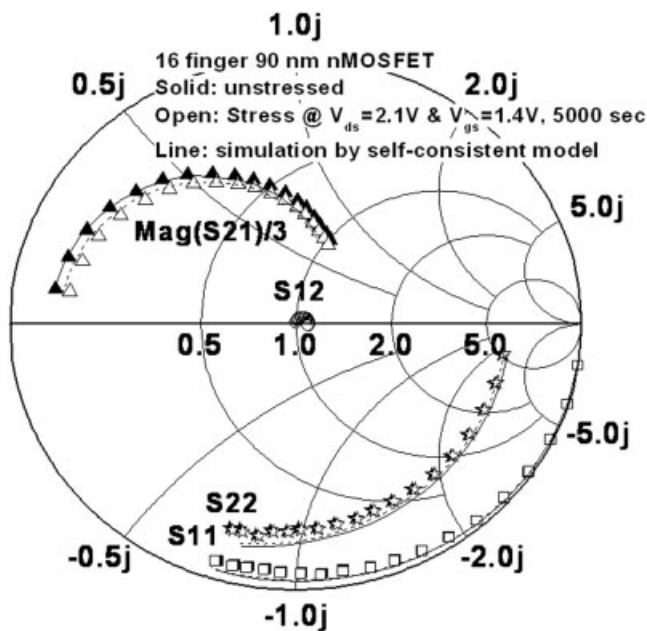

Figure 3 *S*-parameters for 16-gate-fingered 90 nm RF MOSFETs before (solid symbols) and after (open symbols) hot-carrier stress. The lines represent the modeled data

due to interface state (N_{it}) and oxide trap generation at the drain side of the device.

Figure 2 illustrates the time dependence of the transconductance ($g_m = \partial I_d / \partial V_{gs}$) and saturation current ($I_{d,sat}$) for 90 nm node RF MOSFETs, under the hot-carrier stress conditions of $V_{ds} = 2.1$ V and $V_{gs} = 1.4$ V. The above stress conditions gave an accumulated Δg_m of 14% and $\Delta I_{d,sat}$ of 10% after 5000 s. During the stress, both g_m and $I_{d,sat}$ degrade monotonically with increasing stress time and the amount of degradation follows a power law. Such dependence is typical for hot-carrier stress that originates from interface charge generation, and the resulting decrease of the electron mobility. The modeled DC *I-V* characteristics, before and after stress, are also shown in Figure 1.

The effect of the hot-carrier stress is not only important for DC characteristics but it also has a large impact on the RF performance and impedance matching in circuits. The degraded performance (DC to RF) needs to be predicted by device modeling, particularly when the failure criteria is targeted in the range of 10–20% of $\Delta I_{d,sat}$.

Figure 3 depicts the measured and modeled *S*-parameters of 16-gate-fingered 90 nm RF MOSFETs before and after stress. We found that S_{21} and S_{22} displayed more significant changes than S_{11} and S_{12}, after the hot-carrier stress. The effect of the stress on S_{21}
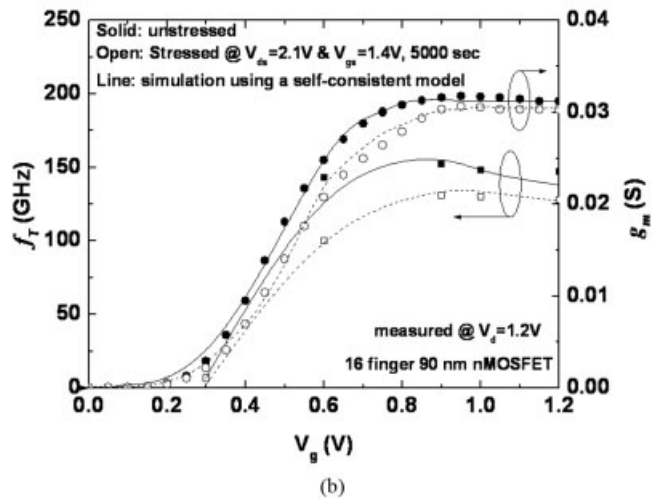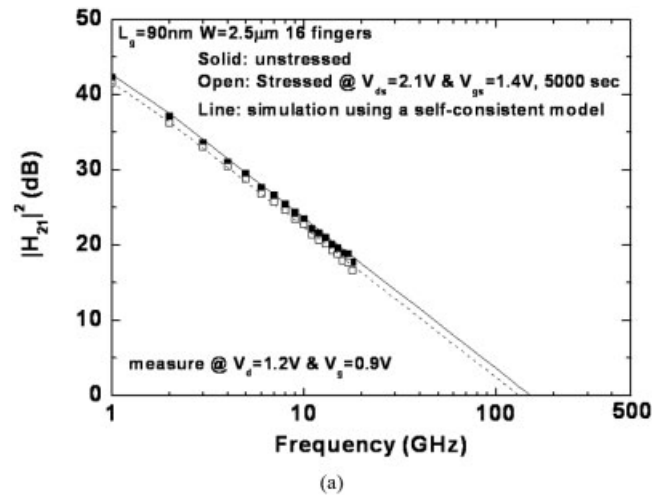

(a)

(b)

Figure 4 Measured and modeled (a) $H_{21}{}^2$ versus frequency and (b) f_T and g_m versus V_g for 16-gate-finger 90 nm MOSFETs before (solid symbols) and after (open symbols) hot-carrier stress. The lines are the modeled data
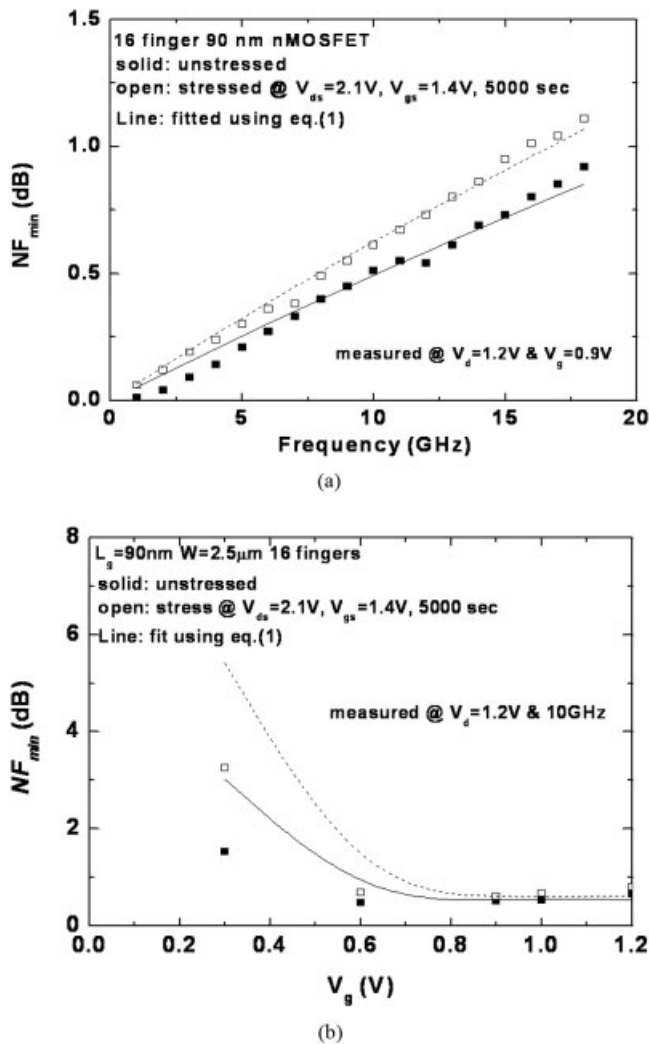
Figure 5 Measured and modeled NF_{min} as function of (a) frequency and (b) gate voltage of 16-gate-fingers 90 nm RF MOSFETs before and after electrical stress. The lines are the modeled data

corresponds to the lower g_m. Again, good matching between measured and device modeled data was obtained.

From the measured S-parameters, the RF current gain H_{21}^2 can be derived as a function of frequency, and this is shown in Figure 4(a). The H_{21}^2 follows the typical −20 dB/decade slope, and the unity gain cut-off frequency (f_T) was obtained by extrapolating H_{21}^2 to 0 dB. The stress lowers the f_T from 152 to 131 GHz. Figure 4(b) illustrates the extrapolated f_T and g_m as a function of V_g, with a fixed $V_{ds} = 1.2$ V. After hot-carrier stress, the f_T curve still follows the g_m curve with the peak f_T being near the peak g_m.

The RF noise is an important parameter for an LNA. To obtain good accuracy, a microstrip transmission line layout was used, which permitted directly the measurement of the intrinsic NF_{min} without any de-embedding of the parasitic pads and substrate loss [9]. Figure 5(a) shows the NF_{min} as a function of frequency. The as-measured NF_{min} was only 0.51 dB at 10 GHz. Figure 5(b) shows the NF_{min} at 10 GHz, $V_d = 1.2$ V, and its variation when sweeping V_g from 0.3 to 1.2 V. The minimum NF_{min} is located at $V_g = 0.9$ V because of the peak f_T in Figure 4(b). This low NF_{min} is located near the peak f_T [Fig. 4(b)]. This is one of the lowest reported NF_{min} for a 90 nm MOSFET [1–3]. The low NF_{min} of

0.51 dB at 10 GHz is sufficient for UWB (3.1–10.6 GHz) applications.

The effect of stress on NF_{min} is also displayed in Figure 5. Stress increased NF_{min} over the whole frequency range up to 18 GHz. At 10 GHz, NF_{min} increased from 0.51 to 0.61 dB in the 16-gate-finger device. The NF_{min} after hot-carrier stress is also dependent on the gate bias. The lowest NF_{min} is located at the peak g_m. This NF_{min} increase needs to be considered and modeled in RF circuit design.

To get an accurate model for NF_{min}, we have used a previously derived analytical equation from the equivalent noise circuit of MOSFETs [7, 8]:

$$NF_{min} \cong 1 + 2\gamma (1 + g_m R_g/\gamma)^{0.5} f/f_T \ (1)$$

Again, close agreement between measured and modeled NF_{min} was obtained for the unstressed and stress devices, as is also shown in Figure 5.

4. CONCLUSION

We have measured and modeled the effects of hot-carrier stress on the DC to RF performance of 16-gate-fingered 90 nm node RF MOSFETs. Close agreement was obtained between the measured and modeled I-V, S-parameters, and NF_{min} data. This approach should be useful in predicting the RF performance degradation of MOSFETs in a circuit when operated under continuous bias.

REFERENCES

1. W. Jeamsaksiri, A. Mercha, J. Ramos, D. Linten, S. Thijs, S. Jenei, C. Detcheverry, P. Wambacq, R. Velghe, and S. Decoutere, Integration of a 90 nm RF CMOS technology (200 GHz f_{max} - 150 GHz f_T NMOS) demonstrated on a 5GHz LNA, Symp VLSI Tech (2004), 100–101.

2. W. Jeamsaksiri, D. Linten, S. Thijs, G. Carchon, J. Ramos, A. Merch, X. Sun, P. Soussan, M. Deha, T. Chiarella, R. Vengas, V. Subramanian, A. Scholten, P. Wambacq, R. Velghe, G. Mnnaert, N. Heylen, R. Verbbeck, W. Boullart, I. Heyvaert, M.I. Natarajan, G. Groeseneken, I. Debusschere, S. Biesemans, and S. Decoutere, A low-cost 90 nm RF-CMOS platform for record RF circuit performance, Symp VLSI Tech (2005), 60–61.

3. W.K. Shih, S. Mudanai, R. Rios, P. Packan, D. Becher, R. Basco, C. Hung, and U. Jalan, Predictive compact modeling of NQS effects and thermal noise in 90 nm mixed-signal/RF CMOS technology, Int Electron Devices Meet (IEDM) Tech Dig (2004), 747–750.

4. K. Kuhn, R. Basco, D. Becher, M. Hattendorf, P. Packan, I. Post, P. Vandervoom, and I. Young, A comparison of state-of-the art NMOS and SiGe HBT devices for analog/mixed-signal/RF circuit applications, Symp VLSI Tech (2004), 224–225.

5. M.C. King, Z.M. Lai, C.H. Huang, C.F. Lee, M.W. Ma, C.M. Huang, Y. Chang, and A. Chin, Modeling finger number dependence on RF noise to 10 GHz in 0.13 μm node MOSFETs with 80nm gate length, IEEE RF IC Symp Dig (2004), Fort Worth, TX 171–174.

6. M.C. King, M.T. Yang, C.W. Kuo, Y. Chang, and A. Chin, RF noise scaling trend of MOSFETs from 0.5 μm to 0.13 μm technology nodes, IEEE MTT-S Int Microwave Symp Dig (2004), 6–11.

7. H.L. Kao, A. Chin, B.F. Hung, J.M. Lai, C.F. Lee, M.-F. Li, G.S. Samudra, C. Zhu, Z.L. Xia, and J.F. Kang, Strain-induced very low noise RF MOSFETs on flexible plastic substrate, Symp VLSI Tech (2005), 160–161.

8. H.L. Kao, A. Chin, J.M. Lai, C.F. Lee, K.C. Chiang, and S.P. McAlister, Modeling RF MOSFETs after electrical stress using low-noise microstrip line layout, RF IC Symp Dig (2005), Long Beach, CA 157–160.

9. L. Pantisano, D. Schreurs, B. Kaczer, W. Jeamsaksiri, R. Venegas, R. Degraeve, K. P. Cheung, and G. Groeseneken, RF performance vulnerability to hot carrier stress and consequent breakdown in low power 90 nm RFCMOS, Int Electron Devices Meet (IEDM) Tech Dig (2003), 181–184.

10. J.P. Walko and B. Abadeer, RF S-parameter degradation under hot carrier stress, IEEE IRPS Symp (2004), 422–425.

SENSITIVITY ANALYSIS OF ITERATIVE ADJOINT TECHNIQUE FOR MICROSTRIP CIRCUITS OPTIMIZATION

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ABSTRACT: *This paper presents an accurate and efficient full-wave method, combined with iterative adjoint technique, for analyzing sensitivities of planar microwave circuits with respect to design parameters. Method of moments (MoM) in spatial domain is utilized, and generalized conjugate residual iterative scheme is applied to solve the linear matrix equations with fast convergence. Green's functions for multilayer planar structures in DCIM form are employed to simplify the spatial domain manipulation. In the present method, a conventional integration model and the corresponding adjoint model are solved by MoM respectively. The adjoint technique, with the aid of iterative schemes, could significantly reduce the computational requirements, especially for the large electrical size device with many perturbing design parameters. Numerical results of S-parameter sensitivities of a low-pass microstrip filter by the present method are presented. Accuracy and efficiency are validated.* © 2007 Wiley Periodicals, Inc. Microwave Opt Technol Lett 49: 607–609, 2007; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.22204

1. INTRODUCTION

Sensitivity analysis is used to evaluate the sensitivity of system performance with respect to design parameters for optimized design. The sensitivity is usually denoted by the gradient of a response function, and then an efficient optimization method makes use of the derivative information of the response to obtain suitable design parameters. This article studies the efficiency of full-wave sensitivity analysis by the method of moments (MoM).

Sensitivities of charges and current densities for planar structures were first investigated by MoM in Refs. 1 and 2. In Ref. 1, shape sensitivities of electrostatic problems for planar structures were studied. By applying the flux-transport theorem, a new integral equation (IE) for the total derivative of the charge with respect to a geometrical parameter was derived from the original IE for the charge distribution. The two IEs were solved by the MoM using the same set of basis and testing functions. A similar approach with mixed potential integral equation (MPIE) was applied to analyze the sensitivities of current density distributions and S-parameters with respect to geometrical parameters in Ref. 2. Although this technique could obtain accurate sensitivity results, it needs complicated manipulations to analytically simplify the impedance ma-

trix elements and its implementation into the optimization environment would require large amount of reprogramming of the current MoM simulation tools. To make the programming implementation easier, a feasible adjoint technique [3] combined with MoM was proposed in Ref. 4 to realize the full-wave sensitivity analysis. Above techniques employ LU decomposition [5] to solve the two matrix equations, requiring $O(N^3)$ computation loads.

This article presents a full-wave technique to analyze sensitivities of multilayer planar structures. With the aid of iterative adjoint technique and the spatial Green's functions in DCIM form [6, 7], the present technique has the following advantages: (1) the adjoint technique is employed to make the sensitivity analysis very easy to implement into the current MoM-based simulation tools; (2) the iterative scheme (generalized conjugate residual, GCR) is introduced to solve the matrix equation, requiring $O(N^2)$ computation for each step. It would greatly save computation time if the iteration converges fast; (3) the spatial Green's kernel in DCIM form makes it possible to investigate the performance sensitivity with respect to the geometrical parameters, which the Green's function is dependent on. This case cannot be solved in Ref. 2. In the present study, sensitivities of S-parameters of a low-pass filter with respect to the design parameters are analyzed to validate the accuracy and efficiency of the present technique.

2. FORMULATION

MoM subject to the MPIE has been proved as an accurate and efficient technique to analyze properties of multilayer planar structures. Current density distribution on metal patch is first solved via linear matrix equation as

$$Z(x)I = V \quad (1)$$

where x is a vector of design parameters, which need to be adjusted to optimize circuit performance. Elements in the impedance matrix Z are obtained as

$$Z_{ij} = j\omega\varepsilon \int_{S_i}\int_{S_j} \overline{G}_A(r,r') \cdot f_j(r') \cdot f_i(r)ds'ds$$

$$+ \frac{1}{j\omega}\int_{S_i}\int_{S_j} G_q(r,r')\nabla \cdot f_i(r)\nabla' \cdot f_j(r')ds'ds \quad (2)$$

where $f_i(r)$ and $f_j(r')$ are the RWG testing and basis functions, and S_i and S_j are their supports, respectively. $\overline{G}_A$ and G_q are the spatial Green's functions in DCIM form for vector and scalar potentials respectively. Here, we use GCR iterative schemes to solve the matrix equation, which needs $O(N^2)$ computation cost for each iterative step. The scattered field can be expressed as

$$E_{sc} = -j\omega A - \nabla\Phi \quad (3)$$

where the vector and scalar potentials can be obtained by using

$$A(r) = \int\int_S \overline{G}_A(r,r') \cdot I(r')dS' \quad (4)$$

$$\Phi = \int\int_S G_q(r,r')\nabla \cdot I(r')dS' \quad (5)$$