Highly Reliable Multilevel and 2-bit/cell Operation of Wrapped Select Gate (WSG) SONOS Memory

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***Abstract*—In this letter, high-performance and reliable wrapped select gate (WSG) polysilicon–oxide–nitride–oxide–silicon (SONOS) memory cells with multilevel and 2-bit/cell operation have been successfully demonstrated. The multilevel storage is easily obtained with fast program/erase speed (10 μs/5 ms) and low programming current (3.5 μA) for our WSG SONOS by a source-side injection. Besides the excellent reliability properties of our multilevel WSG-SONOS memory including unconsidered gate and drain disturbance, long charge retention ($> 150\ ^{\circ}$C) and good endurance ($> 10^4$) are also presented. This novel WSG-SONOS memory with a multilevel and 2-bit/cell operation can be used in future high-density and high-performance memory application.**

***Index Terms*—Multilevel operation, source-side injection, wrapped select gate (WSG) polysilicon–oxide–nitride–oxide–silicon (SONOS).**

I. Introduction

RECENTLY, the polysilicon–oxide–nitride–oxide–silicon (SONOS) memory device has received a lot of attention due to the advantages over the traditional floating-gate flash electrically erasable programmable read-only-memory device, including the reduced operation voltage [1], lower process complexity [2], elimination of drain-induced turn-ON [3], and improved cycling endurance [4]. To achieve the high-density flash memory device, multilevel storage and 2-bit/cell operation are becoming important topics, and it has been proposed that these flash devices [5]–[7] will be applied as the mass storage of portable handy terminals, solid-state cameras, and PC cards. By storing different amount of charges in the nitride trapping layers to reliably distinguish different levels and treating these levels as different combination of bits, the multilevel storage can be successfully performed. In addition, the 2-bit/cell operation for a single cell by using the forward/reverse reading method also effectively enhanced the performance of SONOS memory device. Nevertheless, owing to some critical issues such as charge redistribution during the program [8], charge diffusion in silicon nitride after injection [9], and bottom oxide charge by the cycling [10], it will be more difficult to obtain the local 2-bit/cell characteristics and multilevel operation in sub-90-nm regime. Besides, the multilevel operation is hard to perform by the conventional channel hot electron injection and Fowler–Nordheim tunneling with the low efficiency of the electron injection, poor programming speed, and high operation voltage. Consequently, a novel source-side injection technique has been proposed in the SONOS memory for high-speed programming [11]–[13]. In this letter, we for the first time demonstrate that the wrapped select gate (WSG) SONOS memory with the source-side injection exhibits high-performance multilevel and 2-bit/cell operation. A fast and excellent control of the storage charge is obtained even after large programming disturbance and $> 10^4$ program/erase (P/E) cycling. Moreover, a superior charge retention behavior after a high-temperature baking ($> 150\ ^{\circ}$C) of the WSG-SONOS memory is also presented for highly reliable multilevel and 2-bit/cell flash application.

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II. Experimental

The simple cross-sectional structure of the WSG-SONOS device was indicated in Fig. 1, and the 0.18-μm ground rule technology was used to fabricate our device. The select gate, which was used for an assist gate in the source-side injection, is wrapped with both an oxide-nitride-oxide layer and a word line gate. The fabrication procedures were therefore easily compatible with the general process for the fabrication of complementary metal-oxide-semiconductor integrated circuit. Besides, both source and drain regions can be used as the bit line in the WSG-SONOS memory. In our device, the tunneling oxide/nitride/blocking oxide layers were 5.0/8.0/10.0-nm thick, and the length and width of the select gate were 0.18 and 0.36 μm, respectively.

According to our WSG-SONOS structure, the 2-bit/cell operation of the WSG-SONOS memory can be easily achieved, as shown in the inset of Fig. 1. In addition, the basic two-bit operation conditions of the WSG-SONOS memory were listed in the inset table. Here, only bit-1 was programmed and bit-2 was on initial state. A clear two physical bits storing characteristic in our WSG-SONOS memory was demonstrated from the threshold voltage difference of these two bits which

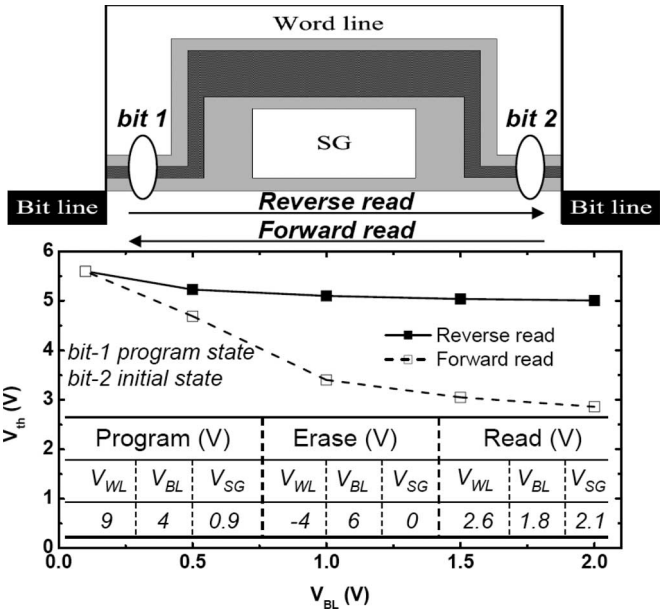

Fig. 1. Cross-sectional scheme of a 2-bit/cell WSG-SONOS memory device with WSG structure. The inset figure shows the excellent 2-bit/cell characteristics for the WSG-SONOS memory. In addition, the basic operation conditions of WSG-SONOS memory are listed in the inset table.

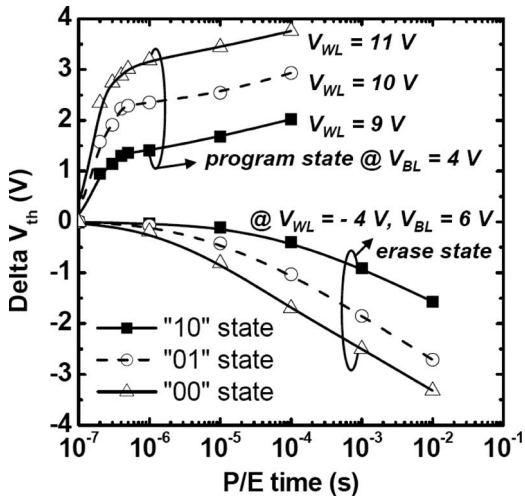

Fig. 2. Multilevel programming and erasing characteristics. The $V_{\rm th}$ shift is larger than 1, 2, and 3 V at $V_{\rm SG} = 0.9$ V, while the programming time is only 1 μs for $V_{\rm WL} = 9$, 10, and 11 V, respectively.

can reach up to 2.0 V during reading, while the drain and source were biased at 1.8 and 0 V, respectively.

III. Results and Discussion

To achieve the multilevel operation, 9, 10, and 11 V were applied to the word gate while the drain, source, and select gate were biased at 4, 0, and 0.9 V, respectively. Under this bias condition, the WSG-SONOS memory was programmed by the source-side injection mechanism. Therefore, as shown in Fig. 2, the word line biased at 9, 10, and 11 V to achieve the "10," "01," and "00" states (programming time T_p is 1 μs) can be easily obtained, while the device is reverse-read at $V_{\rm BL} = 1.8$ V. The window from state to state is larger than

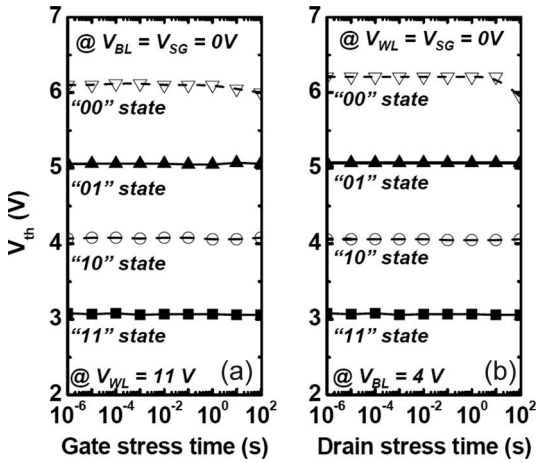

Fig. 3. (a) Gate and (b) drain disturbance performance of the WSG-SONOS memory for the multilevel operation. The $V_{\rm th}$ shift is only about 0.1 V after 100-s word-line stressing ($V_{\rm WL} = 11$ V) for the "00" state and 0.5 V after 100-s bit-line stressing ($V_{\rm BL} = 4$ V) for the "00" state.

1 V for programming at $V_{\rm SG} = 0.9$ V, and T_p is only 1 μs. On the other hand, with the erasing time of only 5 ms for $V_{\rm WL} = -4$ V and $V_{\rm BL} = 6$ V, the multilevel bits can be easily erased by a band-to-band hot hole erasing. Besides, the high programming speed is achieved by quite low programming current smaller than 3.5 μA ("00" state). We believe that this high-speed programming performance of the multilevel operation is attributed to the high-injection efficiency of the source-side injection mechanism [11].

The failure phenomenon, i.e., "program disturbance," often takes place under the electrical stress applied to those neighboring unprogrammed cells during programming a specific cell in the array. Two types of program disturbances including gate (word-line) disturbance and drain/source (bit-line) disturbance are needed to be considered. Fig. 3(a) and (b) shows the gate and drain stressed characteristics of the WSG-SONOS memory with the multilevel operation, respectively. The deviation by the gate disturbance can be found to be less than 0.1 V after 100-s stress for all states. On the other hand, only a small negative shift in "00" state (initial state) of the drain disturbance is observed due to the drain field induced hole injection by a band-to-band tunneling [14]. This drain disturbance can be almost ignored for the other multilevel states of our WSG-SONOS memory device.

Fig. 4 shows the data retention behavior of the WSG-SONOS memory with a multilevel operation at the elevated temperatures of 85 °C, 150 °C, and 250 °C, respectively. There is almost no charge loss for the multilevel operation of WSG-SONOS memory at 85 °C and 150 °C, as indicated in this figure. However, a slightly increased charge loss is observed under the quite high-temperature condition of 250 °C. This charge loss may be resulted from the detrapping process in which the trapped electrons tend to migrate and redistribute in the silicon nitride at elevated temperature [14]. However, this charge loss saturates, and the different states of multilevel operation can still easily be discerned, as shown in this figure. Furthermore, the endurance characteristic of the WSG-SONOS memory is shown in Fig. 5. The cell programmed at $V_{\rm WL} = 9$, 10, and

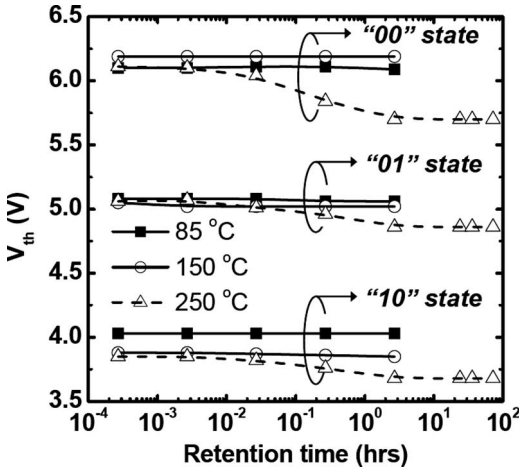

Fig. 4. Data retention performance of the WSG-SONOS memory for the multilevel operation after different high-temperature baking. The $V_{\rm th}$ shift for "00" state is smaller than 0.5 V after 10 000 s at 250 °C baking.

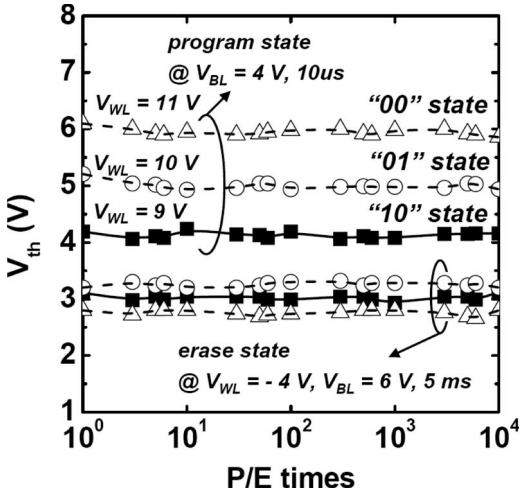

Fig. 5. Endurance characteristics of the WSG-SONOS memory for the multilevel operation. The memory window is almost the same even after 10k P/E cycling for the different programming states.

11 V, and $V_{\rm BL} = 4$ V for 10 μs, and erased at $V_{\rm WL} = -4$ V and $V_{\rm BL} = 6$ V for 5 ms was used for multilevel operation. The threshold voltage of each state is almost the same even after 10^4 P/E cycles. Nearly negligible window narrowing for multilevel operation of the WSG-SONOS memory is observed, meaning that the high-performance and reliable flash memory is successfully realized.

IV. Conclusion

For the first time, a novel and highly reliable multilevel and 2-bit/cell WSG-SONOS memory was demonstrated. The multilevel storage is easily obtained with a fast P/E speed $(10\ \mu{\rm s}/5\ {\rm ms})$ by the source-side injection. In addition, the gate and drain disturbances for multilevel storage of this memory can be nearly ignored. The superior data retention $(> 150\ ^\circ{\rm C})$ and endurance characteristics (10^4) indicated that this WSG-SONOS memory with multilevel and 2-bit/cell operation can be applied into future high-density and high-performance flash memory.

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