Impact of High-κ Offset Spacer in 65-nm Node SOI Devices

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***Abstract*—In this letter, 65-nm node silicon-on-insulator devices with high-κ offset spacer dielectric were investigated by extensive 2-D device simulation. The result shows that the high-κ offset spacer dielectric can effectively increase the ON-state driving current $I_{\rm ON}$ and reduce the OFF leakage current $I_{\rm OFF}$ due to the high vertical fringing electric field effect. This fringing field can significantly improve the $I_{\rm ON}/I_{\rm OFF}$ current ratio and the subthreshold swing compared with the conventional oxide spacer. Consequently, the gate-to-channel control ability is enhanced by the fringing field via the high-κ offset spacer dielectric.**

***Index Terms*—Fringing electric field, high-κ offset spacer dielectric, silicon-on-insulator (SOI).**

I. Introduction

CMOS TECHNOLOGY requires high-performance and low-power transistors with a high driving current $I_{\rm ON}$. Silicon-on-insulator (SOI) MOSFETs are one of the more promising candidates for further scaled MOSFETs [1]–[3]. According to International Technology Roadmap for Semiconductors [1], much effort has been devoted in recent years to realize the 65-nm node SOI processes with 32-nm channel length and oxide thickness $t_{\rm ox} = 12$ [4]–[6]. In order to increase reliability and reduce the leakage current, conventional offset-gated or lightly doped drain structures have been widely used to reduce the lateral drain electric field. However, these structures inevitably decrease the ON driving current $I_{\rm ON}$ due to the extra series resistance. In mainstream CMOS technology, different offset spacer dielectrics are used to reduce the OFF leakage current $I_{\rm OFF}$ and improve the ON-state driving current $I_{\rm ON}$ [7]–[10]. When CMOS transistor technology is scaling down to 65-nm node or beyond, the width of the gate spacer of the transistor becomes a critical feature for minimizing the circuit size [1]. It is because the scaling down of sidewall spacer is not proportional to the scaling down of channel length, resulting in inefficiently scaled device size. Consequently, the fringing electric field becomes a very important factor in short channel devices because of inefficiently scaled spacer widths [11]–[13]. However, there are several competing effects between gate, source, and drain terminals, like fringing-induced barrier lowering (FIBL), drain-induced barrier lowering, fringing-induced barrier shielding, and zero-bias internal barrier lowering, all of which have been studied in 50-nm channel length MOSFETs [10]. In addition to these effects, the reduced series resistance effect due to an enhanced fringing field by using high-κ offset spacer contributes significantly toward the improvement of ON-state driving current $I_{\rm ON}$ to compete with other influences [7]. Therefore, all effects must be considered simultaneously.

In this letter, the 65-nm node SOI devices with four different offset spacer dielectrics are investigated using a 2-D device simulator MEDICI [14]. It is found that with the increase in spacer dielectric constant, the fringing field effect in the source/drain (S/D) extension region is enhanced, elevating the electron potential barrier of the channel film at the OFF, resulting in a reduced $I_{\rm OFF}$. This also reduces the potential barrier and series resistance effect in the channel film at the ON-state, thereby increasing the driving current $I_{\rm ON}$. The vertical electric field and the potential of the surface channel are employed to illustrate the impacts of the high-κ offset spacer in 65-nm node SOI devices. The results are also valid for bulk MOSFETs.

II. Simulation Procedure

Commercial MEDICI programs were used to generate a typical device structure of 65-nm SOI with 32-nm channel length, 12-Å or 1.2 nm gate oxide thickness, and 15-nm body thickness. The doping level of the channel film, S/D, and S/D extension were 5×10^{18}, 5×10^{20}, and 1×10^{19} cm^{-3}, respectively. In order to point out the fringing field effect in the channel and S/D extension, we employ the lightly doped S/D extension concentration and constant doping profile instead of well-tempered doping profile to simplify our structure and analysis [15], [16]. The spacer width was fixed at 30 nm [6], [11], [12]. Four κ values for the offset spacer dielectric were used, including air ($\varepsilon_r = 1$), SiO_2 ($\varepsilon_r = 3.9$), SiN ($\varepsilon_r = 7.5$), HfO_2 ($\varepsilon_r = 25$), and TiO_2 ($\varepsilon_r = 80$), to study the fringing electric field effect on the devices' performance. The threshold voltage $V_{\rm th}$ is defined as the gate voltage at which the drain–current reaches 100 nA/μm and $V_{\rm DS} = 1$ V. The threshold voltages of the transistors with different spacers are all about 0 V.

III. Results and Discussion

Fig. 1(a) and (b) shows the SOI device structure and vertical channel electric field at OFF- and ON-state, respectively.

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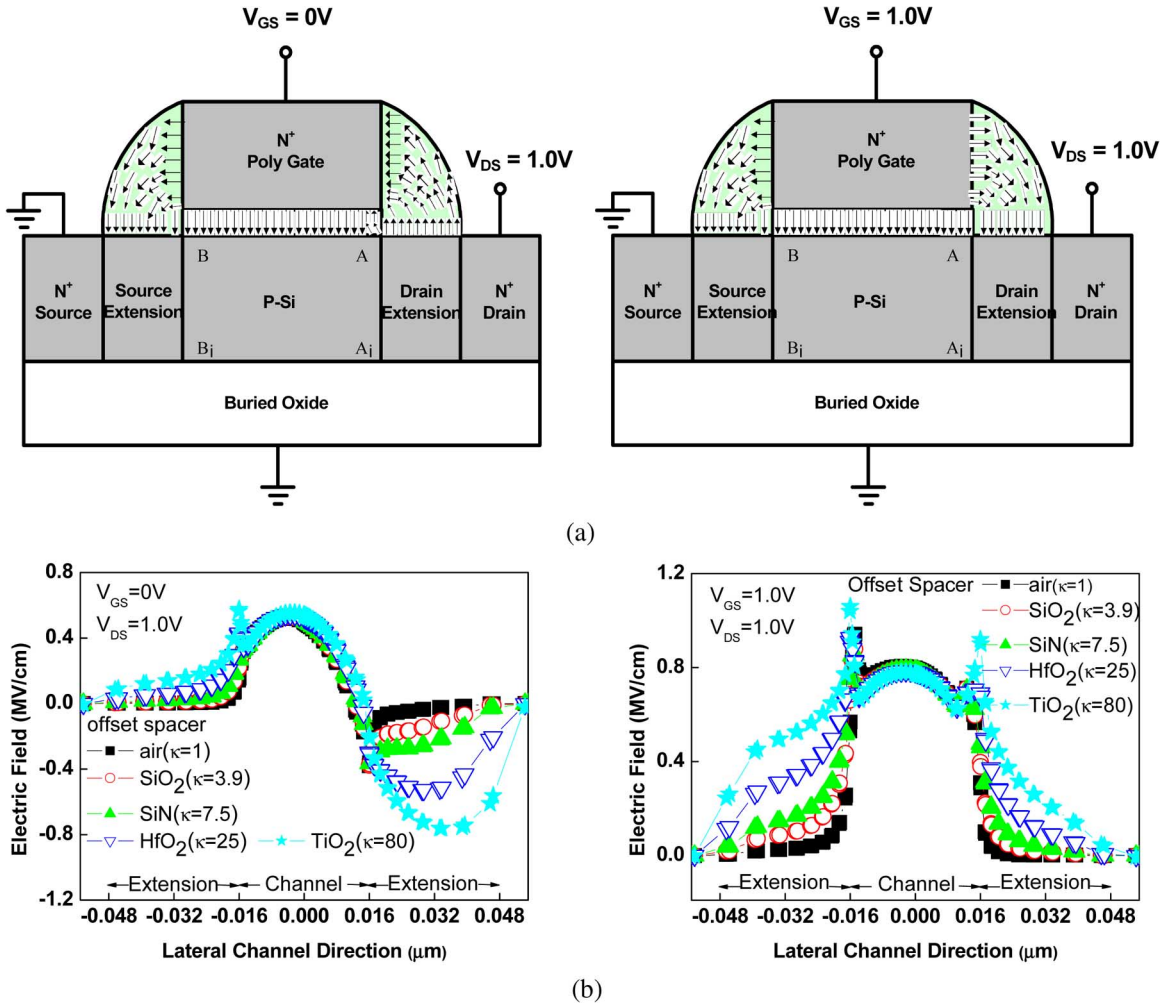

Fig. 1. (a) SOI device structure and (b) vertical channel electric field with different offset spacer dielectrics at OFF ($V_{\rm GS} = 0$ V and $V_{\rm DS} = 1.0$ V) and ON-state ($V_{\rm GS} = 1.0$ V and $V_{\rm DS} = 1.0$ V), respectively.

From Fig. 1(a), we can see that the electric field comes to the polygate from the drain extension region and goes to the source extension region from the polygate at the OFF, i.e., $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 0$ V. This implies that the gate potential elevated the source-side potential and lowered the drain-side potential via offset sidewall spacers as shown in Fig. 2, resulting in an increased electron barrier height to reduce the OFF current. However, the vertical electric field direction is reversed in the drain extension region at the ON-state, i.e., $V_{\rm DS} = 1.0$ V and $V_{\rm GS} = 1.0$ V, as shown in Fig. 1(b). This means that the gate potential elevates the drain-side potential via offset sidewall spacers to reduce the electron barrier height in the thin film and also decreases the S/D series resistance in the extension regions (i.e., the junctions become more accumulated), resulting in an increased driving current $I_{\rm ON}$. With the offset spacer dielectric constant increased, the electric field is enhanced substantially, so that the channel potential is more easily affected by the gate potential.

Fig. 3 shows the $I_{\rm DS}$–$V_{\rm DS}$ curve, which clearly shows the improvement of the driving current $I_{\rm ON}$ with the increase of the offset spacer dielectric constant as described above. Fig. 4 shows the extracted $I_{\rm ON}/I_{\rm OFF}$. For the $\varepsilon_r = 80$ case, an increase of approximately 26% of $I_{\rm ON}$ and a 34% reduction

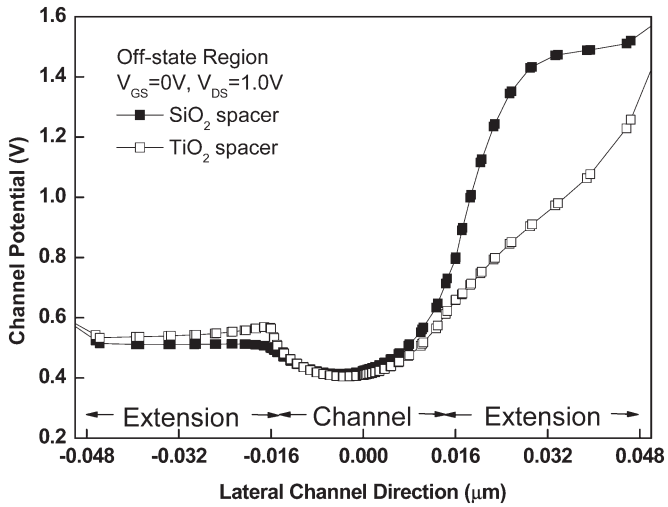

Fig. 2. Surface channel potential with different SiO_2 and TiO_2 spacer dielectrics at OFF-state ($V_{\rm GS} = 0$ V and $V_{\rm DS} = 1.0$ V).

of $I_{\rm OFF}$ can be achieved compared to SiO_2 ($\varepsilon_r = 3.9$) at 1-V supply voltage. The resultant $I_{\rm ON}/I_{\rm OFF}$ ratio is also shown in Fig. 4, indicating that a significant improvement of about two times in $I_{\rm ON}/I_{\rm OFF}$ can be obtained. However, the fringing field

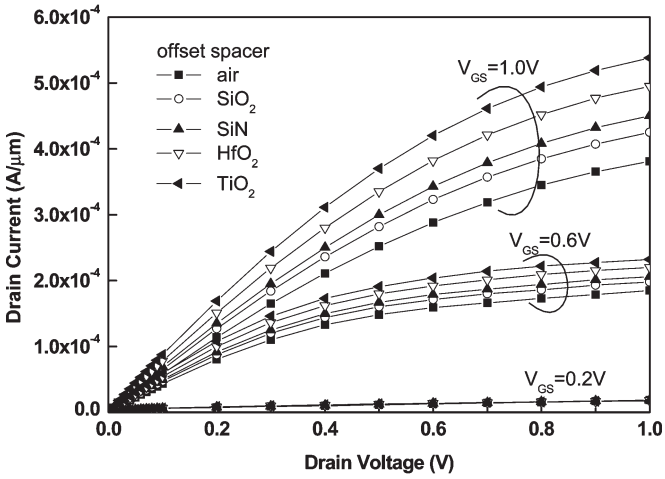

Fig. 3. $I_{\rm DS}$–$V_{\rm DS}$ characteristics of four dielectric offset spacer SOI devices. The driving current increases with the κ value of the offset spacer dielectric.

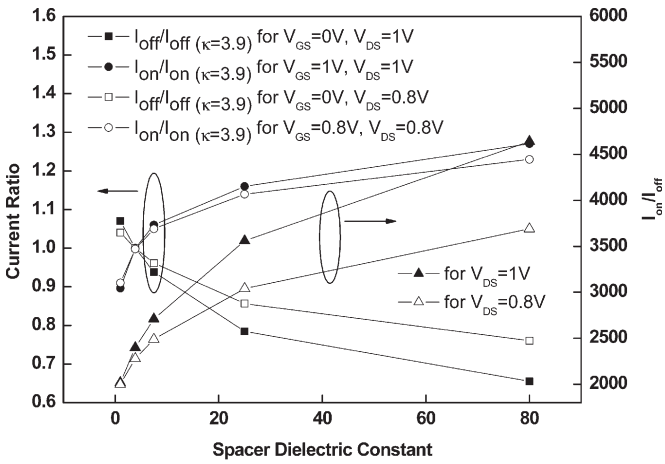

Fig. 4. Current ratio of OFF-state leakage $I_{\rm OFF}/I_{\rm OFF}$ ($\kappa = 3.9$), ON-state driving current $I_{\rm ON}/I_{\rm ON}$ ($\kappa = 3.9$), and ON-OFF state $I_{\rm ON}/I_{\rm OFF}$ of SOI devices with different offset spacer dielectrics and supply voltages.

effect on ON- and OFF currents is reduced if the supply voltage is scaling down, as shown in Fig. 4.

Fig. 5 shows the subthreshold swing characteristic for the 65-nm SOI device with different offset spacer dielectric constants. The subthreshold swing is improved as the offset spacer dielectric constant is increased. These results imply that the gate-to-channel control ability is enhanced due to the assistance of the high-κ offset spacer dielectric. As a result, a lower OFF leakage current and higher driving current 65-nm SOI devices can be achieved by using a high-κ offset spacer dielectric, thereby effectively reducing the power dissipation and increasing the performance of the transistor.

The fringing field effects contributed to the reduced S/D series resistance (R_S/R_D) and to the enhanced FIBL in the channel, and therefore improved the on-current. In addition, the FIBL effect played a more important role in the $I_{\rm ON}$ improvement. In order to distinguish the contribution of $R_{\rm S/D}$ and FIBL, we define the output resistance $R_{\rm out} = V_{\rm DS}/I_{\rm DS}$. R_S and R_D were extracted by grounding the junction planes [A-A' and B-B' in Fig. 1(a)] between the channel and the S/D extensions [17]. The improvement of R_S/R_D and $R_{\rm out}$ was

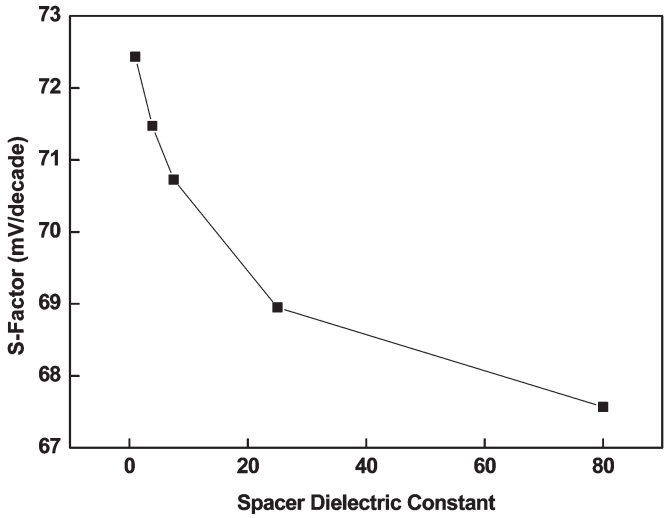

Fig. 5. S-factor of an SOI device with different offset spacer dielectrics. It shows the excellent gate-to-channel control ability in the subthreshold region.

306 to 239 $\Omega \cdot \mu$m for R_S, 840 to 821 $\Omega \cdot \mu$m for R_D, and 2353 to 1859 $\Omega \cdot \mu$m for $R_{\rm out}$, respectively, when the SiO_2 spacer replaced with TiO_2 spacer at ON, $V_{\rm GS} = V_{\rm DS} = 1$ V. The improvement on R_S is much more than R_D because of the stronger field in source side region as shown in Fig. 1(b), and it also indicates that the values of R_S and R_D are bias dependent. We can calculate the ratio $\Delta R_{\rm S/D}/\Delta R_{\rm out} = (67 + 19)/494 = 17.4\%$. Therefore, among the 26% improvement of $R_{\rm out}$, $R_{\rm S/D}$ contributes only 4.5%, and FIBL contributes about 21.5%.

Note that, due to the enhanced fringing field with high-κ spacers, the drain extension provided better voltage coupling from drain junction, resulting in more serious channel length modulation. As a result, the saturation currents were significantly improved.

However, although anticipated, the higher $C_{\rm gd}$ and $C_{\rm gs}$ of high-κ spacer devices compared to those with an oxide spacer are a matter of concern. If we assume a classical small-signal equivalent circuit for MOSFET, we can express f_t and $f_{\rm max}$ as follows [18], [19]:

$$f_t = \frac{g_m}{2\pi C_{\rm gin}\sqrt{1 + 2\frac{C_{\rm Miller}}{C_{\rm gin}}}} \tag{1}$$

$$f_{\rm max} = \frac{g_m}{2\pi C_{\rm gin}} \frac{1}{2\sqrt{(R_g + R_s + R_i)\left(g_d + g_m \frac{C_{\rm Miller}}{C_{\rm gin}}\right)}} \tag{2}$$

where $C_{\rm gin} = C_{\rm gs} + C_{\rm overlap} + C_{\rm fringing}$ and $C_{\rm Miller} = C_{\rm gd} + C_{\rm overlap} + C_{\rm fringing}$ with g_m, the gate transconductance, $C_{\rm gin}$, the total gate-to-source input capacitance and $C_{\rm Miller}$, the total gate-to-drain capacitance, or Miller capacitance. Among these parameters, $C_{\rm gin}$ and $C_{\rm Miller}$ are strongly dominated by $C_{\rm overlap}$ because $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm fringing}$ are very low compared with $C_{\rm overlap}$. In our case, the $C_{\rm gd}$ and $C_{\rm gs}$ will double if the HfO_2 spacer is used. However, it will affect the ac characteristic very little because of the almost compensated $C_{\rm Miller}/C_{\rm gin}$ in (1) and (2). By using the polysilicon spacer [20], [21], a larger

overlap capacitance C_{overlap}, almost 18 times higher than that of the oxide spacer was found in our simulation, which is higher than the high-κ spacer and which seriously degrades the ac performance.

IV. Conclusion

It was found that the gate-to-channel control ability of short channel SOI devices can be significantly enhanced using a high-κ offset spacer. Devices with this structure show a higher ON driving current and a lower OFF leakage current as well as subthreshold swing and counterparts.

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