A 90-dBΩ 10-Gb/s Optical Receiver Analog Front-End in a 0.18-μm CMOS Technology

Wei-Zen Chen, *Member, IEEE*, and Da-Shin Lin

***Abstract*—A 10-Gb/s 90-dBΩ optical receiver analog front-end (AFE), including a transimpedance amplifier (TIA), an automatic gain control circuit, and a postamplifier (PA), is fabricated using a 0.18-μm CMOS technology. In contrast with a conventional limiting amplifier architecture, the PA is consisted of a voltage amplifier followed by a slicer. By means of the TIA and the PA codesign, the receiver front-end provides a −3-dB bandwidth of 7.86 GHz and a gain bandwidth product (GBW) of 248.5 THz-Ω. The tiny photocurrent received by the AFE is amplified to a differential voltage swing of 900 mV_{pp} when driving 50-Ω output loads. The measured input sensitivity of the optical receiver is −13 dBm at a bit-error rate of 10^{-12} with a $2^{31}-1$ pseudorandom test pattern. The optical receiver AFE dissipates a total power of 199 mW from a 1.8-V supply, among which 35 mW is consumed by the output buffer. The chip size is $1300\ \mu m \times 1796\ \mu m$.**

***Index Terms*—Optical receiver, postamplifier (PA), transformer, transimpedance amplifier (TIA).**

I. Introduction

THIS PAPER describes an optical receiver analog front end (AFE) that incorporates a transimpedance amplifier, an automatic gain control circuit, and a post amplifier (PA) in a single chip. Conventionally, the PA is basically a limiting amplifier which consists of identical gain cells and with equal gain-bandwidth performance in each gain stage [2], [6], [7]. However, in such a multistage cascaded amplifier, the last few stages may be driven into large-signal operation mode, and the overall signal bandwidth is limited by the first few stages. It turns out that the gain and bandwidth assignment for each gain stage is not optimally designed.

Different from the prior art, in this design, the PA is composed of a voltage amplifier followed by a slicer, whose gain and bandwidth are assigned separately. Thus, their gain bandwidth product (GBW) requirement per stage can be further relaxed so as to save power dissipation. The proposed receiver also provides several advantages over conventional multiple chips solutions [1]–[3]. First, tiny photocurrent generated from the photodetector can be on-chip enlarged to a logic level. It increases noise immunity and off-chip interference can be avoided. Second, no interstage matching networks are required at the transimpedance amplifier (TIA) output stage and the input stage of the PA. Broadband matching networks in general induce gain loss and are power hungry. By these means the receiver manifests a GBW as high as 248.5 THz-Ω and consumes much less power while fewer peaking inductors are required in comparison to the prior art.

This paper is organized as follows. Section II describes the architecture of the optical receiver. The TIA and the PA are codesigned, and the design issues of the receiver AFE are discussed in Section III. To achieve both wide-band and high gain design goals, inductive peaking techniques are adopted using 3-D symmetric transformers [4]. In this paper, distributed capacitance models [13] of the 3-D transformer are proposed, and its superiorities over the conventional architectures are investigated in detail. Their performance comparisons are discussed in Section IV. Section V describes the experimental results. Finally, our conclusions are presented in Section VI.

II. Optical Receiver Architecture

The receiver architecture is shown in Fig. 1, which integrates a transimpedance amplifier, an automatic gain control (AGC) circuit, and a PA in a single chip. To alleviate bandwidth degradation caused by the parasitic capacitance of the photodetector and IC package, a regulated cascode (RGC) input stage is adopted [5]. The TIA architecture is in pseudo differential configuration with shunt-feedback for better sensitivity and higher common mode noise immunity. Furthermore, an AGC loop is built in to avoid data jitter induced by signal overload. The AGC is composed of an amplitude detector, a comparator, and an integrator [15]. As the TIA's output swing exceeds a threshold voltage, the AGC will be activated to keep output amplitude constant by turning on the tunable feedback resistors M3 and M4. Otherwise, the AGC will be disabled, and M3 and M4 are switched off for high-gain and low-noise operation. The single ended TIA output is converted to a fully differential signal by the B1 amplifier in conjunction with the R1 and C1 low-pass filter. The conversion gain of the TIA is chosen to make its output swing overpass the sensitivity level of the PA, and its bandwidth is chosen to compromise between ISI and noise performance [7].

Different from our previous work in [7], the PA is consisted of a voltage amplification stage (for small-signal amplification) followed by a slicing stage (for large signal operation). In contrast to a conventional limiting amplifier that is composed of five or six identical gain cells [2], [6], [7], the voltage amplifier is designed to provide a sufficient gain to fully switch the slicer. In

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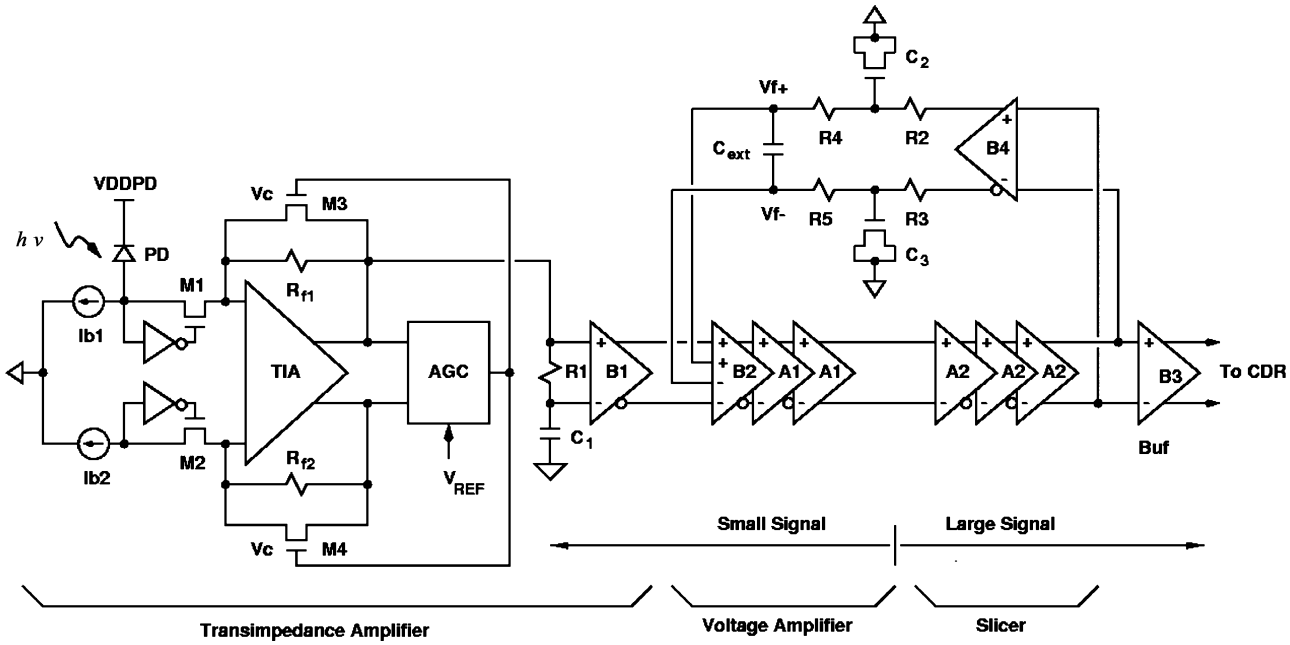


Fig. 1. Optical receiver architecture.

this case, a three-stage cascaded amplifier is required for a minimum power dissipation. Thus the required GBW per gain stage is much relaxed compared to that of conventional architectures, and no peaking inductors are required in the voltage amplifier design. The slicer functions as a predriver for the output buffer. As a large-signal operation stage, it also provides 24-dB conversion gain before driving the last buffer stage, and the bandwidth degradation caused by the slicer is almost negligible [8].

III. TIA AND PA CODESIGN

For an optical receiver, the input sensitivity is limited by the input referred noise current $\overline{I_{n,\text{in}}^2}$, which can be expressed

$$\overline{I_{n,\text{in}}^2} = \overline{I_{n,\text{TIA}}^2}\text{BW}_{\text{TIA}} + \frac{\overline{V_{n,\text{PA}}^2}\text{BW}_{\text{PA}}}{T_z^2} \tag{1}$$

where T_z is the conversion gain of the TIA, $\overline{I_{n,\text{TIA}}^2}$ and $\overline{V_{n,\text{PA}}^2}$ represent the input referred noise current of the TIA and the input referred noise voltage of the PA, BW_{TIA} and BW_{PA} denote their noise bandwidth, respectively. The lower bound of the T_z is chosen to avoid the PA degrading the input sensitivity level, and the input referred noise current of the TIA is essential to the overall receiver performance. As a rule of thumb, the -3-dB bandwidth of the TIA is chosen to be about 0.7 bit rate to compromise between ISI and noise performance, while the -3-dB bandwidth of the PA is chosen for about 1.2 bit rate to minimize ISI.

In this design, to achieve an input sensitivity level of -13 dBm with a photodetector whose responsivity is 1 A/W, the transimpedance amplifier is designed to provide a conversion gain of 50 dBΩ and a -3 dB bandwidth of about 8 GHz. The TIA output is then enlarged and limited to a voltage swing of 900 mVpp (differential) to drive external 50–Ω loads by the PA. The corresponding conversion gain in the post amplification stage is about 40 dB. Since the output stage delivers high output current and introduces significant capacitance to the amplifier core, inverse scaling [16] is not applied in this design [2].

Conventional PA is comprised of identical cascaded gain cells [2], [6], [7]. Assuming each gain cell is identical and approximated by a two-pole amplifier, its conversion gain can be described by A(s), where

$$A(s) = \frac{A_s \cdot \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{2}$$

Here, A_s denotes the small-signal dc gain, ζ is the corresponding damping factor, and ω_n is the nature frequency. Let the targeted -3 dB bandwidth of an N-stage cascaded amplifier be ω_c, and the conversion gain be A_c. For a flat response, the required gain bandwidth product (GBW) per stage can be expressed as [2], [6]

$$\text{GBW} = \omega_c \times \left(\frac{1}{2^{1/N}-1}\right)^{1/4} \times A_c^{1/N}. \tag{3}$$

For a targeted bandwidth of 12 GHz and a conversion gain of 40 dB, according to (3), a five-stage limiting amplifier demands a GBW of 49 GHz per stage, and, thus, inductive peaking for bandwidth enhancement is required in a conventional design. In contrast to a conventional limiting amplifier that is comprised of identical gain cells, in this design, the PA is constructed of a voltage preamplifier (small-signal operating stage) followed by a slicer (large-signal operating stage). For the same input sensitivity level, the preamplifier only needs to provide 16-dB voltage gain to fully switch the slicer. Thus, a three-stage voltage amplifier is chosen for a minimum power dissipation by the analytical model proposed in [6]. It corresponds to a required GBW of 35 GHz per stage according to (3), which is much relaxed compared to that of a conventional stand-alone limiting amplifier with identical gain cells. A lower GBW per stage means no special peaking inductors are required in the gain cell design,

and the chip area can be further saved. The slicer stage, which is consisted of three identical buffers, further provides 24-dB conversion gain before driving the last output buffer. Since it is a large-signal operating stage, the bandwidth degradation caused by the slicer is negligible [8].

The core circuit of the voltage amplifier is shown in Fig. 2(a), which is based on Cherry-Hooper circuit architecture with active feedback [2], [17]. Compared to the prior art in [2], since the GBW requirement of the gain cell is much relaxed, thus no peaking inductor is required to save area. Also, different from our previous work in [7] using resistive feedback, unilaterally active feedback avoids tradeoffs between the feedback factor (close loop gain) and the open loop gain (close loop bandwidth) of the voltage amplifier.

Let C1 and C2, respectively, represent the parasitic capacitance at the drain node of M1 and M3, G_{m1} and G_{m2} denote the transconductance of the differential pair $(M_1 - M_2)$ and $(M_3 - M_4)$, and G_{mf} be the transconductance of the active feedback stage $(M_{f1} - M_{f2})$, the conversion gain of the voltage amplifier can be derived as [2]

$$\frac{V_o}{V_i} = \frac{A_v \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2} \tag{4}$$

where

$$A_v = \frac{G_{m1}G_{m2}R_1R_2}{1 + G_{m2}G_{mf}R_1R_2} \tag{5}$$

$$\varsigma = \frac{1}{2}\frac{R_1C_1 + R_2C_2}{\sqrt{R_1R_2C_1C_2(1 + G_{mf}G_{m2}R_1R_2)}} \tag{6}$$

$$\omega_n = \sqrt{\frac{1 + G_{mf}G_{m2}R_1R_2}{R_1R_2C_1C_2}}. \tag{7}$$

For a maximally flat Butterworth response, the -3-dB bandwidth of the voltage amplifier is about ω_n. In addition, it has been shown in [2] that the active feedback can increase the GBW of the voltage amplifier beyond the technology f_T. The core cell of the slicer is shown in Fig. 2(b). Herein, a symmetric transformer is utilized to accelerate voltage switch and balance the rising and the falling time of the output waveform at a high voltage level.

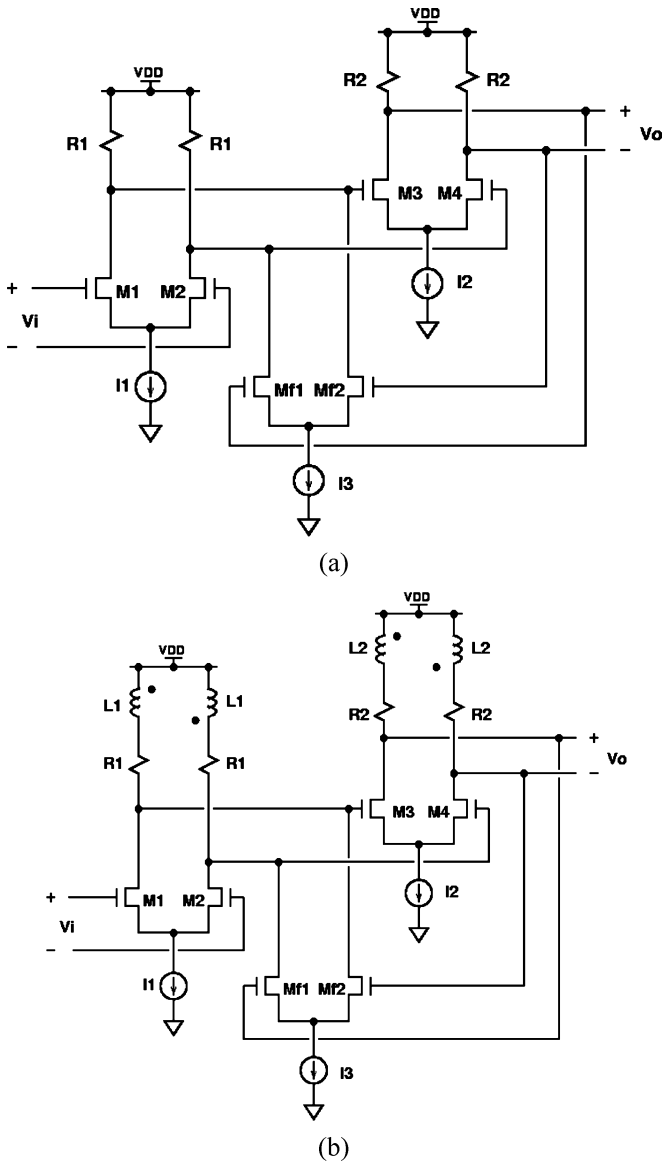


Fig. 2. (a) Gain cell of preamplifier. (b) Gain cell of slicer.

IV. Distributed Capacitance Model of Transformers

To realize broadband amplifiers under low supply voltage, inductive peaking techniques are applied in the TIA, slicer, and buffer stage design [9]. Conventional planar inductors and transformers are in general bulky and occupy significant chip areas [10], [11]. Although a miniaturized 3-D inductor structure has been proposed [12], it is asymmetric and two inductors are needed in a fully differential amplifier. To reduce inductor counts and save chip area, a 3-D inverting type transformer is utilized in this design [4]. Furthermore, as a peaking inductor in a broad band amplifier design, the self-resonant frequency (f_{SR}) of the inductor is more demanding than its quality factor since the peaking inductor would become a capacitive load as the operating frequency exceeds f_{SR}. The resonant frequency can be viewed as the frequency at which the peak magnetic (E_M) and electric energy (E_E) are equal, and can be determined by $f_{\mathrm{SR}} = (2\pi\sqrt{C_{\mathrm{eq}}L_{\mathrm{eq}}})^{-1}$, where L_{eq} and C_{eq}, respectively, represent the equivalent inductance and capacitance of the inductor [11], [12]. In the following, the C_{eq} of both a planar inductor and our proposed 3-D symmetric transformer are analyzed utilizing a distributed capacitance model, and their f_{SR} comparisons are investigated in detail.

For a given peak voltage of V_0 across the inductor and a stored electric energy of (E_E) in the structure, the equivalent capacitance C_{eq} can be calculated by [11]

$$E_E = \frac{1}{2}C_{\mathrm{eq}}V_o^2. \tag{8}$$

To derive the electric energy stored in the parasitic capacitors of the inductor, the following assumptions are made to simplify the derivations [11]–[13].

1) Voltage distribution is proportional to the length of the metal track.

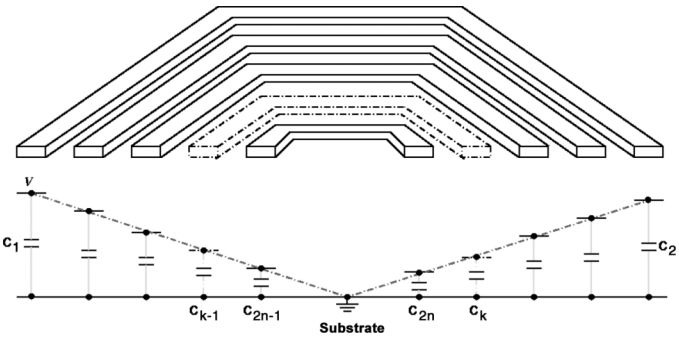


Fig. 3. Cross-sectional view and voltage profile of a planar inductor.

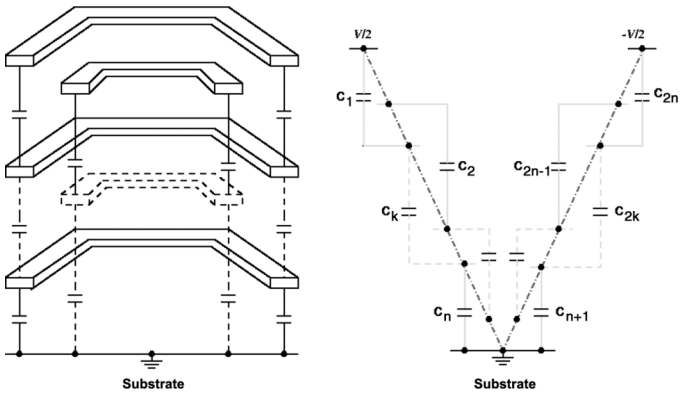


Fig. 4. Cross-sectional view and voltage profile of a 3-D transformer.

2) The voltage potential is equal in half turn of the metal wire in the transformer and is determined by averaging the voltages of the previous half turn and the next one.

Fig. 3 illustrates the cross-sectional view of an n turn planar inductor and its electrical potential distribution. Assume the lengths of each half turn are denoted as $l_1, l_2, \ldots, l_{2n}$, the metal width is W, metal thickness is T, and the total length of the metal wire is $l_T = \sum_{k=1}^{2n} l_k$.

Define $d_k = (1/l_T) \cdot \sum_{i=1}^{k} l_i$, the voltage profile of the inductor can be described as

$$V_k = V_0 \times (1 - d_k). \tag{9}$$

Based on these assumptions, the voltage of the kth half turn can be approximated as

$$V(k) = \frac{1}{2}\left[V_0 \times (1 - d_{k-1}) + V_0 \times (1 - d_k)\right]. \tag{10}$$

Let $C_{\mathrm{mts}}(k)$ denote the unit capacitance of metal k to substrate, the electrical energy stored in the capacitor between the metal layer and the substrate can be expressed as $E_{E1,mts}$, where

$$E_{E1,mts} = \frac{1}{2}\sum_{k=1}^{2n} C_{\mathrm{mts}}(k) \cdot l_k \cdot W \cdot V(k)^2. \tag{11}$$

In addition, let $C_{\mathrm{msm}}(k)$ denote the unit side-wall capacitance between metal k and $k+2$, the electric energy stored in the side-wall parasitic capacitors between the metal layers can be expressed as $E_{E1,mtm}$, where

$$E_{E1,mtm} = \frac{1}{2}\sum_{k=1}^{2n-2} C_{\mathrm{msm}}(k) \cdot l_k \cdot T \cdot \left[V(k) - V(k+2)\right]^2. \tag{12}$$

Combining (11) and (12), the total electric energy $(E_{E1,\mathrm{tot}})$ stored in the structure can be derived as [13]

$$E_{E1,\mathrm{tot}} = E_{E1,mts} + E_{E1,mtm} = \frac{1}{2} C_{\mathrm{eq1}} V_0^2. \tag{13}$$

Thus, the effective parasitic capacitance of a planar inductor can be expressed as C_{eq1}, which is shown here

$$C_{\mathrm{eq1}} \approx \frac{1}{4}\sum_{k=1}^{2n} C_{\mathrm{mts}}(k) \cdot l_k \cdot W \cdot (2 - d_{k-1} - d_k)^2 + \frac{1}{4} \times \sum_{k=1}^{2n-2} C_{\mathrm{msm}}(k) \cdot l_k \cdot T \cdot (d_{k+2} - d_k + d_{k+1} - d_{k-1})^2. \tag{14}$$

On the other hand, the cross-sectional view of an n-turn, single turn per layer, 3-D symmetric transformer and its electrical potential distribution is illustrated in Fig. 4. In case of a differential excitation, the center point of the transformer can be connected to a common mode voltage and ac grounded. The voltage profile of the transformer can be described as

$$V_k = V_0 \times (1/2 - d_k). \tag{15}$$

Also, it can be seen that the metal to substrate capacitors exist in the bottom two metal layers only. Based on the same assumptions previously mentioned, the electrical energy stored in the capacitor between the metal layer and the substrate can be expressed as $E_{E2,mts}$, where

$$E_{E2,mts} = \frac{1}{2}\sum_{k=n-1}^{n+2} C_{\mathrm{mts}}(k) \cdot l_k \cdot W \cdot V(k)^2. \tag{16}$$

On the other hand, since there is only one turn on a metal layer, the side-wall capacitors do not exist. Let $C_{\mathrm{mtm}}(k)$ denote the unit metal to metal overlapped capacitance between metal k and $k+2$, the electrical energy stored in the metal to metal parasitic capacitors can be represented as

$$E_{E2,mtm} = \frac{1}{2}\left[\sum_{k=1}^{n-2} C_{\mathrm{mtm}}(k) \cdot l_k \cdot W \cdot \left[V(k) - V(k+2)\right]^2 + \sum_{k=n+1}^{2n-2} C_{\mathrm{mtm}}(k) \cdot l_k \cdot W \cdot \left[V(k) - V(k+2)\right]^2\right]. \tag{17}$$

By taking both (16) and (17) into account, the total electric energy ($E_{E2,\mathrm{tot}}$) stored in the structure can be derived as [13]

$$E_{E2,\mathrm{tot}} = \frac{1}{2} C_{eq2} V_0^2 = E_{E2,mts} + E_{E2,mtm}. \quad (18)$$

The effective parasitic capacitance of the 3-D transformer can be expressed as C_{eq2}, which is also shown here

$$\begin{aligned} C_{eq2} \approx & \frac{1}{4} \sum_{k=n-1}^{n+2} C_{\mathrm{mts}}(k) \cdot l_k \cdot W \cdot (1 - d_k - d_{k-1})^2 \\ & + \frac{1}{4} \sum_{k=1}^{n-2} C_{\mathrm{mtm}}(k) \cdot l_k \cdot W \\ & \cdot (d_{k+2} - d_k + d_{k+1} - d_{k-1})^2 \\ & + \frac{1}{4} \sum_{k=n+1}^{2n-2} C_{\mathrm{mtm}}(k) \cdot l_k \cdot W \\ & \cdot (d_{k+2} - d_k + d_{k+1} - d_{k-1})^2. \end{aligned} \quad (19)$$

Based on the derived equations in (14) and (19), for an inductor pair with an inductance of 2.85 nH in each branch, five turns, metal width $= 10\ \mu$m, metal spacing $= 1.5\ \mu$m, and an inner diameter of 110 μm, the effective parasitic capacitance of the 3-D transformer (C_{eq2}) is reduced by 45% compared to that of a planar inductor pair (C_{eq1}). The significant improvement is due to the following reasons.

1) The metal to substrate capacitance is minimized and only exists in the bottom two metal layers.
2) The side-wall capacitors are negligible in this architecture, which would become significant in a deep-submicrometer process [13].
3) The metal to metal parasitic capacitances are reduced by increasing the distance between metal plates and minimizing the electrical potential across the top and bottom plates [4].

By EM simulation, the 3-D transformer manifests a higher self resonant frequency (12 GHz versus 9 GHz) compared to its planar counterpart owing to a smaller C_{eq}. Furthermore, the substrate loss of the 3-D transformer is improved by a differential stimulus, and a wider operating bandwidth is achieved in contrast to a single-ended driven counterpart [14]. Most important of all, the chip area of the 3-D transformer is 47% smaller than that of its planar counterparts, which is essential in the multistage broadband amplifier design.

V. Experimental Results

For performance measurement, the receiver IC and a photodetector are mounted on a printed circuit board. The eye diagrams and the bit error rate performance are characterized using Agilent N4901B. The pattern generator sends a $2^{31} - 1$ PRBS test pattern to modulate a commercial 10-Gb/s laser module. With an Oepic-P5030A photodetector, whose responsivity is 1 A/W and parasitic capacitance is about 0.15 pF, the measured sensitivity of the optical receiver AFE at 10 Gb/s is about -13 dBm for a bit error rate of less than 10^{-12}. The bit error rate performance is summarized in Fig. 5. The tolerated power level is up to 0 dBm by the built-in automatic gain control scheme. The

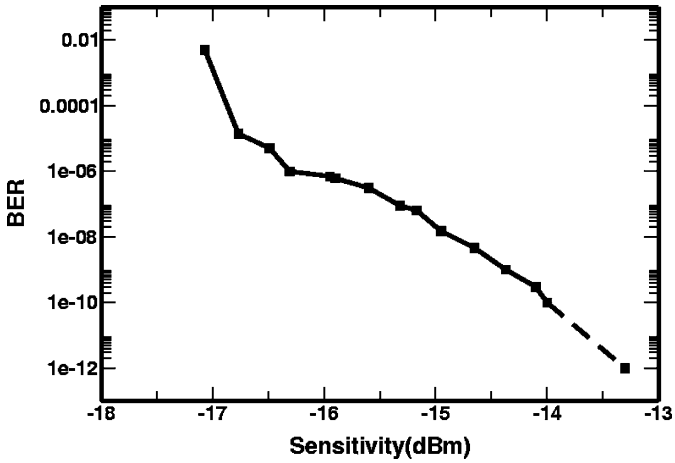


Fig. 5. Measured bit error rate performance of the optical receiver.

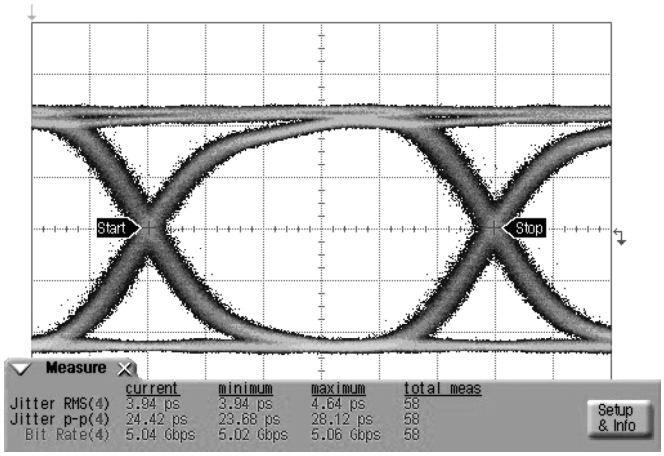


Fig. 6. Measured 5 Gb/s eye diagram with $2^{31} - 1$ PRBS input. (X-axis: 33.3 ps/div, Y-axis: 100 mV/div, $\mathrm{Jitter(pp)} = 24.42$ ps).

input-referred noise current I_N of the optical receiver is derived from its sensitivity performance. As

$$\mathrm{Sensitivity} \approx 10 \log \left[\frac{14.1 I_N (r_e + 1)}{2\rho(r_e - 1)} 1000 \right] \mathrm{dBm} \quad (20)$$

where ρ is the responsivity of the photodetector, and r_e is the extinction ratio. The corresponding I_N is about 6.68 $\mu\mathrm{A_{rms}}$.

Fig. 6 and Fig. 7 illustrate the measured eye diagrams at 5 and 7 Gb/s, respectively, at sensitivity level. The data jitter is about 3.94 $\mathrm{ps_{rms}}$ (24.4 $\mathrm{ps_{pp}}$) and 3.96 $\mathrm{ps_{rms}}$ (30.9 $\mathrm{ps_{pp}}$). Fig. 8(a) illustrates the measured 10 Gb/s eye diagram at the input power of sensitivity level (-13 dBm), and Fig. 8(b) illustrates the measured 10 Gb/s eye diagram when the input power is overloaded. The measured jitters are about 4.95 $\mathrm{ps_{rms}}$ (30.96 $\mathrm{ps_{pp}}$) and 5.67 $\mathrm{ps_{rms}}$ (36.27 $\mathrm{ps_{pp}}$). Fig. 9(a) illustrates the simulated conversion gain of the receiver AFE and the TIA, and the frequency response of the PA, including the voltage amplifier and the slicer, is shown in Fig. 9(b).

In summary, the receiver front-end provides a conversion gain of 90 dBΩ, among which 50 dBΩ is provided by the TIA. It is capable of delivering 900 $\mathrm{mV_{pp}}$ differential voltage swings to 50 Ω output loads directly. The $f_{H-3\,\mathrm{dB}}$ is about 7.86 GHz,

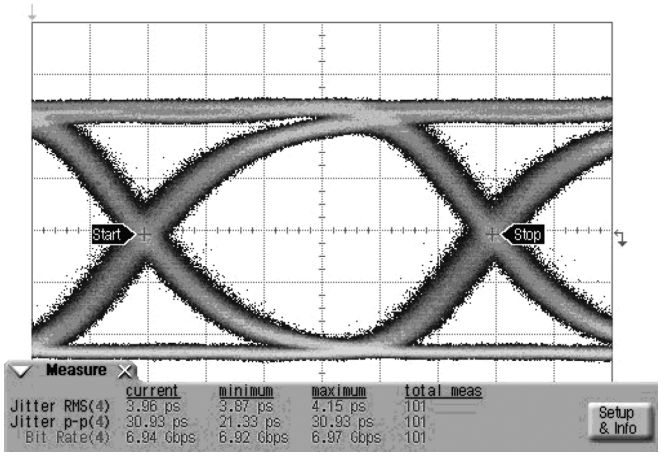
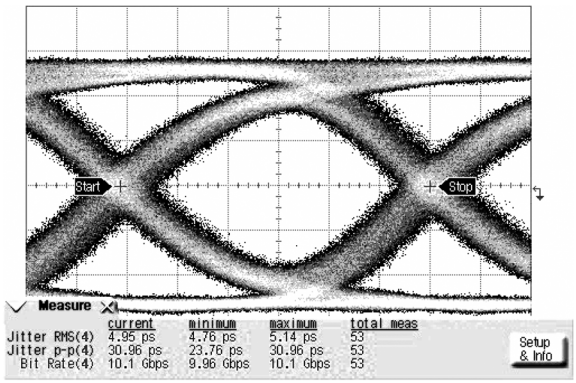
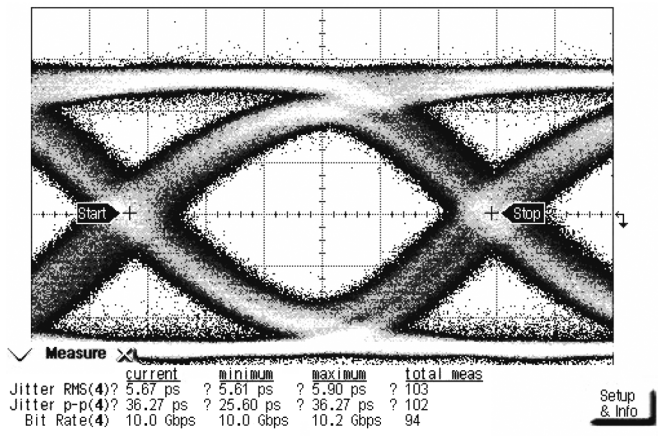


Fig. 7. Measured 7 Gb/s eye diagram with $2^{31} - 1$ PRBS input. (X-axis: 24 ps/div, Y-axis: 97.3 mV/div, $\mathrm{Jitter(pp)} = 30.93$ ps).

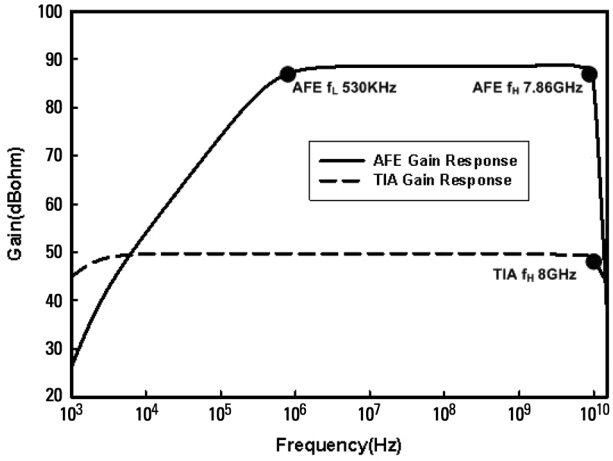


(a)

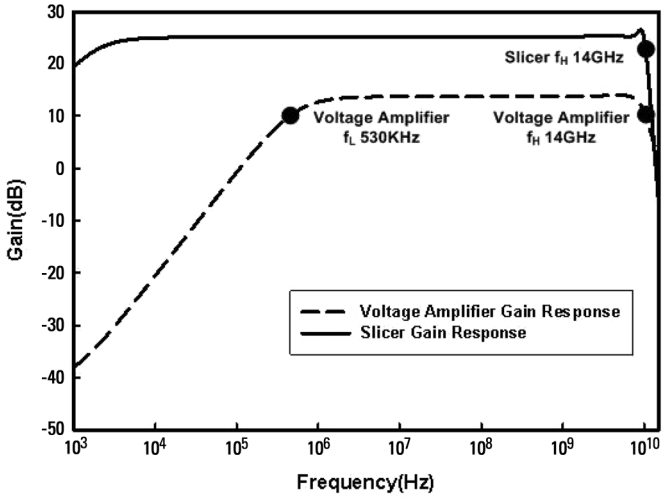


(b)

Fig. 8. Measured 10 Gb/s eye diagram with $2^{31} - 1$ PRBS input. (a) Input power $= -13$ dBm. (b) Input power $= 0$ dBm (X-axis: 16 ps/div, Y-axis: 100 mV/div).



(a)



(b)

Fig. 9. (a) Simulated frequency response of the optical receiver analog front-end. (b) Simulated frequency response of the post voltage amplifier.

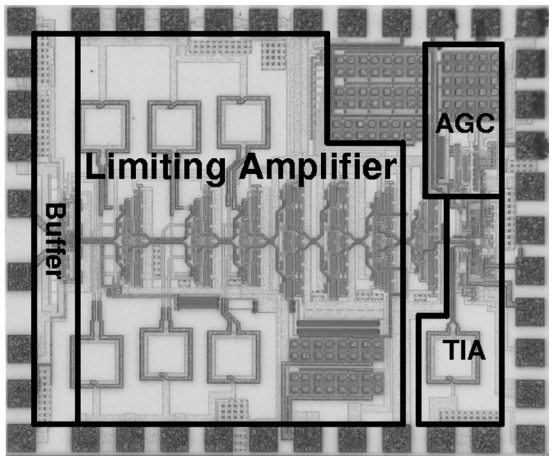


Fig. 10. Chip photograph.

which is limited by the transimpedance amplifier. The PA exhibits a conversion gain of 40 dB. The voltage amplifier provides a 16-dB conversion gain to fully switch the slicer. As a tapered buffer, the slicing stage further provides 24-dB voltage gain. The tolerated power level is up to 0 dBm by the built in automatic gain control scheme. Operating under a 1.8-V supply, the power dissipation is 199 mW, among which 35 mW is consumed by the output buffer. Fig. 10 illustrates the chip photo. Fabricated in a 0.18-μm CMOS technology, the chip size is 1300 μm $\times$ 1566 μm.

TABLE I
PERFORMANCE BENCHMARK

	This work	[1] 02' RFIC	[2] 03' ISSCC	[3] 02' ESSCIRC	[7] 05' JSSC	[16] 00' JSSC	[18] 04' ISSCC
Function	TIA+AGC+LA single chip	TIA and LA chip sets	LA	TIA	TIA+AGC+LA Single chip	LA	Amplifier
Power	199 mW (1.8V)	TIA 108 mW LA 360mW (1.8V)	150 mW (1.8V)	137.5 mW (2.5V)	210 mW (1.8V)	53mW (2.5V)	190mW (2.2V)
CMOS Process	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.25 μm	0.18 μm
Inductor Counts	7	N.A.	24	2	9	0	20
GBW	248.5 THz-Ω	(TIA) 11.7 THz-Ω (LA) 1.19 THz	2.97 THz	4.6 THz-Ω	135 THz-Ω	0.119 THz	0.123 THz

VI. CONCLUSION

This paper describes the design of a 10-Gb/s optical receiver analog front-end in a generic 0.18-μm CMOS technology. The optical AFE provides a conversion gain of 90 dBΩ and a -3 dB bandwidth of about 7.86 GHz, which is limited by the transimpedance amplifier. A regulated cascode input stage is utilized to decouple the loading effect at the input node, and wide bandwidth is achieved by means of shunt feedback and inductive peaking. The PA is composed of a preamplification stage followed by a slicing stage. In contrast to a conventional limiting amplifier which consists of identical gain cells, the GBW requirements in the proposed topology are much relaxed, thus, both peaking inductors and power consumption can be saved. Moreover, an AGC is built in to alleviate overload induced data jitter. Instead of using bulky planar inductors or two asymmertric 3-D inductors, a novel fully symmetric 3-D transformer for inductive peaking is utilized in this design to save chip area. A distributed capacitance model of the 3-D transformer is also proposed. The superiority of the proposed transformer over conventional planar counterpart is demonstrated.

The performance benchmark of this paper, our previous work in [7], and the prior art of TIA and limiting amplifiers [1]–[3], [7], [16], [18] is summarized in Table I. By a single chip integration, gain-bandwidth requirement for the individual building blocks can be rearranged and further optimized. The proposed prototype is power efficient, manifests a GBW as high as 248.5 THz-Ω, while fewer peaking inductors are required.

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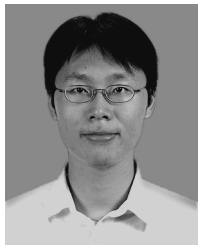

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