Impacts of SiN-Capping Layer on the Device Characteristics and Hot-Carrier Degradation of nMOSFETs

Chia-Yu Lu, Horng-Chih Lin, *Senior Member, IEEE*, Yao-Jen Lee, Yu-Lin Shie, and Chih-Cheng Chao

***Abstract*—Impacts of silicon nitride (SiN)-capping layer and the associated deposition process on the device characteristics and hot-electron degradation of nMOSFETs are investigated in this paper. The SiN layer used to induce channel strain for mobility enhancement was deposited by a low-pressure chemical vapor deposition. The deposition of the SiN aggravates threshold-voltage roll-off due to additional thermal budget and the strain effect. It is also found that the device hot-electron degradation is worse with the addition of the SiN capping. Furthermore, our results indicate that both the bandgap narrowing caused by the channel strain and the abundant hydrogen species from the precursors of SiN deposition contribute to the aggravated hot-electron effect.**

***Index Terms*—Hot-electron effect, low-pressure chemical vapor deposition (LPCVD), nMOSFET, silicon nitride (SiN) capping, tensile strain.**

I. Introduction

RECENTLY, strain engineering in the channel has emerged as one of the most effective remedies to boost the drive current in the scaled devices [1]–[5]. For example, a silicon nitride (SiN)-capping layer deposited by the low-pressure chemical vapor deposition (LPCVD) over the gate was shown to induce a uniaxial tensile strain in the channel which is beneficial for boosting the drive current in scaled nMOSFETs [2]–[4]. The above approach is attractive since it can be incorporated seamlessly in state-of-the-art ULSI technology, and it has received many attentions in the last few years.

Device degradation induced by hot electrons represents one of the most critical reliability issues in deep submicrometer nMOSFETs [6], [7]. The physical mechanisms and characteristics of hot-electron degradation have been extensively examined [8], [9]. The degradations in terms of threshold-voltage shift (ΔV_{th}), drain–current degradation (ΔI_{DS}), and transconductance degradation (ΔG_m) are observed in the accelerated stress test. However, there seem very few works that investigate the impact of SiN-capping layer and the associated deposition process on the hot-carrier reliability of the strained devices. In this paper, we investigate detailed hot-carrier degradation characteristics of NMOS devices having local channel strain induced by the SiN-capping layer.

Manuscript received November 17, 2005; revised September 9, 2006. This work was supported in part by the National Science Council under Contract NSC 94-2215-E-009-065.

C.-Y. Lu was with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. He is now with the Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan, R.O.C.

H.-C. Lin was with National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C. He is now with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

Y.-J. Lee is with National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C.

Y.-L. Shie was with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. He is now is with the Innolux Corporation, Chuna, Taiwan, R.O.C.

C.-C. Chao was with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

Digital Object Identifier 10.1109/TDMR.2006.889268

II. Experiments

The nMOSFET used in this paper were with 2.5-nm thermal oxide as the gate dielectric and 150-nm poly-Si layer as the gate material. After the gate formation, most samples were capped with a 300-nm SiN-capping layer deposited using an LPCVD system, while some wafers were deliberately skipped of the SiN-capping layer to serve as the controls (i.e., control split). The SiN deposition was performed at 780 °C with SiH_2Cl_2 and NH_3 as the reaction precursors. For some samples that received the SiN-capping-layer deposition, the SiN layer was removed later in order to evaluate the impact of SiN deposition (i.e., SiN-removal split). Wafers then received the deposition of a 300-nm-thick TEOS passivation layer, followed by contact holes and metallization processes. Finally, the processing steps were completed with a forming gas anneal at 400 °C. Electrical characterizations were performed using an HP4156 system. The interface traps were evaluated using the charge-pumping method [10], [11] with a fixed amplitude of 1.5 V at 1 MHz.

III. Results and Discussion

A. Effects of Channel Strain on Device Performance

Fig. 1 shows the percentage increase of the drive current of the SiN-capped and SiN-removal samples compared to the controls as a function of channel length. Significant drive-current enhancement is observed for the device with SiN-capping layer. We can see that the drive-current enhancement reaches 21% at a channel length of 0.4 μm in the SiN-capped samples. For the SiN-removal split, it is seen that the current enhancement becomes negligible, confirming that the origin of the current enhancement indeed arises from the stress of the SiN-capping layer. Hence, the current enhancement is truly due to the uniaxial tensile strain induced by the SiN capping which increases with decreasing channel length [3], [4].

1530-4388/$25.00 © 2007 IEEE

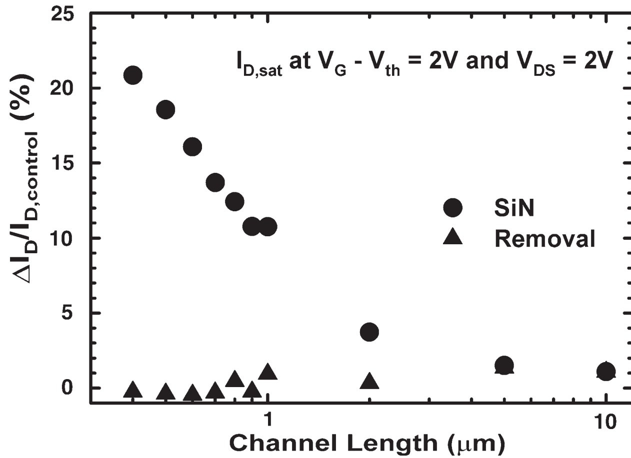


Fig. 1. Saturation current increase versus channel length. The saturation current was defined at $V_G - V_{\rm th} = 2$ V and $V_{\rm DS} = 2$ V.

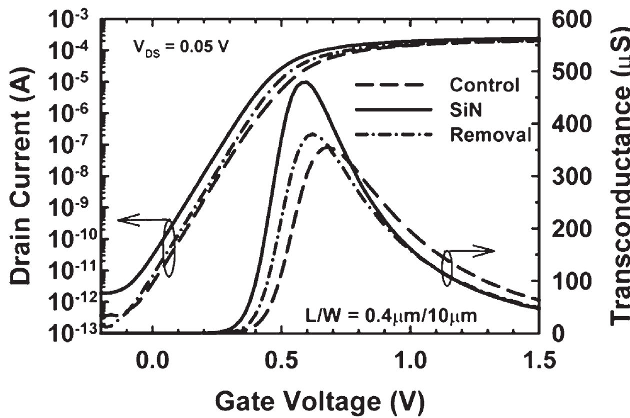


Fig. 2. nMOSFET subthreshold characteristics and transconductance for all three splits.

Subthreshold characteristics of the same devices are shown in Fig. 2. The aforementioned impact of SiN on current enhancement also reflects on the results of transconductance. The SiN-removal sample shows slightly higher transconductance than the control counterpart, mainly due to the reduced interface state density that will be addressed in more detail later. Nevertheless, the subthreshold slope of the devices does not seem to be affected by the SiN capping, as shown in Fig. 2.

B. Short-Channel Effects

Fig. 3 shows the threshold-voltage $(V_{\rm th})$ roll-off characteristics of the devices. The results are obtained at $V_{\rm DS} = 0.05$ V. Among the three splits of devices, the control samples depict a pronounced reverse short-channel effect (RSCE). This is ascribed to the nonuniform lateral boron distribution in the channel. It was pointed out that the lateral boron distribution is closely related to the S/D implant damage and the associated postanneal steps [12]. Boron segregation occurs and results in a peak distribution at the channel edge if the channel defects are not properly annealed out. This leads to the observed RSCE in the control split. The phenomenon, however, is greatly suppressed for the other two splits. Additional thermal budget introduced by the SiN deposition step helps eliminate the channel defects and redistribute the B dopants [12], explaining the suppression of the RSCE. Another interesting trend shown in Fig. 3 is that the prominent $V_{\rm th}$ roll-off behavior for the SiN-capped devices is relaxed by the removal of the SiN layer. We believe this is related to the bandgap narrowing effect caused by the channel strain [13], [14]. In our case, the induced tensile strain tends to lift the two- and fourfold degeneracy of the conduction band and leads to a smaller bandgap due to the lowering in the twofold band edge. The extent of bandgap narrowing as a function of the induced unaxial strain could be found in a previous work [14, Fig. 10]. Since the strain level increases with a decreasing channel length, the bandgap narrowing contributes to the aggravated $V_{\rm th}$ roll-off in the short-channel SiN-capped devices. In the SiN-removal split, since the strain effect is eliminated, the $V_{\rm th}$ roll-of becomes relaxed.

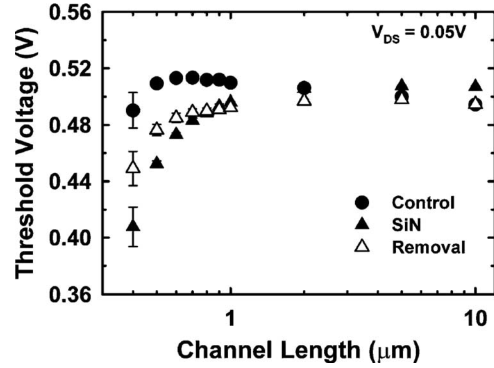


Fig. 3. Threshold voltage as a function of channel length for all three splits.

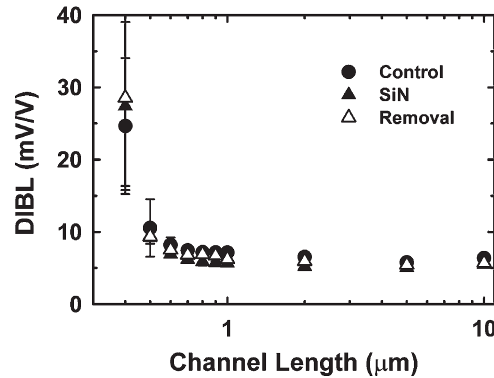


Fig. 4. DIBL in all three splits as a function of channel length. DIBL was evaluated by measuring the drain–current change as $V_{\rm DS}$ is increased at some fixed gate voltage below threshold voltage.

Drain induced barrier lowing (DIBL) is another guide for evaluating the short-channel effects. The results are shown in Fig. 4. We can see that basically no obvious difference is observed among all samples. This indicates that the use of SiN-capping would not complicate the DIBL control of the devices.

C. Hot-Carrier Effects

Next, we shift our focus to the hot-carrier reliability. The substrate current of the fabricated devices with various channel lengths are shown and compared in Fig. 5. It is clearly seen that with reducing channel length, the substrate current is much larger in the SiN-capped device, as compared with the other

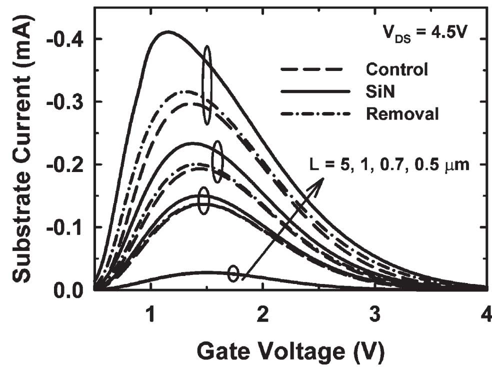


Fig. 5. Substrate current versus gate voltage with channel lengths of 0.5, 0.7, 1, and 5 μm.

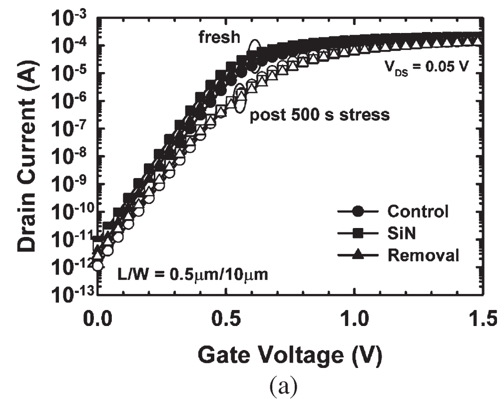
two splits (for example, more than 0.1-mA increase at the channel length of 0.5 μm). The difference in substrate current among different splits becomes negligible for the long-channel case (e.g., $L = 5$ μm). This result indicates that the channel strain plays an important role in affecting the generation of channel hot electrons and the associated impact ionization process. This is related to the bandgap narrowing effect induced by the channel strain as well as the increased mobility, both tend to enhance the impact ionization rate [15], [16], and may potentially worsen the hot-electron degradation in the strained devices. An empirical expression [17] for the substrate current is

$$I_{\text{sub}} \propto \exp\left(\frac{-\varphi_i}{q\lambda E}\right) \quad (1)$$

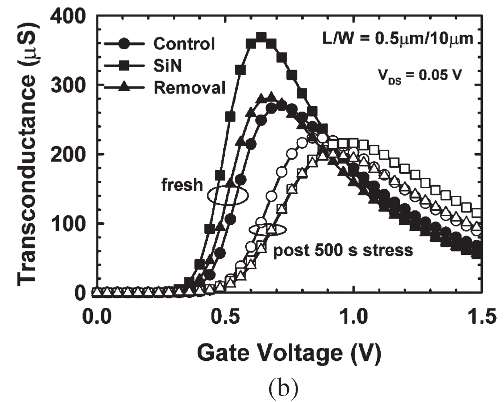
where λ is the mean-free path of the electrons and E is the electric field. φ_i is the threshold energy to cause impact ionization in the channel, which is shown to be about the magnitude of the bandgap [18]. Therefore, the bandgap narrowing will result in an increased I_{sub}, as observed in the experimental data.

In Fig. 5, it is also interesting to note that the substrate current in the SiN-removal samples is slightly larger than the control counterparts when the channel length is short. This is attributed to the additional thermal budget by the SiN deposition process that tends to reduce the residual implant damage located in the channel close to the drain region, as mentioned in previous section. It is expected that the residual implant damage sites scatter the conduction electrons. The scattering processes reduce the energy of the electrons and relax the generation of hot carriers; therefore, the impact ionization ratio (and thus the substrate current) is reduced. When the thermal budget associated with the SiN deposition is performed, portion of the residual implant damage is annealed out, leading to a slight increase in I_{sub} in short-channel devices. However, the amount of the residual implant damage is not sufficiently high to draw significant impact on the devices' drive current, explaining why the drive current is comparable between the control and the SiN-removal devices.

Typical results of hot-electron stressing for the three splits of samples are shown in Fig. 6. Channel length and width of the test devices are 0.5 and 10 μm, respectively. The devices were stressed at $V_{\text{DS}} = 4.5$ V and V_{GS} at maximum substrate current. The I_D–V_G characteristics at $V_{\text{DS}} = 0.05$ V were measured



(a)



(b)

Fig. 6. (a) Subthreshold characteristics and (b) transconductance of devices before and after 5000-s hot-electron stressing. Channel length/width = 0.5 μm/10 μm.

before and after the stress to check the degradation caused by the hot electrons. As can be seen in Fig. 6, the degradation is the worst in the SiN-capped sample among the three splits. The aggravation is alleviated with SiN removal, although the resultant degradation is still worse than the control sample.

Fig. 7 shows the shift of the threshold voltage (ΔV_{th}), increased interface state density (ΔN_{it}), and degraded peak transconductance (ΔG_{m}) as a function of the stress time. The device with channel strain depicts aggravated degradation in terms of larger shifts in these parameters. As mentioned above, the bandgap narrowing effect and the increased carrier mobility in the strained channel devices [19], [20] are postulated to be the two primarily culprits for the aggravated hot-carrier degradation of the SiN-capped samples. These two factors would increase the impact ionization rate in the device, which is evidenced in Fig. 5, and lead to higher degradation.

In Figs. 6 and 7, it is noted that the device with SiN removal also depicts more severe degradation than the control device, even though the channel strain has been eliminated. This phenomenon clearly indicates that the SiN deposition process itself results in the enhanced damage effect in the short-channel devices. According to previous reports [17], [19], interface states could be generated due to the breaking of Si–H bonds by hot electrons, and the generated interface states would greatly degrade the device performance. Fig. 8 shows the hot-carrier degradation as a function of injection charges, which is defined as the product of maximum substrate current and stress time. In the figures, it is seen that the SiN-capping and

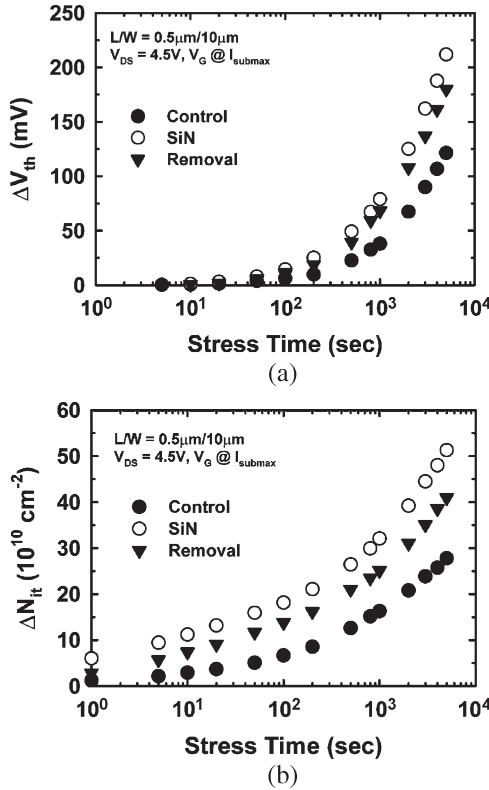


Fig. 7. Results of hot-electron stressing at $V_{\rm DS} = 4.5$ V and maximum substrate current performed on all three splits of devices with channel length/width $= 0.5\ \mu$m/10 μm. (a) Threshold-voltage shift and (b) interface state generation.

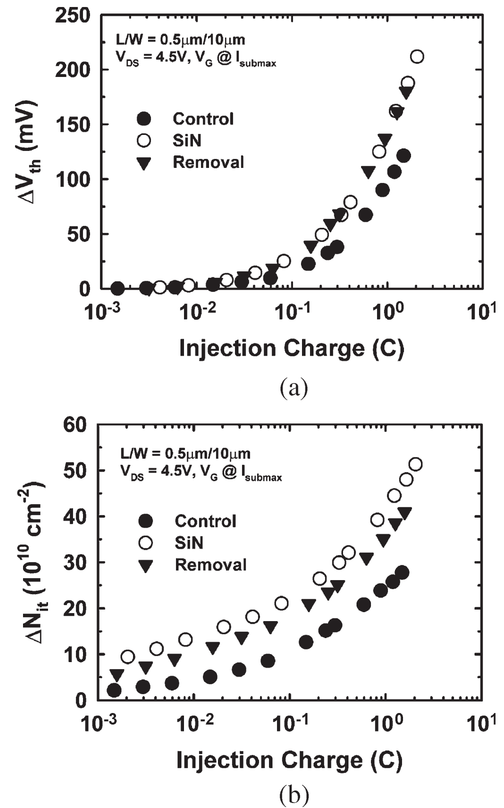


Fig. 8. (a) Threshold-voltage shift and (b) interface state generation as a function of injection charges (the product of maximum substrate current and stress time) under hot-electron stressing at $V_{\rm DS} = 4.5$ V.

removal samples exhibit nearly identical degradation trends which are obviously severer than the control one, implying that the properties of oxide/channel interface for the SiN-capping and removal splits are similar, but quite different from the control. This is basically consistent with our inference that the hydrogen species diffuse from SiN during the deposition step may have modified the oxide/channel interface, leading to the worse hot-carrier degradation.

Fig. 9 shows the charge-pumping current of fresh devices. Actually, SiN-removal sample depicts the smallest charge-pumping current ($I_{\rm cp}$) among the three splits of samples. This is ascribed to the use of H-containing precursors (e.g., SiH_2Cl_2 and NH_3) in the SiN deposition step, and the incorporated hydrogen species tends to passivate the interface states. As a result, lower charge-pumping current is obtained for the SiN-removal sample in Fig. 9. Note that such reduction in interface states comparing to the control sample is not observed for the strained devices. The origin for the higher interface state density in the fresh SiN-capped devices is not clear at this stage, although it is highly suspected that more weaken bonds due to the induced strain exist at the interface. These bonds are easily broken and contribute to the excess interface states. It should also be noted that due to the thin oxide thickness (3 nm), the difference in interface states among the three splits will not result in significantly different subthreshold swing characteristics of the devices shown in Fig. 2.

Although the additional H species incorporated in the SiN-removal device could reduce the interface state density in fresh devices, the extra Si–H bonds would also be responsible for the worse hot-carrier degradation shown in Figs. 6 and 7. Fig. 10 shows the difference in $N_{\rm it}$ before and after 5000-s hot-carrier stress among the three splits of samples. It is seen that more interface states than those in the control sample are actually generated in the SiN-removal devices, again implying that the extra hydrogen species from SiN layer are an important contributor for the aggravated degradation.

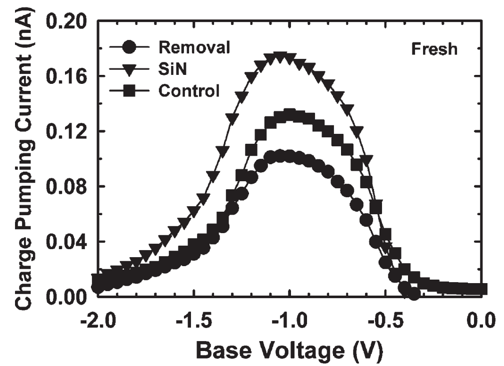


Fig. 9. Charge-pumping current for the three splits of fresh devices with channel length/width $= 0.5\ \mu$m/10 μm. The measurement was performed under fixed amplitude of 1.5 V and frequency of 1 MHz.

Fig. 11 shows the relationship between $\Delta N_{\rm it}$ and $C_{\rm ox}\Delta V_{\rm th}/q$, where $C_{\rm ox}$ is the oxide capacitance per unit area and q is 1.6×10^{-19} Coulomb. It is interesting to see that the value of $\Delta N_{\rm it}$ is higher than the diagonal line (i.e., the solid line

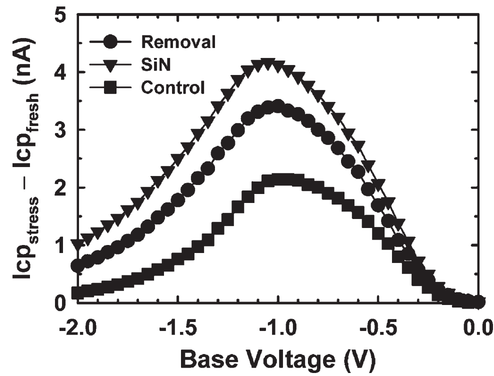


Fig. 10. Increase in charge-pumping current after the stress for the three splits of devices with channel length/width $= 0.5\ \mu\text{m}/10\ \mu\text{m}$.

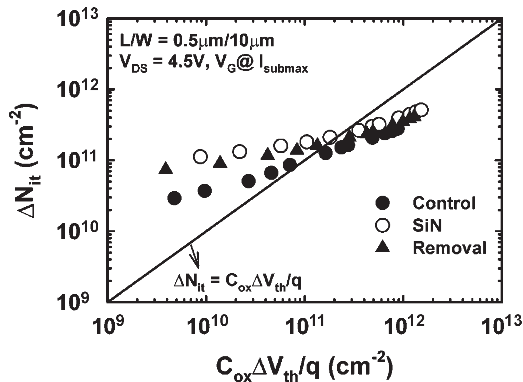


Fig. 11. Generated interface states versus $C_{\rm ox}\Delta V_{\rm th}/q$ during hot-carrier stressing.

in the figure with slope of one) at the early stage of the stress, indicating that positive charges are generated. The generation of positive charges is related to the high oxide field during hot-carrier stressing, and it is attributed to the release of hydrogen at the interface [21]. Since the SiN deposition process introduces extra hydrogen incorporation in the oxide, the amount of the generated positive charges is larger for the SiN-capped and SiN-removal splits. When the stressing proceeds for a sufficiently long time, electron trapping gradually dominates and contributes to the $V_{\rm th}$ shift, as shown in the figure.

Based on the above results, we conclude that both the deposited SiN layer and the deposition process itself have significant impacts on the device operation and the associated reliability characteristics. For threshold-voltage control, not only the bandgap narrowing effect induced by the channel strain but also the thermal treatment associated with the SiN deposition need to be taken into account. Impurities contained in the SiN layer should also be carefully addressed. This paper shows that hot-electron degradation is negatively affected when the SiN is deposited over the gate, even if the SiN is removed later and the channel strain is relieved. The existence of extra Si–H bonds at the oxide/Si interface due to the deposition of SiN is presumably the main cause for this observation. Optimization of the deposition is thus necessary for improving the immunity of the strained devices to the hot-carrier effect. For example, using deuterium-containing precursors or deuterium annealing process [22] could be helpful in this regard.

IV. Conclusion

In this paper, we investigate the effects of LPCVD SiN process and the channel strain induced by the SiN-capping layer on the device characteristics as well as the hot-electron degradation of the nMOSFETs. The results indicate that the thermal budget associated with the deposition of the SiN-capping layer could alleviate the RSCE of the uncapped devices. The bandgap narrowing effect due to the channel strain may result in further lowering in $V_{\rm th}$ as the channel length is shortened.

The channel strain induced by the SiN-capping layer over the gate greatly boosts the drive current of short-channel devices. For example, enhancement ratio as high as 21% is achieved for the SiN-capped device at a channel length of 0.4 μm. Nevertheless, the accompanying bandgap narrowing and the increased carrier mobility tend to worsen the hot-electron reliability. In this aspect, attention should also be paid to the SiN deposition. Owing to the use of hydrogen-containing precursors, abundant hydrogen species is incorporated in the oxide that may also contribute to the hot-electron degradation. Optimization of both SiN deposition process and the film properties are thus essential for implementation of the uniaxial strain in NMOS devices.

Acknowledgment

The authors would like to thank the National Nano Device Laboratories (NDL) for assistance in device fabrication.

References

[1] F. Ootsuka, S. Wakahara, K. Ichinose, A. Honzawa, S. Wada, H. Sato, T. Ando, H. Ohta, K. Watanabe, and T. Onai, “A highly dense, high-performance 130 nm node CMOS technology for large scale system-on-a-chip applications,” in *IEDM Tech. Dig.*, 2000, pp. 575–578.

[2] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, “A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors,” in *IEDM Tech. Dig.*, 2003, pp. 978–980.

[3] S. Pidin, T. Mori, K. Inoue, S. Fukuta, N. Itoh, E. Mutoh, K. Ohkoshi, R. Nakamura, K. Kobayashi, K. Kawamura, T. Saiki, S. Fukuyama, S. Satoh, M. Kase, and K. Hashimoto, “A novel strain enhanced CMOS architecture using selectively deposited high tensile and high compressive silicon nitride films,” in *IEDM Tech. Dig.*, 2004, pp. 213–216.

[4] K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, T. Hoffmann, A. Murthy, J. Sandford, R. Shaheed, K. Zawadzki, K. Zhang, S. Thompson, and M. Bohr, “Delaying forever: Uniaxial strained silicon transistors in a 90 nm CMOS technology,” in *Proc. Symp. VLSI Technol. Dig. Tech. Papers*, 2004, pp. 50–51.

[5] C. Y. Lu, H. C. Lin, Y. F. Chang, and T. Y. Huang, “Devices characteristics and aggravated negative bias temperature instability in pMOSFETs with uniaxial compressive strain,” *Jpn. J. Appl. Phys.*, vol. 45, no. 4B, pp. 3064–3069, Apr. 2006.

[6] E. Li, E. Rosenbaum, J. Tao, and P. Fang, “Projecting lifetime of deep submicron MOSFETs,” *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 671–678, Apr. 2001.

[7] H. S. Momose, S. Nakamura, T. Ohguro, T. Yoshitomi, E. Morifuji, T. Morimoto, Y. Katsumata, and H. Iwai, “A study of hot-carrier degradation in n- and p-MOSFETs with ultra-thin gate oxides in the direct-tunneling regime,” in *IEDM Tech. Dig.*, 1997, pp. 453–456.

[8] A. Schwerin, W. Hansch, and W. Weber, “The relationship between oxide charge and device degradation: A comparative study of n- and p-channel MOSFET’s,” *IEEE Trans. Electron Devices*, vol. ED-34, no. 12, pp. 2493–2500, Dec. 1987.

[9] P. Heremans, R. Bellens, G. Groeseneken, and H. Maes, “Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFETs,” *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 2194–2209, Dec. 1988.

[10] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-31, no. 1, pp. 42–53, Jan. 1984.

[11] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation," *IEEE Trans. Electron Devices*, vol. 36, no. 7, pp. 1318–1335, Jul. 1989.

[12] H. I. Hanafi, W. P. Noble, R. S. Bass, K. Varahramyan, Y. Lii, and A. J. Dally, "A model for anomalous short-channel behavior in submicron MOSFETs," *IEEE Electron Device Lett.*, vol. 14, no. 12, pp. 575–577, Dec. 1993.

[13] J.-S. Goo, Q. Xiang, Y. Takamura, F. Arasnia, E. N. Paton, P. Besser, J. Pan, and M.-R. Lin, "Band offset induced threshold variation in strained-Si nMOSFETs," *IEEE Electron Device Lett.*, vol. 24, no. 9, pp. 568–570, Sep. 2003.

[14] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs," in *IEDM Tech. Dig.*, 2004, pp. 221–224.

[15] J. E. Chung, P.-K. Ko, and C. Hu, "A model for hot-electron-induced MOSFET linear-current degradation based on mobility reduction due to interface-state generation," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1362–1370, Jun. 1991.

[16] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation," *IEEE Trans. Electron Devices*, vol. 36, no. 7, pp. 1318–1335, Jul. 1989.

[17] C. Hu, S. C. Tam, F.-C. Hsu, P.-K. Ko, T.-Y. Chan, and K. W. Terrill, "Hot-electron-induced MOSFET degradation—Model, monitor, and improvement," *IEEE Trans. Electron Devices*, vol. ED-32, no. 2, pp. 375–385, Feb. 1985.

[18] K. Yeom, J. M. Hinckley, and J. Singh, "Theoretical study on threshold energy and impact ionization coefficient for electrons in $Si_{1-x}Ge_x$," *Appl. Phys. Lett.*, vol. 64, no. 22, pp. 2985–2987, 1994.

[19] N. Sano, M. Tomizawa, and A. Yoshii, "Temperature dependence of hot carrier effects in short-channel Si-MOSFETs," *IEEE Trans. Electron Devices*, vol. 42, no. 12, pp. 2211–2216, Dec. 1995.

[20] M. F. Lu, S. Chiang, A. Liu, S. H. Lu, M. S. Yeh, J. R. Hwang, T. H. Tang, W. T. Shiau, M. C. Chen, and T. Wang, "Hot carrier degradation in novel strained-Si nMOSFETs," in *Proc. Int. Rel. Phys. Symp.*, 2004, pp. 18–22.

[21] D. J. DiMaria, E. Cartier, and D. A. Buchanan, "Anode hole injection and trapping in silicon dioxide," *J. Appl. Phys.*, vol. 80, no. 1, pp. 304–317, Jul. 1996.

[22] I. C. Kizilyalli, J. W. Lyding, and K. Hess, "Deuterium post-metal annealing of MOSFET's for improved hot carrier reliability," *IEEE Electron Device Lett.*, vol. 18, no. 3, pp. 81–83, Mar. 1997.

Chia-Yu Lu was born in Pingtung, Taiwan, R.O.C., on August 1, 1977. He received the B.S. degree in electrical engineering from Chang-Gung University, Taoyuan, Taiwan, R.O.C., in 1999, and the M.S. and Ph.D. degrees from Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 2001 and 2006, respectively.

Currently, he is with the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, R.O.C., as a Device Engineer. His research interests are in the reliability characteristics of local-strained MOSFET, devices process, and characterization of deep submicrometer CMOS devices.

Horng-Chih Lin (S'90–M'95–SM'01) was born in I-Lan, Taiwan, R.O.C., on August 1, 1967. He received the B.S. degree in physics from National Central University, Chung-Li, Taiwan, R.O.C., in 1989, and the Ph.D. degree from Institute of Electronics, National Chiao Tung University (NCTU), Hsinchu, Taiwan, R.O.C., in 1994.

From 1994 to 2004, he was with the National Nano Device Laboratories (NDL), where he was engaged in the research projects of nanoscale device technology development. He joined the faculty of NCTU, Hsinchu, Taiwan, R.O.C., in 2004, where he is currently an Associate Professor with the Department of Electronics Engineering and the Institute of Electronics. His current research interests include thin-film transistor (TFT) fabrication and characterization, reliability of CMOS devices, and novel SOI device technology. He has authored or coauthored over 100 technical papers in international journals and conferences in the above areas.

Dr. Lin served on the Program Committee of the International Reliability Physics Symposium (IRPS) in 2001 and 2002. He also served on the Program Committee of the International Conference on Solid State Devices and Materials (SSDM) in 2005 and 2006.

Yao-Jen Lee was born in Kaohsiung, Taiwan, R.O.C., on January 25, 1976. He received the B.S. degree in electrical engineering from National Chung-Hsing University, Taichung, Taiwan, R.O.C., in 1998, and the M.S. and Ph.D. degrees from the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 2000 and 2004, respectively.

He joined the National Nano Device Laboratories, Hsinchu, Taiwan, R.O.C., as an Associate Researcher. His research interests are in the reliability characteristics of local-strained MOSFET, NBTI, DTMOS, and characterization of deep submicrometer CMOS devices.

Yu-Lin Shie was born in Changhua, Taiwan, R.O.C., on July 22, 1982. He received the B.S. degree in physics from Chung-Hsing University, Taichung, Taiwan, R.O.C., in 2004, and the M.S. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 2006.

Currently, he is with the Innolux Corporation, Chuna, Taiwan, R.O.C., as a Device Engineer.

Chih-Cheng Chao was born in Taichung, Taiwan, R.O.C., on March 15, 1982. He received the B.S. and M.S. degrees from National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 2004 and 2006, respectively, both in electronics engineering.