Improved Performance of F-Ions-Implanted Poly-Si Thin-Film Transistors Using Solid Phase Crystallization and Excimer Laser Crystallization

Chun-Hao Tu, Ting-Chang Chang, Po-Tsun Liu, Che-Yu Yang, *Student Member, IEEE*, Li-Wei Feng, Chia-Chou Tsai, Li-Ting Chang, Yung-Chun Wu, Simon M. Sze, *Life Fellow, IEEE*, and Chun-Yen Chang, *Life Fellow, IEEE*

***Abstract*—Polycrystalline silicon thin-film transistors (Poly-Si TFTs) with F-ions-implantation were investigated in this study. The electrical characteristics and reliability of the F-ions-implanted poly-Si TFTs were reported for solid phase crystallization (*SPC*) and excimer laser crystallization (*ELC*) methods respectively. The thermal annealing causes F-ions to pile up at the poly-Si interface, without the initial pad oxide deposition. With the introduction of fluorine in poly-Si film, the trap state density was effectively reduced. Also, the presence of strong Si-F bonds enhances electrical endurance against hot carrier impact by using F-ions-implantation. These improvements in electrical characteristics are even obvious for the ELC poly-Si TFTs compared to the SPC ones.**

***Index Terms*—Excimer laser crystallization (*ELC*), F-ions implant, polycrystalline silicon thin-film transistors (poly-Si TFTs), SPC.**

I. INTRODUCTION

In RECENT YEARS, the polycrystalline silicon thin-film transistors (poly-Si TFTs) were widely used in many application, especially for active-matrix liquid phase crystal displays (AMLCDs) [1], [2]. The major attraction of the poly-Si TFTs in AMLCDs lies in the significantly improved carrier mobility, as well as the ability to integrate the pixel switching elements, panel array, and peripheral driving circuit on the same substrate [3]–[5]. Low temperature technology is required to realize commercial flat plane display (FPD) on inexpensive glass substrate when fabricating high performance poly-Si TFTs, since the maximum process temperature is limited to less than 600 °C. The solid phase crystallization (***SPC***) and excimer laser crystallization (***ELC***) methods were widely used to recrystallize amorphous silicon (a-Si) to poly-Si at low temperature fabrication process. The *SPC* process, requiring 24–48 h, is a time consuming procedure, which obviously affects the throughput and thermal budget of fabrication processes [6]. Furthermore, the resultant lower field effect mobility will limit the development for *SPC* poly-Si TFTs for small grain size. The excimer laser system can create larger grain size and little intra-grain defect than using conventional *SPC* method [7], [8]. Furthermore, the laser annealing process is not a high temperature fabrication and a rapid process. Hence, the laser annealing system is generally applied in flat plant display application. However, the difference of thermal expansion coefficient for molten poly-Si and buffer oxide causes serious mechanical stress during the *ELC* thermal annealing process.

The off-state electrical characteristics of poly-Si TFTs are dominated by the trap state density of grain boundary. Based on this issue of poly-Si TFTs, the method for reducing trap state density is applied to enhance the electrical characteristics. The typically used passivation methods are hydrogen plasma treatment and ion implantation [9]–[11]. The hydrogen plasma treatment is widely used to passivate trap states at poly-Si grain boundaries to avoid the undesirable leakage current [9]. However, it is difficult to control hydrogen concentration precisely in the poly-Si TFTs [9]. Also, the Si-H bonds are not strong enough against the hot carrier impact, during high electrical bias operation. One of the promising strategies on the electrical improvement of the poly-Si TFTs was proposed using F-ion implantation to eliminate the defects in the grain boundaries [10], [11]. Several proposed F-implantation technologies are summarized as followed. In the initial study, the pad oxide deposition on a-Si layer before crystallization was implemented to cause F-ions to pile up at the interfaces between the poly-Si and the oxide to eliminate the strain bonds. Also, F-implanted poly-Si TFTs without pad oxide deposition step were proposed to study in our previous work [12], [13]. The oxidized a-Si film on surface during thermal crystallization provides the driving force for the implanted fluorine elements to segregate on the surfaces. The proposed modified F-implantation passivation technology reduces manufacture process steps, and exhibits high potential for the application on AMLCDs. The undesirable strain bonds in the interface between poly-Si and SiO_2 are passivated by using F-ions-implantation. Furthermore, the segregated F-ions at the interface between poly-Si and buffer oxide eliminated the

Manuscript received March 15, 2006; revised May 20, 2006; June 28, 2006; and August 17, 2006. This work was performed at National Nano Device Laboratory. This work was supported by the National Science Council of the Republic of China under Contracts NSC 95-2221-E-009-283, NSC 95-2221-E-009-270, NSC 95-2120-M-110-003, and NSC 95-2221-E-009-254-MY2, and supported in part by MOEA Technology Development for Academia Project 94-EC-17-A-07-S1-046.

C.-H. Tu, C.-Y. Yang, L.-W. Feng, C.-C. Tsai, L.-T. Chang, S. M. Sze, and C.-Y. Chang are with the Institute of Electronics, National Chiao Tung University, Hsin-chu 300, Taiwan, R.O.C.

Y.-C. Wu is with the Department of Engineering and System Science, National Tsing-Hua University, Hsinchu, Taiwan, R.O.C.

T.-C. Chang is with the Department of Physics and Institute of Electro-Optical Engineering, National Sun Yat-Sen University, Kaohsiang 804, Taiwan, R.O.C., and also with National Nano Device Laboratories, Hsin-Chu 300, Taiwan, R.O.C. (e-mail: tcchang@mail.phys.nsysu.edu.tw).

P.-T. Liu is with the Department of Photonics and Display Institute, National Chiao Tung University, Hsin-Chu 300, Taiwan, R.O.C. (e-mail: ptliu@mail.nctu.edu.tw).

Color versions of one or more of the figures are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JDT.2006.890707

1551-319X/$25.00 © 2007 IEEE

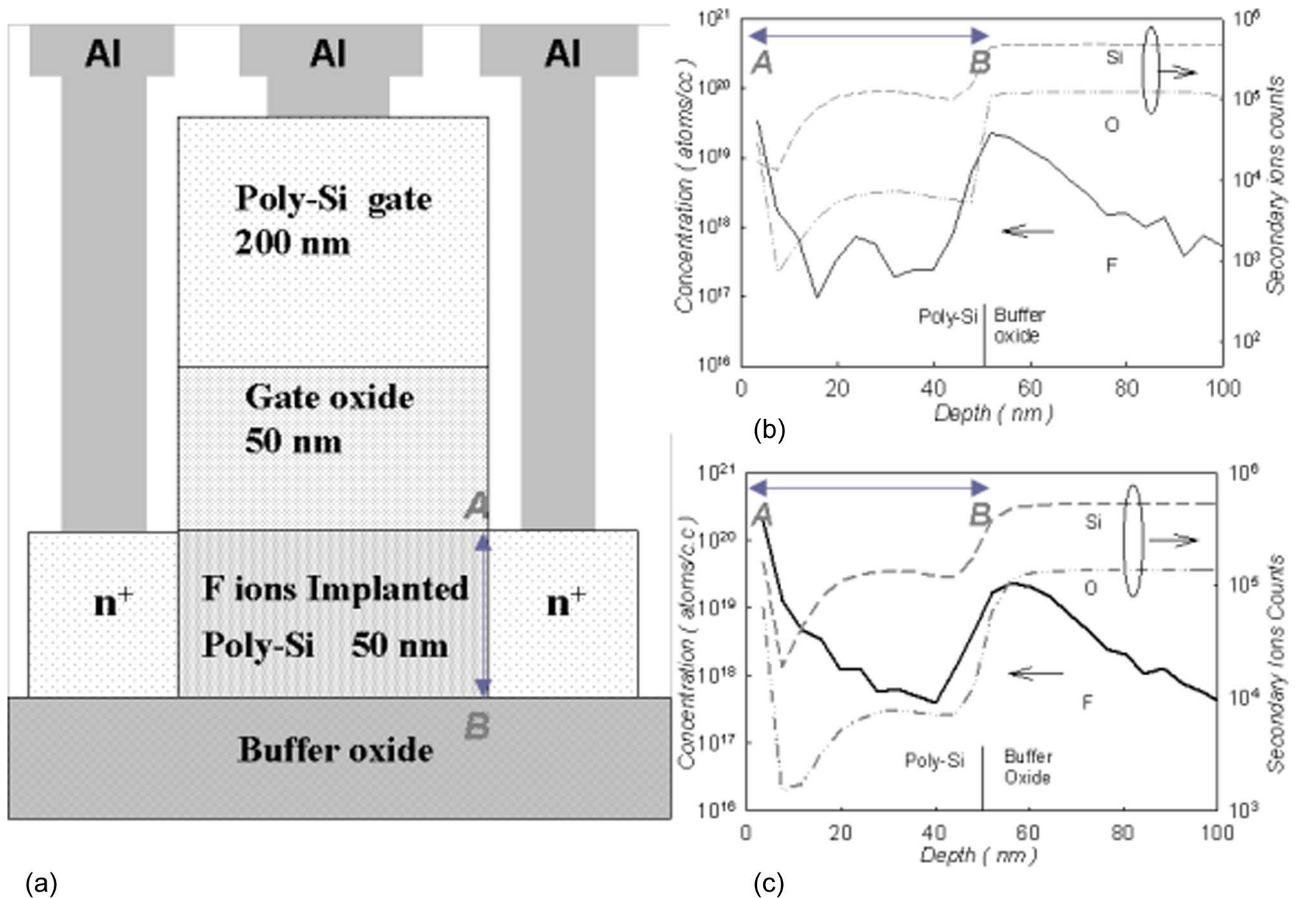


Fig. 1 (a) Cross-section of F-ions incorporated poly-Si TFTs. (b) The SIMS analysis of F-ions in poly-Si channel after SPC. (c) The SIMS analysis of F-ions in poly-Si channel after ELC.

strain bonds which are generated during rapid excimer laser annealing, leading to the superior electrical characteristics [14]. In addition, the strong Si-F bond replaced the weak Si-H and Si-Si bonds, resulting in the superior electrical DC stress reliability compared to standard poly-Si TFTs.

This work investigated the electrical characteristics of F-implanted poly-Si TFTs without the initial deposition of pad oxide before crystallization process. The poly-Si crystallization were realized by using conventional solid phase crystallization (*SPC*) and excimer laser crystallization (*ELC*). The behavior of F-implanted a-Si during the both the above crystallization steps were discussed. Also, the electrical reliability of poly-Si TFTs using both the crystallization methods were compared in this work.

II. Experiments

The 50-nm-thick undoped a-Si layer was deposited by decomposition of pure silane (SiH_4) on oxide-coated silicon wafer with using low pressure chemical vapor deposition (LPCVD) system at 550 °C. Then the F-ions were implanted to the a-Si layer without any pad oxide deposited first. The ion implantation conditions were set at an ion accelerating energy of 11 keV and the doping dosages are 5×10^{13} cm^{-2}. The crystallization for F-ions-implanted a-Si and standard a-Si was realized by heating in a furnace at 600 °C for 24 h in N_2 ambient and excimer laser annealing system, respectively. The *ELC* was realized by a KrF excimer laser system at room temperature in vacuum ($\sim 10^{-3}$ torr) with a laser energy of 300 mJ/cm^2. After patterning and etching the active region, the 50-nm-thick tetraethylorthosilicate (TEOS) layer and the 200-nm-thick poly-Si gate were deposited by LPCVD system. The deposition temperature of TEOS layer and poly-Si layer are 700 °C and 575 °C, respectively. The ions are used for the source–drain ion implantation after patterning and etching the poly-gate. The ion accelerating energy is 17 keV and the dosage is 5×10^{15} cm^{-2}. The activation was realized by depositing of the TEOS passivation layer using LPCVD system at 700 °C for 3 h. The contact hole regions were patterned and etched by a buffer oxide etching (BOE) solution. Finally, the aluminum metallization was performed, followed by 350 °C sintering in the thermal furnace for 30 min. The device cross section is shown in Fig. 1(a).

III. Results and Discussion

The behavior of F-ions in poly-Si after thermal annealing was investigated in this work. Fig. 1(b) and (1c) show the secondary ions mass spectroscope (SIMS) analysis of F-ions after *SPC* and *ELC*, respectively. It is found that the F-ions are piled up at the surface of poly-Si and the interface between poly-Si and buffer oxide. Without pad oxide deposited on a-Si layer, the F-ions are segregated to the poly-Si surface during recrystallization. Hence, it needs no extra thermal annealing step and no additional process steps for the F piling up. In addition, the electrical characteristics of F-ions-implanted poly-Si TFTs are investigated in this study. Fig. 2 shows the transfer

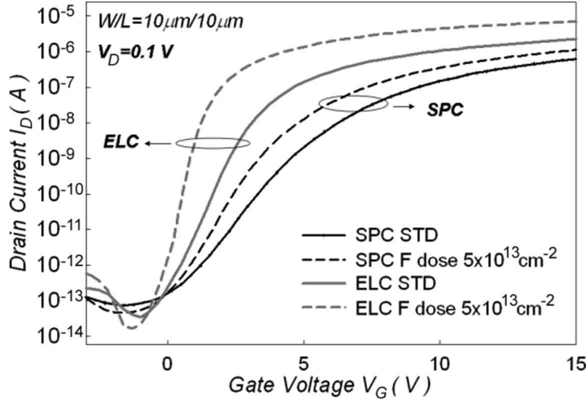


Fig. 2. The transfer characteristics of the poly-Si TFTs for F-ions-implantation dosage of 5×10^{13} cm^{-2} and standard.

TABLE I
THE PARAMETERS OF THE POLY-Si TFTs FOR F-IONS-IMPLANTED AND STANDARD USING SPC METHOD AND ELA METHOD

		μ_{FE} (cm^2/VS)	V_{TH} (V)	s.s (V/dec)	I_{ON}/I_{OFF} (10^6)	N_t (10^{12} cm^{-2})
STD	SPC	19.74	6.24	1.20	11.10	9.48
	ELC	56.65	3.07	0.61	26.01	5.18
F 5x10^{13}cm^{-2}	SPC	54.48	4.78	0.97	56.38	8.37
	ELC	103.94	1.19	0.30	87.62	3.07

characteristics of poly-Si TFTs for F-ions-implantation dosages of 5×10^{13} cm^{-2} and standard poly-Si TFTs. It is clearly found that the electrical characteristics are improved with F-ions-incorporated poly-Si TFTs no matter using *SPC* method or *ELC* method. The major parameters including field-effect mobility ($\mu_{\rm FE}$), threshold voltage ($V_{\rm TH}$), subthreshold swing ($S.S$), and trap state density (Nt) are summarized in the Table I. It is considered that the reduction of trap state density improves the electrical characteristics for the two types of devices. The fluorine effectively passivates the dangling bond, leading to lower trap state density. The threshold voltage ($V_{\rm TH}$) is defined as the gate voltage that yields the drain current ($I_{\rm DS}$) ($I_{\rm DS}$ = 10 nA $\times$ W/L). The threshold voltage is greatly reduced by using F-ions-implantation. The poly-Si TFTs with reduced $V_{\rm TH}$ have even more potential for the application on AMLCD. In addition, the $\mu_{\rm FE}$ is greatly improved in this work. It is found that the $\mu_{\rm FE}$ value for poly-Si using *SPC* method varies from 19.74 cm^2/V $\cdot$ s to 54.48 cm^2/V $\cdot$ s. Furthermore, the μ_{FE} value of F-ions-implanted poly-Si TFT (*ELC* method) is approximately two times to those of standard (56.65 cm^2/V$\cdot$s to 103.94 cm^2/V $\cdot$ s).

Fluorine piled up at the poly-Si/buffer-oxide interface, confirmed by SIMS analysis, and passivated the stress-induced strained bonds to form stronger Si-F bonds due to the high electronegativity of F atoms. The reduction of trap states between poly-Si and buffer oxide improves the performance of the poly-Si TFTs, such as $I_{\rm ON}$, $s.s$, and $I_{\rm OFF}$ [14]. Hence, the superior electrical characteristics are attributed to the relaxation of mechanical stress and trap state elimination in poly-Si TFTs, especially for using *ELC* method.

The activation energy (E_A) calculation is useful to confirm the fact of trap state density elimination for F-ions-implanted poly-Si TFTs. Fig. 3(a) and (b) show the E_A of drain current as a function of gate voltage measured at $V_D = 5$ V for standard and F-ions-implanted poly-Si TFTs. The activation energy was extracted by the measurement of $I_D - V_G$ characteristic in the temperature range from 20°C to 150°C. From the equation $I_D = I_0 e^{-(Ea/KT)}$, using the linear fitting of the $\ln({\rm I_D})$ versus the 1/KT plot, in which K is the Boltzmann constant and T is the temperature. Then the activation energy can be extracted. The E_A related with the barrier height in the poly-Si channel, expresses the carriers transportability [15]. For the F-ions-implanted poly-Si TFTs, the value of E_A extracted from on-state current is reduced, while E_A extracted from the off-state current is increased, indicating that F-ion implantation effectively reduces the trap state density. The E_A of off-state current is increased and the E_A of on-state current is reduced for the F-ions-implanted poly-Si TFT, indicating that F implantation alters the trap state density. This result is consistent with the above discussion. Furthermore, by calculating the trap states density distribution in the bandgap [16], the trap state densities for *SPC* method and *ELC* method, are clear reduced with F-ions incorporation are shown in Fig. 4(a) and (b), respectively. It is consistent with the result of activation energy as shown in Fig. 3(a) and (b). It is believed that the reduced trap states density causes the enhanced electrical characteristics. F-ions-incorporated poly-Si TFTs obtain reduced both the tail states and the deep states. The reduced deep states lead to decreased $V_{\rm TH}$ in n-ch poly-Si TFTs [10]. The tail state reduction improves the electrical characteristics such as s.s and μ_{FE} value [10], also compatible with our experimental results.

The study also considered the DC stress reliability for F-ions-implanted poly-Si TFTs. To investigate the device reliability, the poly-Si TFTs were bias stressed at $V_D = 20$ V and $V_G = 20$ V for time duration of 100, 200, 600, and 1000 s. Fig. 5 shows the $\Delta V_{\rm TH}$ values by the *SPC* method and *ELC* method. F-ions-implanted poly-Si TFTs are found to yield more moderate $\Delta V_{\rm TH}$ values than in standard poly-Si TFTs. Furthermore, hot carrier multiplication near the drain side degraded the $V_{\rm TH}$, $I_{\rm ON}$ and $s.s$ values. The $I_{\rm ON}$ and $s.s$ also reflect the reliability of the proposed TFT device. Figs. 6 and 7 illustrate the $\Delta I_{\rm ON}$ and $\Delta S.S$ after DC bias stress and demonstrate the F-ions implantation significantly reduce hot-carrier-induced degradation, respectively. Degradation induced by hot carrier stress can be attributed to the generation of gate oxide/poly-Si interface states and/or the Si-Si and/or Si-H weak bonds in the poly-Si channel [17], [18]. The Si dangling bonds are terminated by F-ions, and the resulting strong Si-F bonding enhances the endurance to hot carrier impact, thus improving the overall electrical reliability.

The electrical characteristics of poly-Si TFTs using *ELC* method are superior to using *SPC* method for larger grain size and less intra grain defect. However, the hot carrier impact is found to degrade the electrical characteristics. Compared with both crystallization methods, the *ELC* method indeed clearly improves the electrical characteristics, such as the μ_{FE}. The resultant higher μ_{FE} causes more serious degradation on electrical properties. In contrast, with F-ion implantation the improvement of DC bias stress reliability for *ELC* poly-Si TFTs

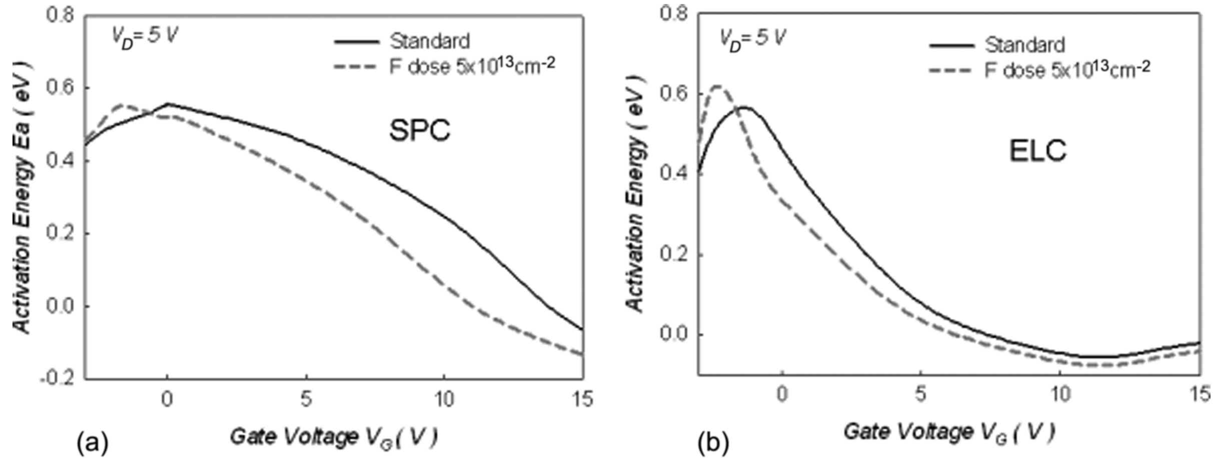


Fig. 3. (a) The activation energy (E_A) of the poly-Si TFTs (*SPC*) for F-ions-implantation dosage of 5×10^{13} cm^{-2} and standard at $V_D = 5$ V. (b) The activation energy (E_A) of the poly-Si TFTs (*ELC*) for F-ions-implantation dosage of 5×10^{13} cm^{-2} and standard at $V_D = 5$ V.

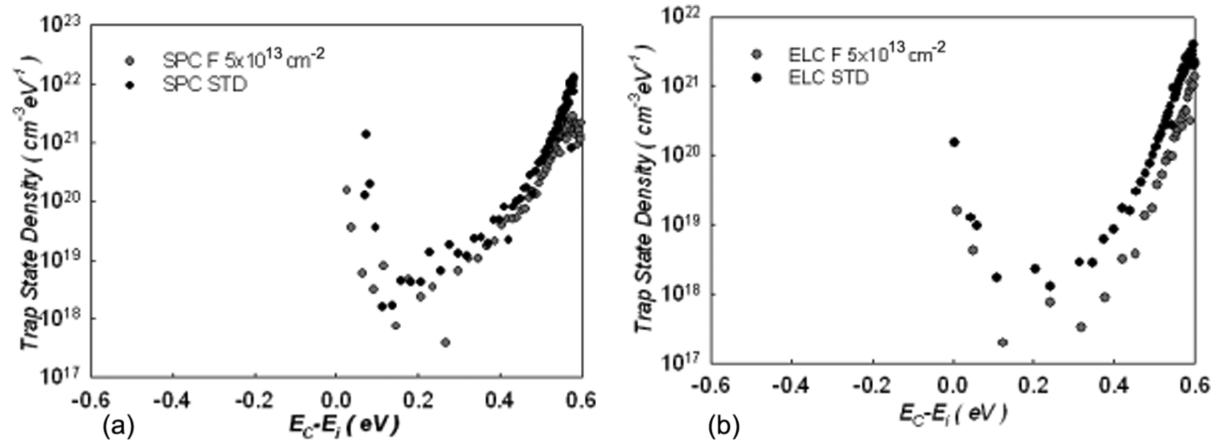


Fig. 4. (a) The trap state distribution in the bandgap of the poly-Si TFTs (*SPC*) for F-ions-implantation dosage of 5×10^{13} cm^{-2}. (b) The trap state distribution in the bandgap of the poly-Si TFTs (*ELC*) for F-ions-implantation dosage of 5×10^{13} cm^{-2}.

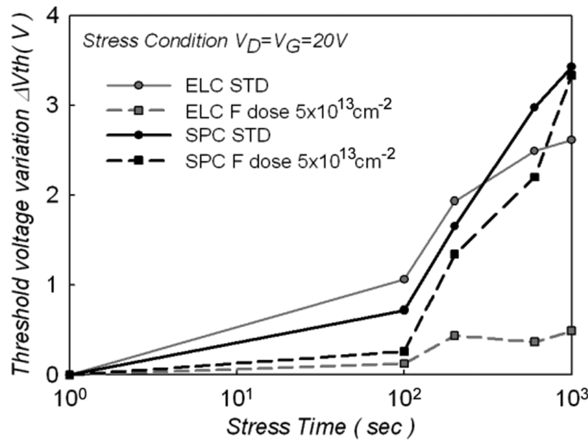


Fig. 5. The threshold voltage variation verse stress time for standard poly-Si TFTs and F-ions-implanted poly-Si TFTs for dosage of 5×10^{13} cm^{-2}.

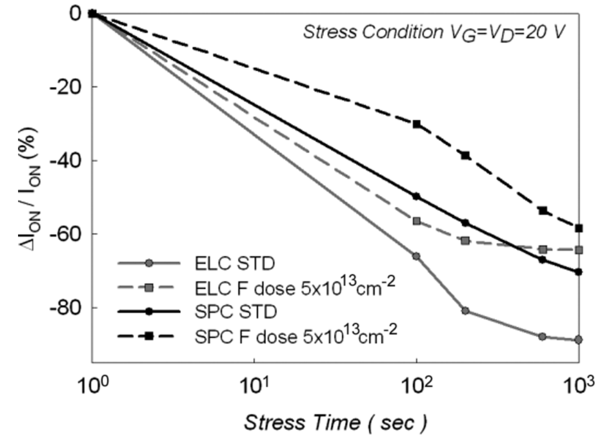


Fig. 6. The on current variation verse stress time for standard poly-Si TFTs and F-ions-implanted poly-Si TFTs for dosage of 5×10^{13} cm^{-2}.

is distinct. The lower trap state density for F-ions-implanted poly-Si TFTs (*ELC*), as shown in Table I, dominates the electrical improvement. The passivated Si dangling bonds (Si-F) can resist the hot carrier impact, although higher hot carrier energy can be obtained from *ELC* poly-Si TFTs with superior μ_{FE}.

The *ELC* method clearly improved the electrical characteristics, but degraded the DC stress reliability due to the high carrier field effect mobility. However, the F-ions-implantation for *ELC* method is more useful to improve the ability to resist the electrical DC stress.

IV. Conclusion

The electrical characteristics of the F-ions-implanted poly-Si TFTs have been investigated in this study. The fluorine ions segregated $(5 \times 10^{13}$ cm$^{-2})$ at the poly-Si interfaces by *SPC* and

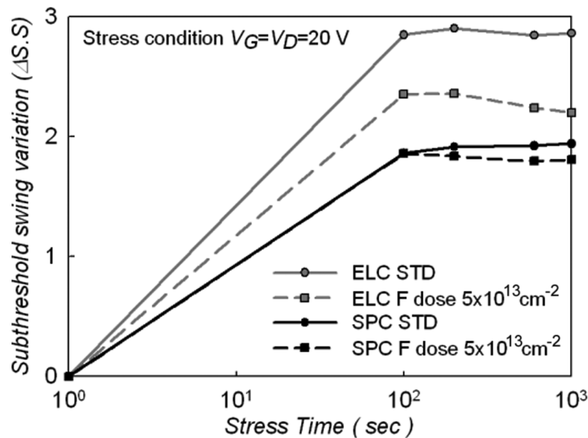


Fig. 7. The subthreshold swing variation verse stress time for standard poly-Si TFTs and F-ions-implanted poly-Si TFTs for dosage of 5×10^{13} cm^{-2}.

ELC processes, which effectively reduces the trap state density to enhance the electrical characteristics. The improvement of threshold voltage for *SPC* and *ELC* with the incorporation of fluorine ions are from 6.24 V to 4.78 V and 3.07 V to 1.19 V, respectively. Also, the strong Si-F bonds instead of the Si-H and Si-Si bonds can prevent hot carrier impact near the drain side, and possess superior electrical reliability over typical poly-Si TFTs. These improvements in electrical characteristics indicate the proposed F-ions-implantation method is suitable for high performance poly-Si TFT application in the display fields.

REFERENCES

[1] H. Oshima and S. Morozumi, "Future trends for TFT integrated circuits on glass substrates," in *IEDM Tech. Dig.*, 1989, pp. 157–160.

[2] S. D. Brotherton, Semicond, "Polycrystalline silicon thin film transistors," *Semicond. Science Tech*, vol. 10, pp. 721–738, 1995.

[3] K. Nakazawa, "Recrystallization of amorphous silicon films deposited by low-pressure chemical vapor deposition from Si2H6 gas," *J. Appl. Phys.*, vol. 69, pp. 1703–1706, 1991.

[4] T. J. King and K. C. Saraswat, "Low-temperature ($\leqq 550^\circ$C) fabrication of poly-Si thin-film transistors," *IEEE Electron Device Lett.*, vol. 13, pp. 309–311, 1992.

[5] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Tsuda, and S. Nakano, "High mobility poly-Si TFT by a new excimer laser annealing method for large area electronics," in *IEDM Tech. Dig*, 1991, vol. 91, pp. 563–566.

[6] R. E. I. Schropp, B. Stannowski, and J. K. Rath, "New challenges in thin film transistor (TFT) research," *Journal of Non-Crystalline Solids*, vol. 299–302, pp. 1304–1310, 2002.

[7] G. K. Giust and T. W. Sigmon, "High-performance thin-film transistors fabricated using exciter laser processing and grain engineering," *IEEE Trans. Electron Devices*, vol. 45, pp. 925–932, Apr. 1998.

[8] J. S. Im, R. S. Sposili, and M. A. Crowder, "Single-crystal Si films for thin-film transistor devices," *Appl. Phys. Lett.*, vol. 70, no. 25, pp. 3434–3436, 1997.

[9] I. W. Wu, A. G. Lewis, T. Y. Huang, and A. Chiang, "Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation," *IEEE Electron Device Letter*, vol. 12, pp. 181–183, 1993.

[10] H. N. Chern, C. L. Lee, and T. F. Lei, "The effects of fluorine passivation on polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 41, pp. 698–702, 1994.

[11] J. W. Park, B. T. Ahn, and K. Lee, "Effects of F+ implantation on the characteristics of poly-Si films and low-temperature n-ch poly-Si thin-film transistors," *Jan. J. Appl. Phy.*, vol. 34, pp. 1436–1441, 1995.

[12] C. H. Tu, T. C. Chang, P. T. Liu, H. W. Zan, Y. H. Tai, C. Y. Yang, Y. C. Wu, H. C. Liu, W. R. Chen, and C. Y. Chang, "Enhanced performance of poly-Si thin film transistors using fluorine ions implantation," *Electrochemical and Solid-State Letters*, vol. 8, pp. G246–G248, 2005.

[13] C. H. Tu, T. C. Chang, P. T. Liu, C. Y. Yang, H. C. Liu, W. R. Chen, Y. C. Wu, and C. Y. Chang, "Improvement of electrical characteristics for fluorine-ion-implanted poly-Si TFTs using ELC," *IEEE Electron Device Letter*, vol. 27, pp. 262–264, 2006.

[14] T. Kuan, A. Chou, and J. Kanicki, "Two-dimensional numerical simulation of solid-phase-crystallized polysilicon thin-film transistor characteristics," *Jpn. J. Appl. Phys.*, vol. 38, pt. 1, pp. 2251–2255, 1999.

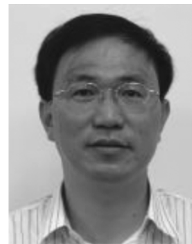
[15] C. L. Fan and M. C. Chen, "Performance improvement of excimer laser annealed poly-Si TFTs using fluorine ion implantation," *Electrochemical and Solid-State Letter*, vol. 5, pp. G75–G77, 2002.

[16] G. Fortunato and P. Migliorato, "Determination of gap state density in polycrystalline silicon by field-effect conductance," *Appl Phys Lett.*, vol. 49, pp. 1025–1027, 1986.

[17] S. Banerjee, R. Sundaresan, H. Shichijo, and S. Malhi, "Hot-electron degradation of n-channel polysilicon MOSFETs," *IEEE Trans. Electron Devices*, vol. 35, pp. 152–157, 1988.

[18] M. Hack, A. G. Lewis, and I. W. Wu, "Physical models for degradation effects in polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 40, pp. 890–897, 1993.

Chun-Hao Tu received the B.S degree in Physics from National Sun Yat-Sen University, Taiwan, R.O.C., in 2000. He is currently pursuing the Ph.D. degree at the National Chiao-Tung University, Taiwan, R.O.C. His Ph.D. research interests include fabrication, and characterization of amorphous silicon TFTs, LTPS TFTs and nonvolatile memory.



Ting-Chang Chang is a chair professor in Deportment of Physics, National Sun Yat-Sen University. In his specialty, he has made pioneering contributions to semiconductor device technology, ULSI memory devices and TFT-LCD Displays. He has published 150 articles in SCI journals and obtains 28 patents of United States and 70 patents of Taiwan. Besides, He proposed the project of Industry-Academy Cooperation with United Micoelectronics Corporation to research nano-porous low-k materials for ULSI application, and received great progress and achievement. He thereby had the honor to win the "Award of Industry-Academy Cooperation" from Ministry of Education in 2002. This is a remarkable honor in academic achievement. Recently, he is interested in the study of nonvolatile memory devices and nano-dot technology. He and his co-works exhibit greatly performance in these fields.

Po-Tsun Liu received his Ph.D. degree in the Institute of Electronics from the National Chiao Tung University in January 2000. He joined the National Nano Device Laboratory (NDL), Taiwan, as an associate researcher from January 2000, and became the leader of Department of Electro-optics and Bio-technology in March 2004. He has made a great deal of pioneering contributions to low-permittivity (low-k) dielectrics, copper interconnects and thin film transistors (TFTs) technologies. In his research on low-k dielectrics, he utilized plasma treatment technique for the first time to improve electrical characteristics of low-k silicate materials. In addition, he and his collaborators developed a novel technology to pattern low-k materials directly by using electron-beam lithography and X-ray radiation technology, instead of typically used photoresist coating and etch processing. Dr. Liu joined as the faculty of National Chiao Tung University

(NCTU) as an associate professor at the Department of Photonics and Display Institute on October in 2004. His main researches focus on the flat panel display (FPD) technologies, specialized in thin film transistors (TFTs), the advanced nano-scale semiconductor device technology, nanocrystal nonvolatile memory devices, and nano-fabrication technologies. He is a member of IEEE Society and Society for Information Display. So far, he has published 100 articles of SCI international journals, 51 international conference papers and obtained 52 U.S. and Taiwan patents. Because of the prominent contributions, he was selected in *Marquis Who's Who in the World* (20th edition, 2003).

Che-Yu Yang (S'05) received the B.S degree in Physics from National Sun Yat-Sen University and M.S degree in Electronics Engineering from National Chiao-Tung University,, Taiwan, R.O.C., in 2003 and 2005, respectively. His M.S research interests include fabrication, and characterization of LTPS TFTs.

Li-Wei Feng received the B.S degree in Physics from National Sun Yat-Sen University, Taiwan, R.O.C., in 2003 and M. S. degree in Electronics Engineering from National Chiao-Tung University, Taiwan, R.O.C in 2005. He is currently pursuing the Ph.D. degree at the National Chiao-Tung University, Taiwan, R.O.C. His Ph.D. research interests include fabrication, and characterization of amorphous silicon TFTs, LTPS TFTs and nonvolatile memory.

Chia-Chou Tsai received the B.S degree in physics from National Sun Yat-Sen University, Kaohsiung, Taiwan, R.O.C., in 2004, the M.S. degree from the National Chiao Tung University (NCTU), Hsinchu, Taiwan, R.O.C., in 2006. His thesis focused on nanowire nonvolatile memory devices and low temperature poly-Si TFT.

Li-Ting Chang was born in Kaohsiung, Taiwan, R.O.C. She received the B.S degree in physics from National Sun Yat-Sen Univeristy, Kaohsiung, Taiwan, R.O.C., in 2004, and is currently working toward the M.S. degree in electrical engineering at National Chiao Tung University, Hsinchu, Taiwan, R.O.C. Past research activities included nanodot technology, and low temperature poly-Si TFTs.

Yung-Chun Wu received the B.S degree in physics from National Central University and M. S. degree in physics from National Taiwan University, Taiwan, R.O.C. in 1996 and 1998, respectively. He is currently pursuing the Ph.D. degree at the National Chiao-Tung University, Taiwan, R.O.C. His Ph.D. research activities include fabrication, simulation and characterization of submicron LTPS TFT and novel nano-scale devices.

From 1998 to 2002, he was an assistant researcher at National Nano-Device Laboratory, Taiwan, R.O.C., engaged in research of single electron transistor and electron beam lithography technology.

Simon M. Sze (M'66–SM'74–F'77–LF'02) is presently UMC Chair Professor and an honorary professor in the Department of Electronics Engineering, National Chiao Tung University (NCTU), Hsinchu, Taiwan, R.O.C. He was with Bell Laboratories in New Jersey, USA, from 1963 to 1989. He joined the faculty of the NCTU Electronic Engineering Department in 1990. He has served as a visiting professor to many academic institutions, including the University of Cambridge, Delft University, the University of Hong Kong, Suchou University, Stanford University, and the Swiss Federal Institute of Technology. He has made fundamental and pioneering contributions to semiconductor devices, especially the metal-semiconductor contacts, microwave devices, and submicron MOSFET technologies. Of particular importance, is his invention of the floating-gate semiconductor nonvolatile memory, such as the EEPROM and the flash memory. This memory is a key component for the cellular phone, notebook computer, smart IC card, digital camera, DVD, GPS, PDA, and a host of other electronic systems. He has authored or coauthored over 200 technical papers. He has written, edited, and contributed to 26 books. His book *Physics of Semiconductor Devices* (Wiley, 1st Edition, 1969; 2nd Edition, 1981) is the most cited work in contemporary engineering and applied science publications. It has been translated into seven languages. More than one million copies have been sold as of 2004.

Prof. Sze has received the IEEE J. J. Ebers Award, the Sun Yet-sen Award, the National Chair Professor Award, and the National Science and Technology Prize. He is a member of the Academia Sinica, the Chinese Academy of Engineering, and the U.S. National Academy of Engineering.

Chun-Yen Chang (S'69–M'70–SM'81–F'88–LF'05) was born in Feng-Shan, Taiwan, R.O.C. He received the B.S. degree in electrical engineering from Cheng Kung University, Taiwan, in 1960, and the M.S. degree in tunneling in semiconductor-supercondutor junctions and the Ph.D. degree in carrier transport across metal-semiconductor barrier, both from National Chiao-Tung University (NCTU) Hsinchu, Taiwan, in 1969.

He has devoted himself to education and academic research for more than 40 years. He has contributed profoundly to the areas of microelectronics and optoelectronics, including the invention of the method of low-pressure-MOCVD-using tri-ethyl-gallium to fabricate LED, laser, and microwave transistors, Zn-incorporation of SiO for stabilization of power devices, and nitridation of SiO for ULSIs, etc. From 1962 to 1963, he fulfilled his military service by establishing at NCTU Taiwan's first experiment TV transmitter that formed the founding structure of today's CTS. In 1963, he joined NCTU to serve as an instructor establishing a high vacuum laboratory. In 1964, he and his colleague established the semiconductor research center (SRC) at NCTU with a very up-to-date, albeit homemade, facility for silicon device processing, where they made the nation's first Si Planar transistor in April 1965, and subsequently the first IC in August 1966. In 1968, he published Taiwan's first-ever semiconductor paper in the

international journal *Solid State Electronics*. In 1969, he became a Full Professor, teaching solid state physics, quantum mechanics, semiconductor devices and technologies. From 1977 through 1987, he single-handedly established a strong electrical engineering and computer science program at NCKU where GaAs, Si, poly-Si researches were established in Taiwan for the first time. Since 1987 he served consecutively as Dean of Research (1987–1990), Dean of Engineering (1990–1994), and Dean of Electrical Engineering and Computer Science (1994–1995). Simultaneously he was serving as the founding president of National Nano Device Laboratories (NDL) from 1990 through 1997. In 1997, he became Director of the Microelectronics and Information System Research Center (MIRC), NCTU (1997–1998). Many of his former students have since become founders of the most influential Hi-Tech enterprises in Taiwan, namely UMC, TSMC, Winbond, MOSEL, Acer, Leo, etc. In August 1, 1998, he was appointed as the President of NCTU (1998–2006). As the National-Chair-Professor and President of NCTU, his vision is to lead the university for excellence in engineering, humanity, art, science, management and bio-technology. To strive forward to world class multidisciplinary university is the main goal to which he and his colleagues have committed.

Dr. Chang received the IEEE third millennium medal in 2000. He is a member of Academia Sinica and a Foreign Associate of the National Academy of Engineering.