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A test structure was proposed to investigate the spatial and temporal evolution of hot-carrier degradation in *n*-channel poly-Si thin-film transistors. Our experimental results clearly show that the initial damage during the early stage of hot-carrier stressing, which is still undetectable by conventional test structures, can be easily observed by the structure. In addition, the proposed test structure is also capable of resolving the evolution of the degradation along the channel, thus providing a powerful tool to study the location-dependent damage mechanisms. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2710302]

I. INTRODUCTION

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) are used in many applications, including flat-panel displays and large-area microelectronics.[1] Because of their better film crystallinity, significant improvement in carrier mobility and drive current can be realized in poly-Si TFTs, compared with the amorphous silicon TFTs. Nevertheless, hot-carrier (HC) degradation remains as one of the most critical reliability concerns for practical applications of poly-Si TFTs.[2] Hot carriers are caused by the high electric field existing in the channel. By releasing their energy, these hot carriers could cause defect generation and performance degradation.[3] Since the channel electric field is not uniformly distributed, HC damage is location-dependent in the channel.

Due to the lack of substrate contacts, together with the presence of numerous inter-/intragrain defects,[4] the whole picture is much more complicated for poly-Si TFTs, compared with bulk metal oxide semiconductor field effect transistors (MOSFETs). As a result, numerical simulation techniques are normally required to acquire the location dependence of the HC effects under specific stress conditions.[5] Resolving the evolution of hot-carrier degradation is also challenging. This is because the damage creation itself may affect the temporal potential distribution during stressing and therefore subsequent degradation characteristics. Recently, a test structure capable of spatially resolving the damage along the channel of the stressed transistor has been proposed by our group.[6] With the proposed structure, analyses of HC degradation and mechanism along the stressed channel become feasible. In this work, we further investigate in detail the sensitivity and effectiveness of the test structure in revealing the impact of applied stress conditions, as well as the position dependence and the evolution of the degradation.

II. DEVICE STRUCTURE AND FABRICATION

Figure 1(a) illustrates the top view of the test structure. It consists of one test transistor along the *x* direction [Fig. 1(b), denoted as TT] and three monitor transistors along the *y* direction [Fig. 1(c), denoted as S-MT, C-MT, and D-MT]. All TTs and MTs were characterized before and after the stressing. The damage induced at different portions of the channel can be directly characterized by the MTs. It is worth noting that the proposed test structure requires only layout modifications, and could be easily integrated with the display panel processing without extra masks or steps.

Samples in this work were prepared on oxidized Si wa-

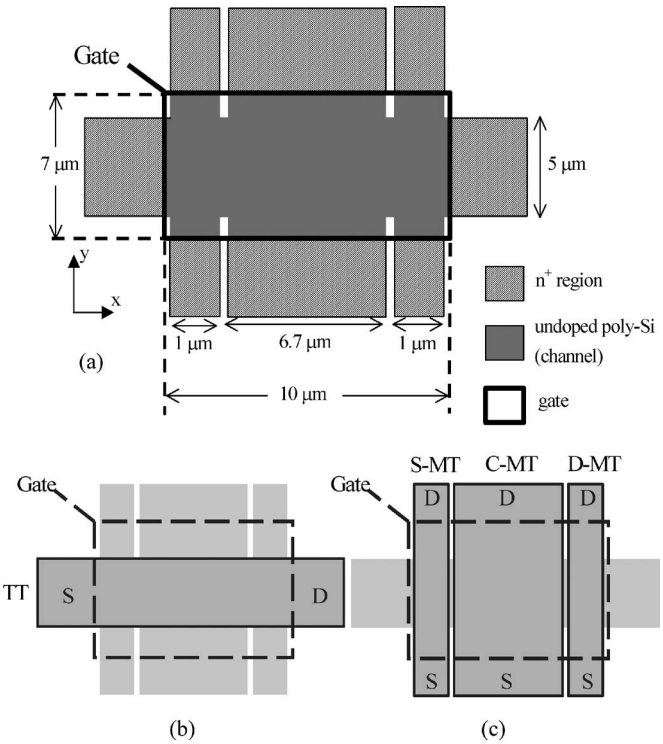

FIG. 1. Schematic and operating configurations of the test structure.

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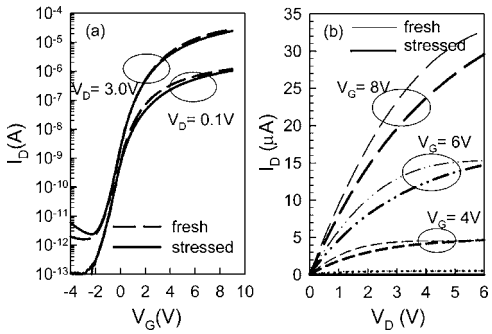

FIG. 2. (a) Subthreshold and (b) output characteristics of the test transistor (TT) before and after hot-carrier stress under V_G/V_D=9 V/18 V for 1000 s.

fers. A 50 nm thick amorphous silicon was deposited and recrystallized at 600 °C in N_2 for 24 h, and then patterned to serve as the active device region. Next, a 35 nm thick oxide and 200 nm thick n^+ poly-Si were deposited and patterned to form the gate dielectric and gate electrode, respectively. Afterwards, standard processings for source/drain formation, passivation, and metallization were performed. Finally, samples received a plasma treatment in NH_3 ambient at 300 °C for 1 h.

III. RESULTS AND DISCUSSION

A. High drain voltage stressing

For high drain voltage stressing, the test transistor was stressed under a high V_D of 18 V and V_G of 9 V. Figures 2(a) and 2(b) show the subthreshold and output characteristics, respectively, of the TT, after 1000 s of stressing. It can be seen that noticeable degradation is observed in the figures. Specifically, a slightly retarded subthreshold swing is observed in Fig. 2(a) and a slightly degraded output current in observed in Fig. 2(b). These results are consistent with the well-known hot-carrier degradation mechanisms: Hot-carrier stressing can generate additional interface states and/or grain-boundary defect states[7] and form a defect-rich and resistive region near the drain side.[5]

The aforementioned damage scenario has been characterized in the literature by a number of techniques, including reverse source/drain measurement,[8] capacitance-voltage (C-V) measurement,[9] device simulation,[5,10] asymmetric drain/source structure,[8] and picosecond time-resolved emission microscope.[11] However, all the above methods failed to directly and unambiguously pinpoint the damage location. By contrast, MTs in our proposed test structure provide useful degradation characteristics in different parts of the channel, as shown in Fig. 3. It can be seen that the subthreshold characteristics of the MT near the drain side (D-MT) show clear and visible degradations in both subthreshold swing and on-state current (I_{on}). On the contrary, the monitor transistor near the source side (S-MT) depicts only negligible damage. These results confirm that the location dependence of HC degradation could be clearly resolved with the test structure.

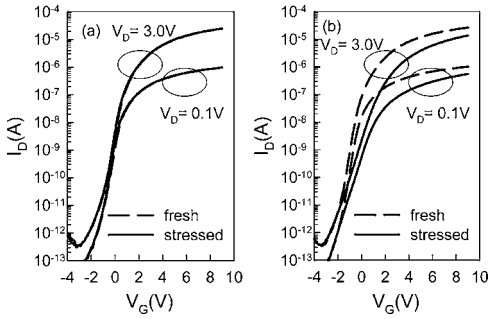

FIG. 3. Subthreshold characteristics of (a) S-MT and (b) D-MT, before and after hot-carrier stress under V_G/V_D=9 V/18 V for 1000 s.

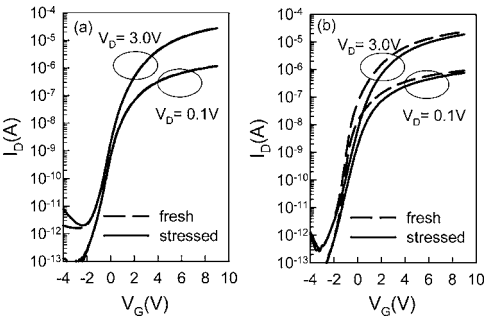

FIG. 4. Subthreshold characteristics of (a) TT and (b) D-MT, before and after hot-carrier stress under V_G/V_D=6.5 V/13 V for 1000 s.

B. Low drain voltage stressing

The test structure also provides excellent sensitivity for the detection of hot-carrier degradation. To induce visible degradation, researchers usually resorted to severe stress condition with high stress voltage or sufficiently long stress time. For practical device operation, however, the applied biases to the device are low, so the degradation is almost impossible to observe. The proposed test structure with its high sensitivity is suitable to resolve this problem. This is demonstrated by comparing the characteristics of TT [Fig. 2(a)] and D-MT [Fig. 3(b)]. It is clearly seen that the degradation in the normal structure (TT) is amplified by the associated D-MT. To further highlight this feature, the test structure was stressed under V_D of 13 V and V_G of 6.5 V for 1000 s, a condition where the stress field was much reduced than that in Figs. 2 and 3. As shown in Fig. 4(a), the test transistor exhibits barely detectable degradation after the stressing because of the milder stress condition. This will call

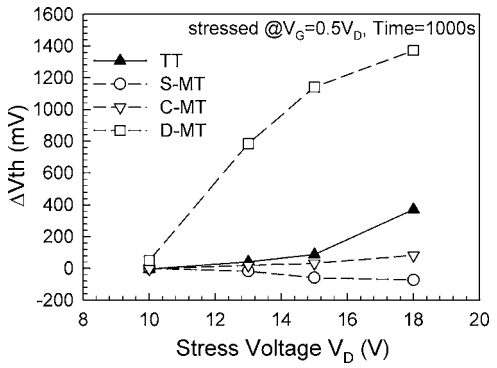

FIG. 5. Threshold voltage shift of the test structure under various hot-carrier stress conditions with constant V_G/V_D ratio of 0.5.

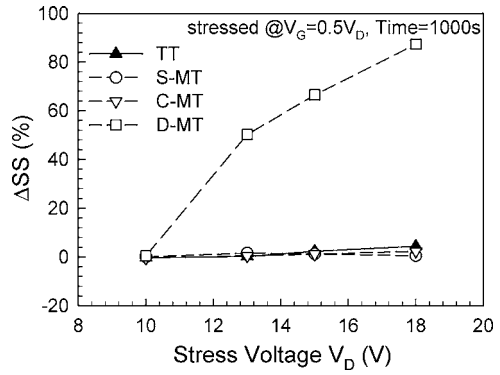

FIG. 6. Subthreshold swing degradation of the test structure under various hot-carrier stress conditions with constant V_G/V_D ratio of 0.5.

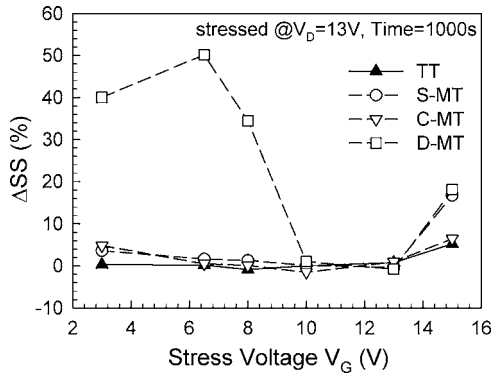

FIG. 8. Subthreshold swing degradation of the test structure under various hot-carrier stress conditions at a fixed V_D of 13 V.

for a very long stress time for the TT to produce detectable degradation similar to that shown in Fig. 2. However, the associated D-MT shows visible degradation, as shown in Fig. 4(b). The enhanced sensitivity thus allows the study of the degradation under a milder stress condition.

Figures 5 and 6 show the shift in threshold voltage (ΔV_{th}) and subthreshold swing (ΔSS), respectively, as a function of stress V_D with $V_G=0.5V_D$ for 1000 s. As expected, the degradation increases with increasing V_D. When V_D is less than 15 V, TTs depict a threshold voltage shift of less than 100 mV and negligible change in the subthreshold swing. This again indicates that the traditional test structure is not suitable for monitoring milder stress conditions. In contrast, the minor damage can be unambiguously detected with the monitor transistors in the test structure. Moreover, the severely degraded characteristics of D-MTs after stressing clearly pinpoint the major damage site. In fact, it is possible to investigate the damage mechanisms in different parts of the channel. This point is further addressed in the following subsection.

C. Effects of stress gate voltage

Figures 7 and 8 show the shift in threshold voltage and subthreshold swing, respectively, of the TT and MTs after 1000 s stress at V_D of 13 V and various V_G. It is seen that ΔV_{th} of the test transistor is positive in the low V_G regime, monotonically decreases with increasing V_G, and becomes negative as V_G exceeds 10 V. The information is, however, very limited. By contrast, MTs' data reveal several interesting features. First, the drain-side damage is dominant in the low V_G regime, and peaks at around $V_G=0.5V_D$. A similar trend is also observed in ΔSS, as shown in Fig. 8, implying that the generation of oxide interface states and defects at grain boundaries are the likely culprits. The major damage site gradually moves toward the source as V_G increases. The negative threshold voltage shift in the S-MT device as $V_G > 8$ V indicates that hole trapping in the gate oxide now dominates the degradation.

D. Evolution of the HC degradation

From the above results, we can see that the degradation is complicated and is related to both V_G and V_D. Next, we investigate the evolution of degradation under two distinctly different stress modes, namely, $V_G=0.5V_D$ and $V_G=V_D$.

As shown in Figs. 9 and 10, the evolution of the degradation induced in different parts of the channel under $V_D/V_G=13$ V/6.5 V can be directly resolved with the test structure. Specifically, although TT's data show negligible subthreshold shift after the stressing, the D-MT shows unambiguous degradation at a very early stage, and the degradation increases monotonically with increasing stress time. Moreover, a negative threshold voltage shift for S-MTs becomes clear when the stress time is longer than 100 s. Similar findings can also be found in Figs. 5 and 7, confirming that the dominant damage mechanism is indeed position dependent. Although this has been well known in the literature, the direct observation of position-dependent damage mecha-

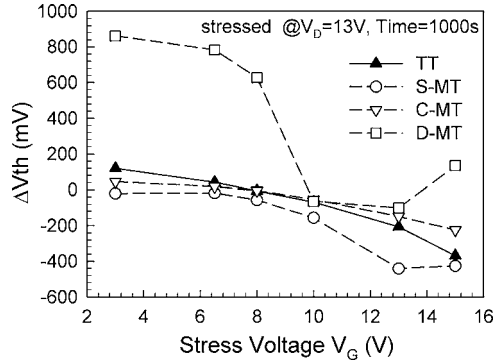

FIG. 7. Threshold voltage shift of the test structure under various hot-carrier stress conditions at a fixed V_D of 13 V.

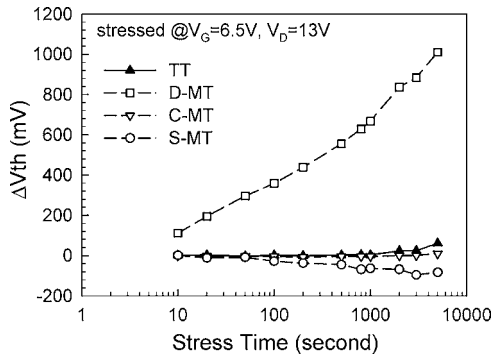

FIG. 9. Evolution of threshold voltage shift of the test structure during hot-carrier stress under $V_G/V_D=6.5$ V/13 V.

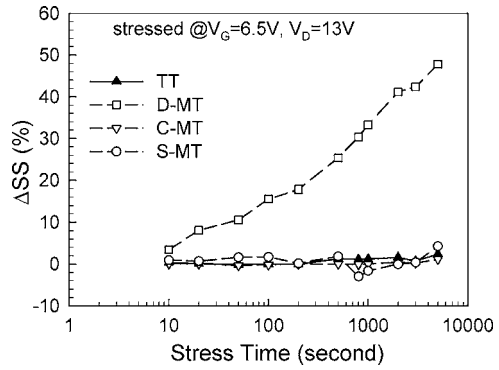

FIG. 10. Evolution of subthreshold swing degradation of the test structure during hot-carrier stress under V_G/V_D=6.5 V/13 V.

nisms without involving a complicated experimental scheme illustrates the uniqueness and usefulness of the proposed test structure.

From the aforementioned results, the degradation during HC stressing under $V_G=0.5V_D$ condition is illustrated in Fig. 11. In this case, impact ionization occurs at the drain side by the high field strength, and causes the generation of electron-hole pairs. The generated hot carriers may release their energy in the channel or near the oxide/channel interface where defects are created. Since no substrate contact is present in the TFT structure, the generated holes tend to drift toward the grounded source; some of them may have sufficient energy to surmount the barrier and are injected into the oxide. This mechanism explains the negative threshold voltage shift of S-MTs.

Temporal evolution analyses for devices under $V_G=V_D$ stress mode are presented in Figs. 12 and 13. It is seen that the test and all monitor transistors depict a negative threshold voltage shift, implying that the generation of positive charge is mainly responsible for the degradation. Moreover, among these devices, S-MT exhibits the largest shift. It should be noted that, although the S-MT characterized in Fig. 9 under $V_G=0.5V_D$ stress mode also exhibits a negative threshold voltage shift, the extent of the shift in the present case (Fig. 12) is much larger. For the two stress modes, it is well known that the impact ionization rate is suppressed under $V_G=V_D$ stress mode.[12] This indicates that hole trapping illustrated in Fig. 11 alone cannot account for the observation shown in Fig. 12, and some other mechanisms should be responsible for the degradation. It is likely that the oxide field between the gate and the channel plays an important role, as a high gate voltage (e.g., 13 V) applied during stressing that exerts an oxide field (~3.7 MV/cm) above the channel near the source side. It has been pointed out previously[13] that such

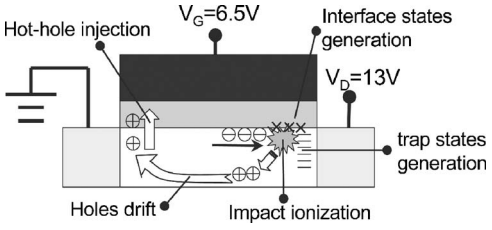

FIG. 11. Schematic illustration of the hot-carrier degradation mechanisms under V_G/V_D=6.5 V/13 V.

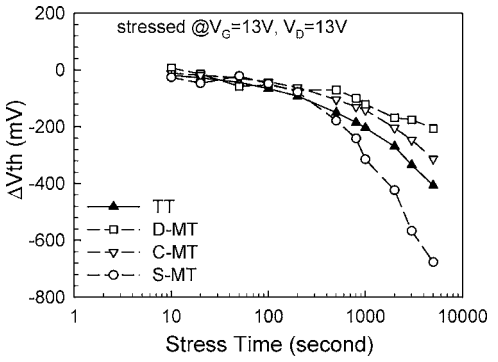

FIG. 12. Evolution of threshold voltage shift of the test structure during hot-carrier stress under V_G/V_D=13 V/13 V.

field may lead to the generation of a positive charge in the oxide. This phenomenon can consistently explain the results observed in Figs. 12 and 13.

IV. CONCLUSION

In this work, a TFT test structure is employed for the characterization of HC degradation. The fabrication of the proposed test structure is simple and compatible with standard ultra-large-scale integration (ULSI) processing without extra masking. Several advantages of the test structure are demonstrated in this work. (1) the capability of resolving the damage characteristics in different parts of the channel, (2) the greatly enhanced sensitivity in detecting the localized damage, which is helpful for studying the damage characteristics under a milder stress condition, (3) the evolution of degradation in specific regions could also be detected directly, and (4) dominant damage mechanism could be identified. Specifically, in this work we found that at least two mechanisms are responsible for the negative threshold voltage shift detected by the monitor transistors. With these unique features, the proposed test structure represents a powerful tool in practical applications for studying the reliability of TFT devices.

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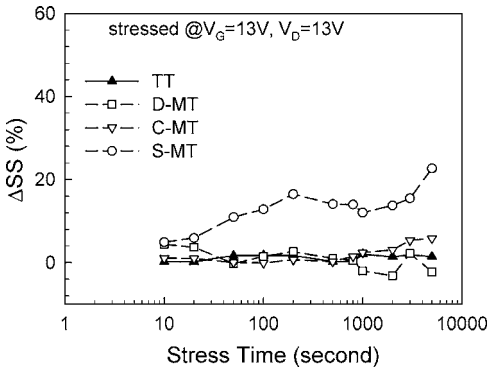

FIG. 13. Evolution of subthreshold swing degradation of the test structure during hot-carrier stress under V_G/V_D=13 V/13 V.

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