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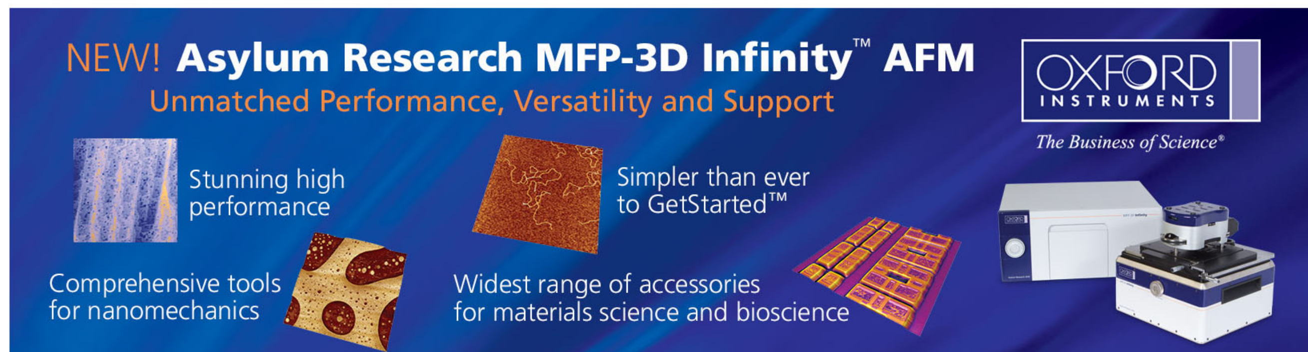

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Stability of continuous-wave laser-crystallized epilike silicon transistors

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Stability of high-hole-mobility thin-film transistors (TFTs) on single-grainlike silicon channels formed by continuous-wave laser crystallization during hot-carrier stressing (HCS) was studied. As channel layers become thicker, laser-mediated channel crystallinity increases, increasing channel roughness. On such epilike polycrystalline silicon substrates, the poorer interface quality for thicker channels, even those with lower tail-state densities of grain traps, is responsible for the extensive charge trapping and creation of deep-state densities in the fabricated TFTs due to HCS. Hence, on a thin channel with a thickness of 50 nm and ultrasmooth surfaces, HCS hardly degrades the electrical parameters of the devices. © *2007 American Institute of Physics*.
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The development of laser-crystallized single-grainlike polycrystalline silicon (polysilicon) thin-film transistors (poly-Si TFTs) on glass substrates extends current applications of TFTs as pixel switches to prophetical circuits[1] and current drivers.[2] A high-speed and reliable transistor must have a thin channel, such that the interfacial features dominate the performance of polysilicon TFTs.[3] Accordingly, two laser annealing approaches, continuous-wave (cw) laser crystallization[1] (CLC) and excimer-laser-annealing-based sequential lateral solidification (SLS),[4] have attracted substantial interest due to their usefulness in the formation of epilike microstructures and the maintenance of low surface roughness on crystallized channels.[5]

Voutsas *et al.*[6] investigated the dependence of degradation mechanisms on the thickness of SLS channels. Changes in the degradation of electrical parameters that are caused by hot-carrier stressing (HCS) and related to channel thickness were attributed to crystalline quality and partial depletion-induced carrier accumulation. However, in laser-induced crystallization methods, the thickness of irradiated films simultaneously affects channel crystallinity and roughness.[4,7] Hence, the dependence of channel roughness and device reliability on the thickness of CLC channels warrants further study.

This investigation explores the mechanisms of degradation of CLC epilike Si TFTs during HCS, with reference to channel thickness.

Poly-Si channels on glass substrates were formed by the green cw laser crystallization of amorphous silicon islands with thicknesses of 50 and 150 nm, which were deposited by plasma-enhanced chemical vapor deposition (PECVD). In fabricated *p*-type TFTs, PECVD SiO_2 grown at 380 °C with a thickness of 100 nm is applied as a gate dielectric. The stability of fabricated devices with width/length=60 μm/60 μm during HCS with gate voltage (V_g)=drain voltage (V_d)=−20 V at room temperature was examined. As HCS proceeded, the transfer characteristics (drain current I_d vs V_g), and therefore electrical parameters of the devices, were taken periodically during bias stressing using the same method as reported by Karim *et al.*[8] and Zafar *et al.*[9] Grain trap-state densities n_{GT} for all TFTs were examined using the field-effect conductance method.[10]

The crystallinity in laser-crystallized films normally increases with film thickness,[4] as revealed by the topographies of CLC poly-Si (in the insets of Fig. 1). This relationship is responsible for the larger channel roughness on thicker films because larger grains lead to larger fluctuations in the surface profile.[7] Consequently, the tail-state density of grain traps, which was closely related to channel crystallinity,[5] n_{GT} at an

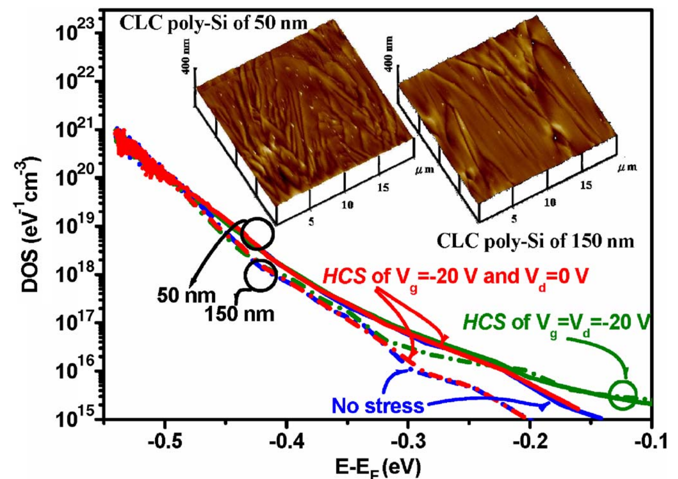

FIG. 1. (Color online) (a) Energy distribution associated with grain trap-state densities in fresh, hot-carrier, and gate-bias stressed TFTs made on CLC poly-Si with thicknesses of 50 and 150 nm. The insets display atomic force microscope topographies of two CLC channels with thicknesses of 50 and 150 nm.

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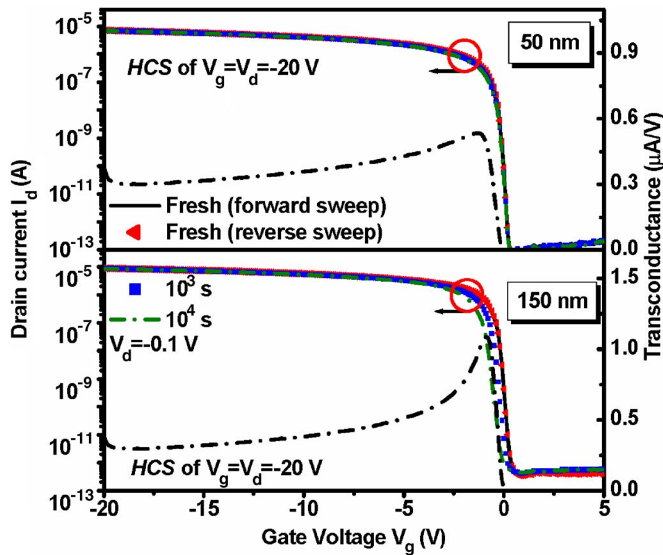

FIG. 2. (Color online) Transient transfer characteristics and transconductance curves of TFTs made on CLC poly-Si with thicknesses of (a) 50 nm and (b) 150 nm during HCS. I_d-V_g hysteresis curves of fresh devices are also shown.

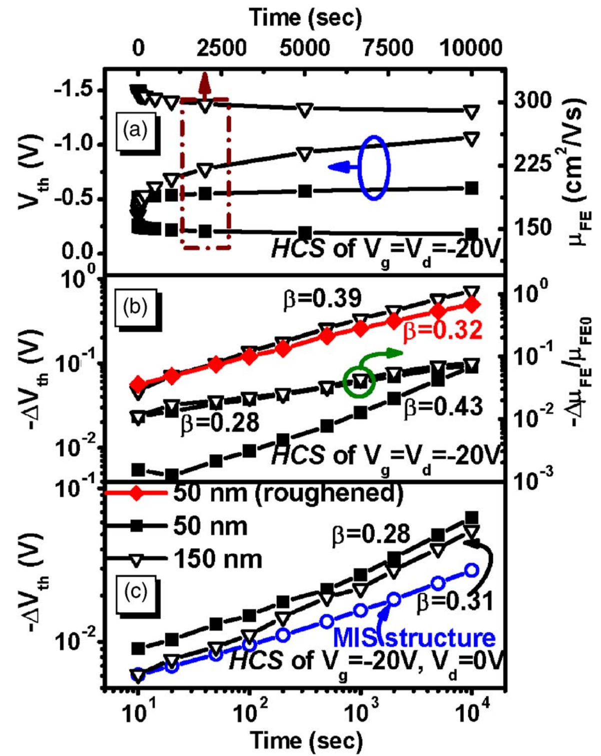

FIG. 3. (Color online) (a) Transients of field-effect mobility and threshold voltage of TFTs made on CLC poly-Si with thicknesses of 50 and 150 nm during HCS with $V_g=V_d=-20$ V. Degradation of V_{th} and μ_{FE} of TFTs made on CLC poly-Si with thicknesses of 50 and 150 nm during HCS with (b) $V_g=V_d=-20$ V and (c) $V_g=-20$ V and $V_d=0$ V. Degradation of flatband voltage of a metal–SiO_2–bulk-Si structure stressed at $V_g=-20$ V is also shown.

energetic level (E) that was far from the Fermi level (E_F), $\Delta E=E-E_F=-0.55$ to -0.4 eV, was lower in thicker channels (Fig. 1). Notably, the field-effect mobility (μ_{FE}) of TFTs was determined by the number of tail states in such an epi-like CLC poly-Si of a particular thickness, rather than throughout the channel layer.[11] This finding explains why the μ_{FE} of devices obtained with CLC poly-Si with a thickness of 150 nm is as high as 315 $\mathrm{cm}^2/\mathrm{V\,s}$, which is double that obtained with CLC poly-Si with a thickness of 50 nm, as revealed by the linear transconductance (G_m) curves plotted in Fig. 2.

Figure 2 plots some representative transient transfer characteristics of hot-carrier stressed TFTs on CLC poly-Si with thicknesses of 50 and 150 nm. Figures 3(a) and 3(b) plot the transients of μ_{FE} and threshold voltage (V_{th}), and the degradation of the V_{th} shift (ΔV_{th}) and the normalized μ_{FE} shift ($\Delta\mu_{\mathrm{FE}}/\mu_{\mathrm{FE0}}$, where μ_{FE0} stands for initial μ_{FE}) for stressed devices in Fig. 2 against film thickness and stress time (t). According to the carrier-induced defect creation, charge trapping, and empirical models,[8,9,12,13] the degradations of V_{th} and $\Delta\mu_{\mathrm{FE}}/\mu_{\mathrm{FE0}}$ due to bias stressing follow a power law in time ($\sim t^{\beta}$), where power-law exponents $(\beta)=0.1-0.3$ are related to hot-carrier injection while $\beta=0.4-0.6$ point towards deep-state creation.[6,13,14] HCS negligibly changed the tail-state densities of grain traps in both channels (Fig. 1), which is consistent with β of 0.28 in $\Delta\mu_{\mathrm{FE}}/\mu_{\mathrm{FE0}}$ degradation for both channels. However, the values of β associated with V_{th} degradation for thick and thin channels are 0.39 and 0.43, respectively.

Unlike μ_{FE}, V_{th} and the subthreshold slope (S) are governed by the numbers of interface and grain trap states per unit channel area, N_T,[15,16] at $\Delta E\sim 0$ to -0.3 eV, where S is governed strongly by N_T near the intrinsic Fermi level ($\Delta E\sim 0$ eV). For fresh TFTs, the areal density of grain trap states, N_G, averaged over the range $\Delta E=0$ to -0.3 eV in thick CLC poly-Si was about $4.8\times 10^{10}\ \mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$—less than that, $5.2\times 10^{10}\ \mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$, in thin CLC poly-Si, where N_G was estimated from $n_{GT}\,t_{\mathrm{CLC}}$ and t_{CLC} denotes the thickness of the CLC poly-Si. HCS clearly increased the n_{GT} of stressed TFTs at $\Delta E\sim -1$ to -0.3 eV in both channels (Fig. 1), verifying that deep-state generation is involved in V_{th} degradation. Moreover, after HCS, V_{th}, the averaged N_G, and the change in n_{GT} at the deep energetic level in the thick channel exceed inversely those in the thin channel [Figs. 1, 3(a), 3(b), and 4].

Fresh (stressed) devices on thick channels with a roughness of 4.2 nm had a worse S, 117 (157) mV/decade, than the S, 93 (97) mV/decade, of devices on thin channels with a roughness of 3.7 nm. Given these values of S, the value of N_T at $\Delta E\sim 0$ eV was calculated.[15–17] N_G at $\Delta E\sim -0.1$ eV for

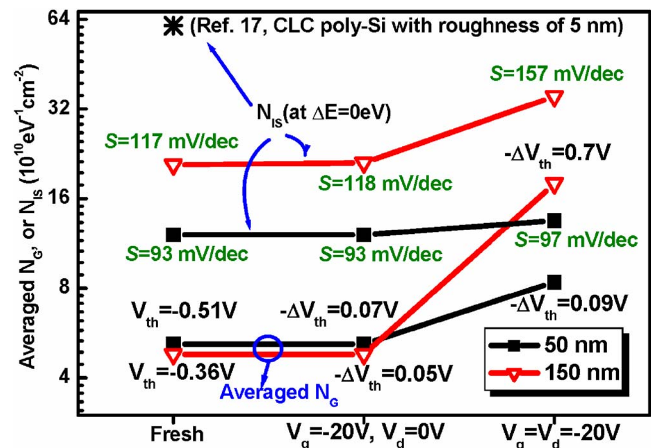

FIG. 4. (Color online) Threshold voltage, subthreshold slope, areal grain, and interface trap-state densities at different energetic levels in fresh and stressed TFTs on CLC poly-Si with thicknesses of 50 and 150 nm.

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all samples was under 3×10^{10} cm^{-2} eV^{-1}, using an n_{GT} of 2×10^{15} cm^{-3} eV^{-1}; this value is one order of magnitude lower than the N_T obtained from S. Accordingly, on such an epilike poly-Si, interface trap-state densities, N_{IS} (Ref. 17) given by the formula $N_{IS}=N_T-N_G$,[18] at $\Delta E\sim0$ eV, and related to channel roughness almost completely determine the S of fabricated TFTs (see Fig. 4). Furthermore, the quality of the interface reportedly affects the deep states of grain traps,[5,19] such that the changes in n_{GT} due to HCS at the deep energetic level were observed. Very small changes in S and N_{IS} at the midgap energetic level in thin channels due to HCS were consistent with $V_{\rm th}$ and n_{GT} as well as the averaged N_G at the deep energetic level.

For an Al–SiO_2-bulk Si (metal-oxide-semiconductor) structure, a gate stress of −20 V merely shifts the flatband voltage of 30 mV; the value was much lower than those measured in hot-carrier stressed TFTs on CLC poly-Si [Figs. 3(b), 3(c), and 4]. This result indicates that charge trapping in gate dielectrics barely affects HCS-induced degradations in the present devices. No hysteresis was observed in the transfer characteristics (Fig. 2). Therefore, hysteresis was ruled out as a major mechanism in $\mu_{\rm FE}$ and $V_{\rm th}$ degradation. As a result, channel or interface defects were responsible for HCS-induced degradations.

In HCS, a high drain bias ensures that carriers attain sufficient energy from the field to be injected into the gate dielectrics and to generate defect sites at the interface.[13,20] Hence, introducing a very low drain bias in HCS, namely, gate-bias stressing,[20] facilitates the observation of the role of channel defects on the stability of electrical parameters of stressed devices. Stressed at $V_g=-20$ V and $V_d=0$ V, substantially reduced changes in V_t and grain trap-state densities were observed in both channels [see Figs. 1, 3(c), and 4] and explained by the fact that highly crystalline CLC poly-Si has a few densities of tail states to accommodate accumulated carriers, inhibiting markedly deep-state generation in channel layers by bias stressing.[20,21] Under gate-bias stressing (or HCS with no drain bias), in thicker channels with greater channel crystallinity, the carrier-trapping effect is weaker because grain defects are fewer and so the change in V_t is smaller and larger exponents are associated with the $\Delta V_{\rm th}$, as observed in currently used devices [Figs. 3(c) and 4].[6]

A slightly roughened CLC polysilicon/SiO_2 either provides trap sites or establishes a local electric field, enhancing hot-carrier injection.[3,18–20] Under HCS with high drain bias, charge trapping at interfaces generates extra states, in response to increased interface and grain deep-state densities (Figs. 1 and 4). For thicker channels with greater channel crystallinity, the larger changes in electric parameters, deep-state densities of grain defects and interface trap-state densities at the midgap energetic level due to HCS, are attributed to their poorer interface quality (Figs. 1, 3, and 4). The poorer channel interface in thick channels than in thin channels causes the charge trapping mechanism to affect the $V_{\rm th}$ degradation more for thicker channels, the result of which agrees with the smaller exponents that are associated with the $\Delta V_{\rm th}$ of these thicker channels. In thin channels with surfaces with a roughness of 5.1 nm, associated with increased laser power, the power-law exponents in $V_{\rm th}$ degradation by HCS were reduced to 0.32 [Fig. 3(b)], a finding which is consistent with interface-quality-dominated degradation.

In summary, channel roughness, rather than high crystalline channel layers, dominated the stability of high-hole-mobility thin-film transistors on epilike silicon channels formed by CLC. On such single-grainlike channels, an increase in channel roughness with channel thickness enhances charge trapping at the interfaces, generating substantially more deep states at the deep energetic level. Hence, on thin channels with ultrasmooth surfaces, TFTs during HCS exhibited negligibly changed electrical parameters and generated fewer deep states than those on thick channels.

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