High-Temperature Stable Ir_xSi Gates With High Work Function on HfSiON p-MOSFETs

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***Abstract*—A novel 1000 °C-stable Ir_xSi gate on HfSiON is shown for the first time with full process compatibility to current very-large-scale-integration fabrication lines and proper effective work function of 4.95 eV at 1.6-nm equivalent-oxide thickness. In addition, small threshold voltages and good hole mobilities are measured in Ir_xSi/HfSiON transistors. The 1000 °C thermal stability above pure metal (900 °C only) is due to the inserted 5-nm amorphous Si, which also gives less Fermi-level pinning by the accumulated metallic full silicidation at the interface.**

***Index Terms*—Full silicidation (FUSI), HfSiON, Ir_xSi.**

I. Introduction

TO CONTINUE down-scaling very-large-scale-integration (VLSI) technology and increase the integration density, high-κ gate dielectrics are needed for MOSFETs to reduce the large dc power consumption from gate leakage current [1]–[10]. In addition, metal gates are required to eliminate poly gate depletion. However, metal-gate/high-κ CMOSFETs show undesired high threshold voltages (V_t), which is opposite to the VLSI scaling trend. This phenomenon is known as "Fermi-level pinning" [1], although the background physics may be attributed to interface dipole and/or charged defects [1], [8]. To compensate this Fermi-level pinning effect, high-work-function metal electrodes larger than the 5.2 eV of p^+ poly-Si are needed. However, only Ir (5.27 eV) and Pt (5.65 eV) in the Periodic Table [11] can meet this requirement, which make the metal-gate/high-κ p-MOSFETs especially challenging [1], [2]. Ir is more preferable than Pt due to a simpler etching process by reactive ion etching [12], [13]. Unfortunately, large metal diffusion through high-κ dielectrics was found in pure Ir gates after 1000 °C rapid thermal annealing (RTA), which caused p-MOS device failures [7], [8]. Previous attempts by using Ir–N to improve the thermal stability also failed due to weak Ir–N bonding strengths, where Ir–N decomposition and penetrating high-κ dielectrics were found after high-temperature RTA [8]. Another possibility is using low-temperature full silicidation (FUSI) gates [3]–[9]. However, the p-MOS devices incorporating high work function Pt_xSi or Ir_xSi still failed to integrate into the CMOS SALICIDE process due to the lack of required selective wet etching of Pt or Ir during SALICIDE.

To overcome this problem, we have proposed and demonstrated a new high-temperature stable Ir_xSi FUSI gate on high-κ HfSiON. This is different from the low-temperature FUSI process [3]–[6] since it is formed first before ion implantation and undergoes 1000 °C RTA thermal cycle for implant activation. To achieve this high-temperature stability goal, additional Si was inserted between Ir and high-κ HfSiON, where less Fermi-level pinning was obtained by forming Ir-rich Ir_xSi gates. High-κ HfSiON also has good metal-diffusion barrier property [14], [15], which is similar to our previous HfAlON [7], [8], but it has the important advantage of better compatibility with currently used SiON gate dielectric with added Hf for higher κ value. After 1000 °C RTA, Ir_xSi/HfSiON p-MOSFETs show good device integrity of a high effective work function $(\phi_{\text{m-eff}})$ of 4.95 eV, a small V_t of -0.15 V, and a peak hole mobility of 84 $\text{cm}^2/\text{V}\cdot\text{s}$. These results are compatible with and even better than the best reported metal-gate/high-κ p-MOSFETs [5]–[9].

II. Experimental Procedure

The gate-first Ir_xSi/HfSiON p-MOSFETs were fabricated on 12-in N-type Si wafers with resistivity of 1–10 $\Omega\cdot$cm. After RCA cleaning, 4-nm HfSiO dielectric $(\text{Hf}/(\text{Hf}+\text{Si}) = 50\%)$ was deposited by atomic-layer deposition. HfSiON gate dielectric was formed by applying NH_3 plasma surface nitridation on HfSiO [16]. After postdeposition annealing, 5–30-nm amorphous Si and 20–30-nm Ir were deposited by physical vapor deposition (PVD) [7]. For Ir/Si/HfSiON capacitors, a 1000 °C RTA was applied for 10 s to form Ir_xSi gates. For MOSFETs, additional 400-nm Si was deposited on top of Ir/Si to avoid ion implantation penetrating through the thin Ir/Si. After gate definition, Boron was implanted at 25-KeV energy and 5×10^{15} cm^{-2} dose, and activated at 1000 °C RTA for 10 s. Meanwhile, Ir_xSi was also formed during RTA, where the $x = 3$ was determined by X-ray diffraction measurements. Note that this process is different from the low-temperature FUSI process [3]–[6], and such a simple self-aligned process is fully compatible to current VLSI lines. Secondary ion-mass spectroscopy (SIMS) was measured to study the Ir distribution profile. The fabricated p-MOSFETs were further characterized

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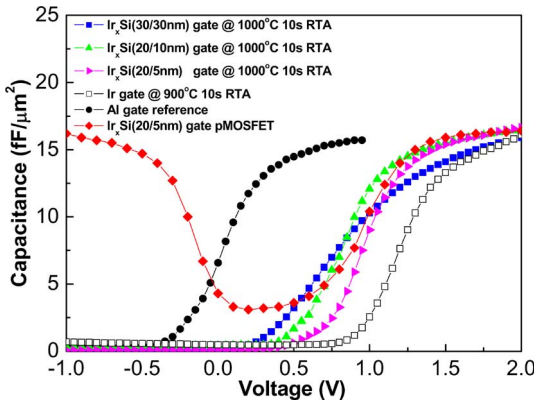

Fig. 1. C–V characteristics of HfSiON/n-Si with Ir$_x$Si-, Ir-, and Al-gate capacitors. The device areas are 100 × 100 μm.

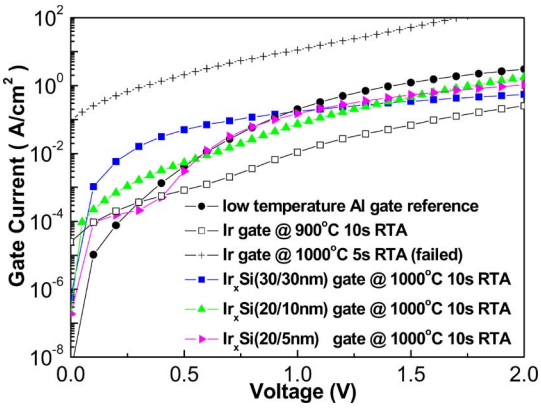

Fig. 2. J–V characteristics of HfSiON/n-Si with Ir$_x$Si-, Ir-, and Al-gate capacitors.

by capacitance–voltage (C–V) and current–voltage (I–V) measurements. For comparison, Al and Ir-gated MOS capacitors on HfSiON were also fabricated. To prevent the different oxide charge from causing error in $\phi_{\text{m-eff}}$ extraction, HfSiON was subjected to the same thermal cycle (1000 °C RTA for 10 s) before Al gate deposition.

III. Results and Discussion

Fig. 1 shows the measured C–V characteristics of Ir$_x$Si, Ir, and Al gates on HfSiON MOS devices. Low-temperature Al-gated HfSiON capacitors were used as a reference because pure metal deposited at low temperature has little interface reaction with high-κ dielectrics to cause Fermi-level pinning [10]. In addition, the flatband voltage (V_{fb}) is expressed as

$$\begin{aligned} V_{\text{fb}} &= \phi_{\text{ms}} - Q_f/C_{\text{ox}} \\ &= (\phi_m - \phi_s) - (Q_f/\varepsilon_o k_{\text{ox}})t_{\text{ox}} \\ &= (\phi_m - \phi_s) - (Q_f/\varepsilon_o k_{\text{SiO2}})\text{EOT} \end{aligned} \quad (1)$$

where ϕ_m and ϕ_s are the work functions for metal gates and Si, respectively. Q_f, C_{ox}, t_{ox}, and equivalent-oxide thickness (EOT) are the oxide charge, capacitance, physical thickness, and EOT for high-κ dielectrics, respectively. Since HfSiON has the same thermal cycle (1000 °C RTA for 10 s) before Al gate formation, the Q_f effect should be similar to FUSI gates. Therefore, the principal effect of V_{fb} shift might be due to the difference of effective ϕ_m. In comparing with the conventional $\phi_{\text{m-eff}}$ extraction from V_{fb}-t_{ox} or V_{fb}-EOT plot, this method uses a simple process without fabricating MOS devices with various t_{ox} and measuring the thickness carefully by transmission electron microscopy (TEM). Since the capacitance value or EOT of ∼1.6 nm is the same for various gated HfSiON capacitors, the shifts of C–V curves with different gate electrodes are attributed to the different work functions. Ir/HfSiON after 900 °C RTA has a large V_{fb} shift of 1.15 V to control low-temperature Al gates (4.1 eV $\phi_{\text{m-eff}}$), which gives the required high $\phi_{\text{m-eff}}$ of 5.25 eV. This work-function value is also close to the reported 5.27 eV for Ir [11], indicating no pinning effect in pure metal Ir gates. This is due to weak bonding strengths of Ir–O or Ir–N that reduce the Fermi-level-pinning-related interface reaction [8]. However, Ir/HfSiON capacitors failed after 1000 °C RTA. To improve thermal stability, additional amorphous Si of 5–30 nm was inserted between Ir and HfSiON. Good C–V characteristics were measured for Ir$_x$Si/HfSiON devices after the required 1000 °C RTA for implant activation, although thermal stability was traded off at the Fermi-level pinning caused by the Si/HfSiON interface reaction. However, the continuously increasing V_{fb} toward the value of pure Ir gates was observed by decreasing the inserted amorphous Si layer, and a high $\phi_{\text{m-eff}}$ of 4.95 eV was obtained for Ir$_x$Si/HfSiON devices with the inserted 5-nm amorphous Si. This 4.95 eV $\phi_{\text{m-eff}}$ is significantly larger than Ni$_3$Si/HfSiON [6]. This result is also slightly better than previous Ir$_x$Si/HfAlON [7] due to thinner amorphous Si on high-κ dielectrics. Slow depletion for Ir$_x$Si/HfSiON devices with 30-nm amorphous Si may be due to nonuniform silicidation as examined by TEM, where locally unreacted Si was found to cause voltage drop in gate electrodes. The formation of FUSI gates is evident from the same inversion and accumulation capacitances measured in MOSFETs.

Fig. 2 shows the J–V characteristics of Ir$_x$Si, Ir, and Al gates on high-κ HfSiON devices. After 1000 °C RTA, Ir/HfSiON devices failed due to large leakage current. In sharp contrast, Ir$_x$Si gates on HfSiON showed successfully improved thermal stability to 1000 °C RTA, which is evident from low leakage current comparable with p$^+$ poly-Si gates [17]. Here, high-temperature thermal cycle is required for dopant activation after ion implantation.

The measured large V_{fb} shift of Ir$_x$Si is supported by SIMS profile, as shown in Fig. 3. Here, Ir segregation toward amorphous Si was measured to form Ir$_x$Si on HfSiON surface. Such FUSI formation directly on high-κ dielectrics is known to reduce Fermi-level pinning [6]–[8]. Therefore, good thermal stability of 1000 °C RTA, a reasonable high $\phi_{\text{m-eff}}$ of 4.95 eV, and a low gate dielectric leakage current can be simultaneously achieved in Ir$_x$Si/HfSiON MOS capacitors. To the best of our knowledge, this is the highest reported $\phi_{\text{m-eff}}$ in high-κ Hf-based oxide [5]–[8]. These are the few methods to achieve a high $\phi_{\text{m-eff}}$ in Hf-based oxide p-MOS devices. Although the V_{fb} tuning can be reached by impurity segregation in FUSI/SiON, this method becomes less useful in high-κ metal oxide due to the stronger interface reaction. In the following, we will study Ir$_x$Si/HfSiON devices with the thinnest 5-nm amorphous Si. This is because the V_{fb} of thicker Si layer is too low for p-MOSFET application.

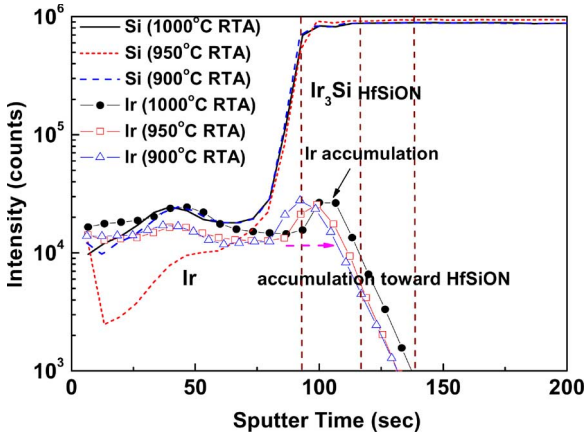

Fig. 3. SIMS profile of Ir_3Si gates on HfSiON at different RTA temperatures. The Ir_3Si that accumulated toward HfSiON interface is found to unpin the Fermi level.

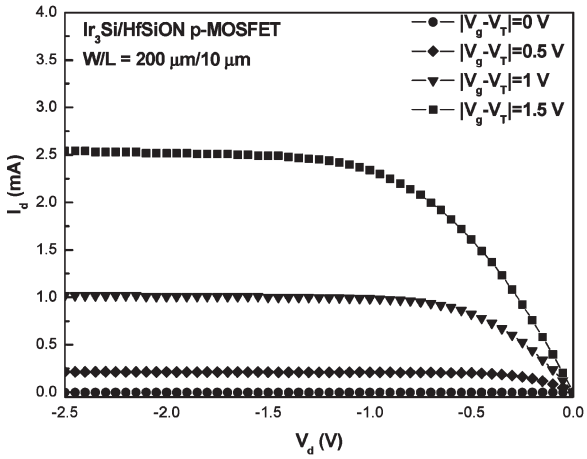

Fig. 4. I_d–V_d characteristics of Ir_3Si/HfSiON p-MOSFETs.

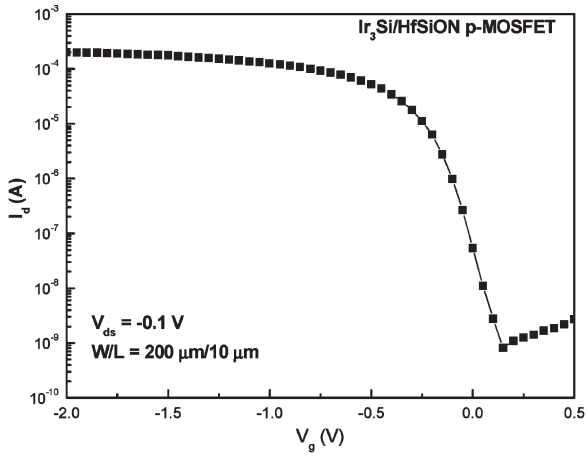

Fig. 5. I_d–V_g characteristics of Ir_3Si/HfSiON p-MOSFETs.

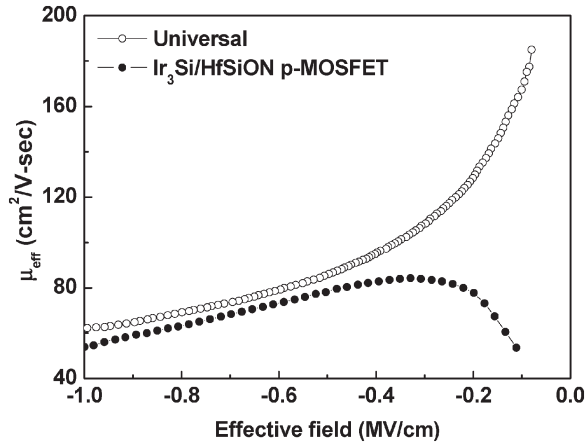

Fig. 6. Extracted hole mobilities from I_d–V_g characteristics of Ir_3Si/HfSiON p-MOSFETs.

Fig. 4 shows the transistor I_d–V_d characteristics as a function of V_g-V_t for 1000 °C RTA Ir_xSi/HfSiON p-MOSFETs. The well-behaved I_d–V_d curves of Ir_xSi/HfSiON transistors show little device performance degradation.

Fig. 5 shows the I_d–V_g characteristics of Ir_xSi-gated p-MOSFETs with HfSiON as the gate dielectric. A small V_t as low as -0.15 V is obtained from the linear I_d–V_g plot, which is consistent with the large $\phi_{\text{m-eff}}$ of 4.95 eV from C–V curves and the Ir accumulation on HfSiON from SIMS.

Fig. 6 shows the extracted hole mobilities versus gate electric fields from the measured I_d–V_g data of Ir_xSi/HfSiON p-MOSFETs. High hole mobilities of 84 and 53 $\text{cm}^2/\text{V}\cdot\text{s}$ are obtained at peak value and 1 MV/cm effective field for Ir_xSi/HfSiON p-MOSFETs, respectively, which is compatible with the published data in the literature [5]–[8]. Good hole mobilities also indicate low Ir diffusion through HfSiON to inversion channel, even though excess Ir is necessary to prevent unreacted amorphous Si from causing gate depletion or increased Fermi-level pinning. Therefore, a high $\phi_{\text{m-eff}}$, a small V_t, and good hole mobilities are simultaneously achieved in Ir_xSi/HfSiON p-MOSFETs with additional merit of process compatible to current VLSI lines.

IV. Conclusion

Good device performance of Ir_xSi/HfSiON p-MOSFETs is shown by a high $\phi_{\text{m-eff}}$ of 4.95 eV, a small V_t of -0.15 V, a peak hole mobility of 84 $\text{cm}^2/\text{V}\cdot\text{s}$, and 1000 °C RTA thermal stability with the advantage of full process compatible to current VLSI lines.

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