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# A floating gate design for electrostatic discharge protection circuits

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**Abstract**

In this paper, a circuit design method for electrostatic discharge (ESD) protection is presented. It considers the gate floating state for ESD protection and negatively gate biased for leakage suppression under normal operations. The circuit is achieved by adding a switch device and a negatively biased circuit at the gate of ESD protection devices. Robustness and leakage of ESD protection circuit are improved. The circuit suits thin thickness of gate oxide of complementary metal oxide semiconductor (CMOS) devices due to an elimination of oxide damage. This approach benefits design of very large-scaled integration circuit and implementation of system-on-a-chip with sub-100 nm CMOS devices.
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*Keywords:* Electrostatic discharge; Robustness; Floating gate; Gate grounded; Leakage current; Negatively biased circuit; Sub-100 nm CMOS device and circuit

## 1. Introduction

Device scaling and supply voltage reduction continuously maintain high density and high-speed application of very large-scaled integration (VLSI) circuit [1,2]. Along with the voltage reduction, the threshold voltage ($V_{\text{th}}$) of metal-oxide semiconductor field-effect transistors (MOSFETs) is simultaneously lowered to support a desired current density [3]. Unfortunately, the threshold voltage scaling results in a high-leakage current in VLSI circuit. Circuit design is a compromise between power consumption and circuit speed [4]. Besides leakage problems, how to obtain an effective protection against electrostatic discharge (ESD) becomes one of challenges [5,6]; in particular, for widely used gate grounded MOSFET structures [7–9]. When using a gate grounded MOSFET as protecting device, the parasitic bipolar transistor (BJT) turned on by drain junction breakdown of MOSFET is the major mechanism of circuits protecting. Unfortunately, in lowering the operation voltage, thickness of the gate oxides at input devices has to be scaled down to maintaining similar driving current [10,11]. Eventually, the breakdown voltage of the gate oxides is lower than the breakdown voltage of the drain junction of the MOSFET in protection circuit. The circuit fails before the gated devices are activated.

In this paper, a gate changeable MOSFET is designed for obtaining low leakage and high ESD robustness protection circuit. We demonstrate an ESD protection circuit which features a changeable gate status. With adding a switch and a negatively biased circuit, the proposed ESD protection works as a floating gate state to obtain an easier triggered on and an improved ESD robustness. At the same time, leakage current of devices can be suppressed through a negatively gate bias. This design methodology makes our ESD protection circuit more robust and reliable. This design consideration is useful in ESD protection design; especially for the sub-100 nm CMOS VLSI circuit design. ESD robustness can be significantly improved without adding complicated circuits.

This paper is organized as follows. In Section 2, we state the device fabrication and characteristic measurement. In Section 3, we discuss the leakage and ESD. In Section 4, we focus on the design of switch circuit for the purpose of floating gate. Finally, we draw the conclusions.

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## 2. Device fabrication and measurement

The fabrication process used in this work is a dual oxide CMOS process that has two kinds of oxides; one is 2.6 nm thicken for 1.2 V devices and the other is 7.0 nm for 3.3 V devices. Conventionally, the 3.3 V devices are used in designing input/output (I/O) and ESD cells; therefore, we use the 3.3 V devices in our experiments. Two kinds of test structures are used, shown in Fig. 1, one is the gate grounded device, and the other is the floating gate device. In the experiment, the leakage characteristics are measured by HP-4156B semiconductor analyzer, where the resolution of current is 50 fA. Additionally, the ESD robustness is verified by using the Keytech Zapmaster human body model (HBM) tester and Barth TLP 4200 with a pulse width of 100 ns. Finally, the failure analysis is done by using secondary electron microscope (SEM).

## 3. The leakage and ESD concerns

We show the leakage current and ESD robustness issues of a 0.13 μm CMOS technology. We, firstly, present the leakage problem of the gate grounded MOSFET; furthermore, the benefits of the gate switchable one are also demonstrated. We will also show a better ESD robustness obtained by the additional gate controlling circuit.

Reduction of the threshold voltage amplifies the leakage current of the device. It is caused from a sub-threshold swing (SS) of MOSFETs keeping almost constant (about 100 mV/decade). For all technology generations, generation of drain current requires a minimum threshold level when a 0.7 V gate voltage is applied. In other words, a decrement of threshold voltage means an parallel shift of current–voltage ($I$–$V$) to left. As shown in Fig. 2, if we want to design our device to have a minimum current at 0 V, we must have a threshold voltage of 0.7 V. Consequently, our device has a threshold voltage of 0.5 V that we must have a minimum current at −0.2 V. It should be noticed that an n-type MOSFET with $V_{th} = 0.5$ V biased at $V_g = 0$ V will have a leakage current about two-order higher than that biased at −0.2 V. This result shows one of important issues of the gate grounded design for ESD protection circuit that suffers a high-leakage current. It becomes much more serious when the $V_{th}$ is further reduced.

Supplying a negative bias to the gate electrode of ESD protection greatly suppresses the leakage current. The leakage current under different negative gate biases is shown in Fig. 3. Applying a −0.1 V bias at the gate electrode, compared with the zero biased one, reduces about one-order magnitude of leakage current. There is a two-order reduction on the leakage current for the case of −0.2 V. We note that the suppression of leakage current saturates at −0.2 V. It suggests that a −0.2 V gate bias is a candidate for reducing leakage current. This observation is consistent with the $I$–$V$ characteristics shown in Fig. 2 that drain current is almost keeping as a constant when the gate voltage is smaller than −0.2 V. When using the negatively biased gate design for ESD protection circuit, gate induced drain leakage current (GIDL) effect must be considered. The GIDL effect will cause an unwanted leakage current when the gate electrodes of device are negatively biased. We design our negatively biased voltage before the GIDL dominating the leakage current.

Scaling down of devices is significantly related to many key technologies. Among technologies, shallow junction and thin gate oxide are the most important concerns in suppressing the short channel effects. However, scaling down of gate oxide encounters ESD problem for gate grounded MOSFETs. It is due to that ESD protection is provided by turning on parasitic bipolar transistor (BJT) of MOSFET through drain junction breakdown. Thin thickness of gate oxide will also decrease the breakdown voltage of the gate oxide. As a result, the breakdown voltage of the

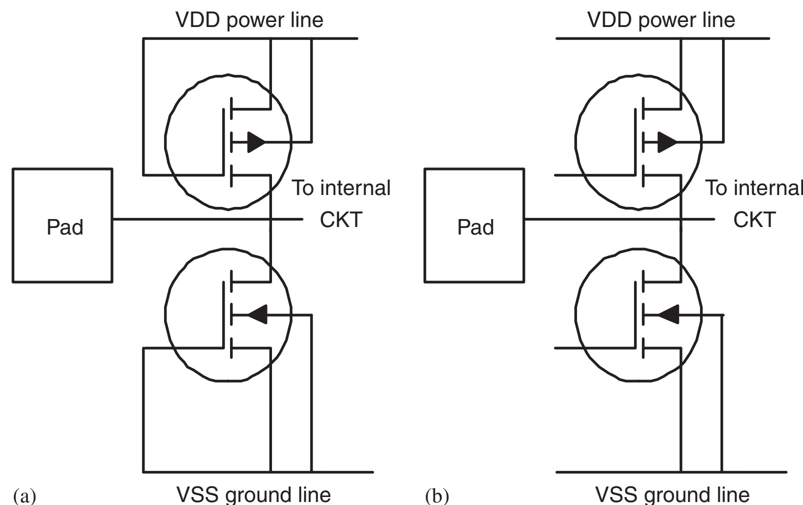


Fig. 1. Schematic plots of the (a) grounded and (b) floating gate ESD protection circuits.

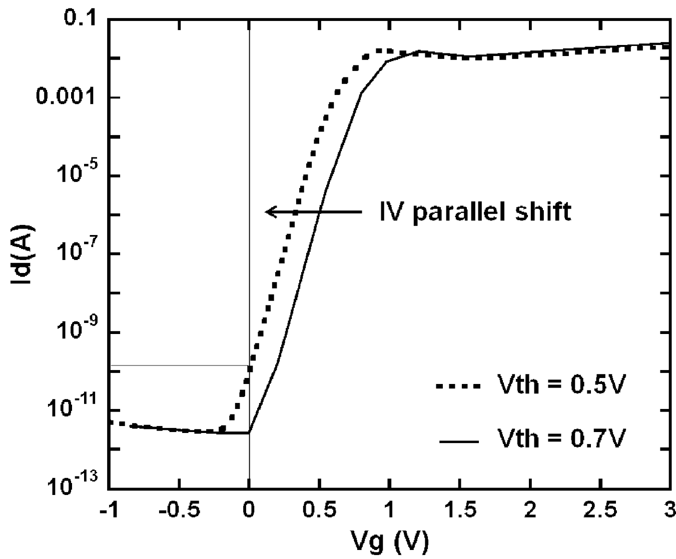


Fig. 2. The $I_d$–$V_g$ characteristics of the NMOSFET with respect to different $V_{th}$.

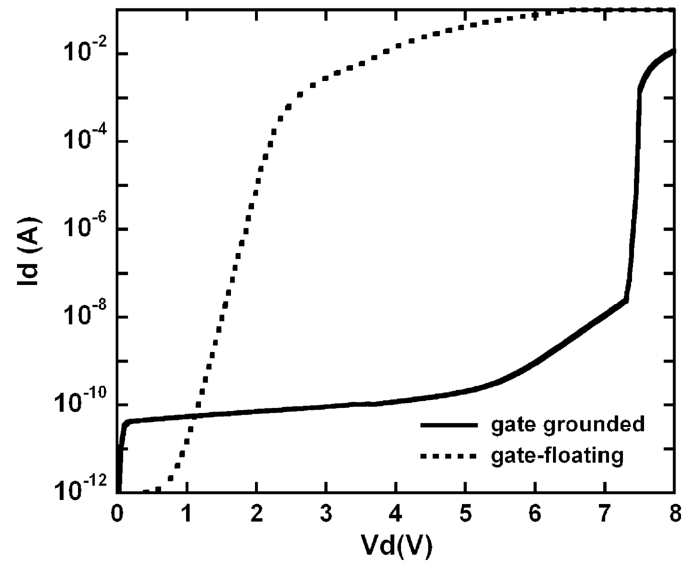


Fig. 4. The $I$–$V$ characteristics of the gate grounded and floating gate MOSFETs.

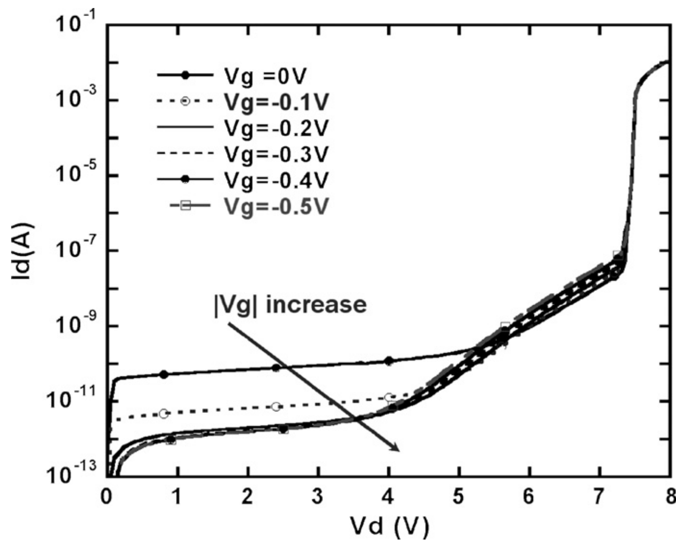


Fig. 3. Leakage characteristics of the NMOSFET, where $V_{th} = 0.5\,V$.

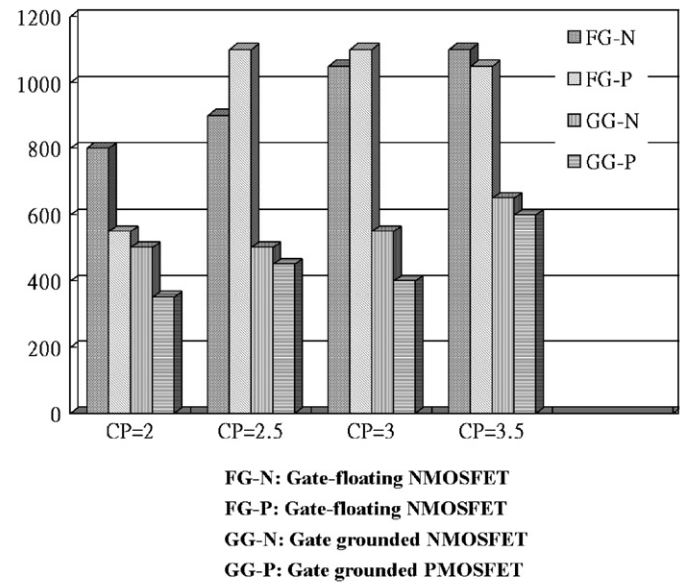


Fig. 5. The ESD robustness of the gate grounded and floating gate MOSFETs. For each plot of CP, bars from the left to right are FG-N, FG-P, GG-N, and GG-P, respectively.

drain junction is higher than that of the gate oxide. Under this situation, the gate oxide is totally damaged because the parasitic BJT does not turn on before the breakdown of gate oxide.

A floating gate structure, an additional controlling circuit, is studies for preventing ultra-thin gate oxide from ESD damage. It provides a floating state under ESD stressing. Fig. 4 exhibits the $I$–$V$ characteristics of the gate grounded and floating gate. This is an interesting observation that we can have a device with high turn on efficiency. Compared with the grounded one, the turn on voltage could be reduced about 5.0 V. We note that the circuit design works at the sub-100 nm generation where the breakdown voltage of gate oxide is around 4.0 V.

Besides a lower turn on voltage, the floating gate MOSFET also benefits the issue of gate oxide damage under ESD events. When gate electrodes are in floating state, the voltage drop across gate oxide can be neglected. It eliminates possible issues of gate oxide damage. A comprehensive study is done in demonstration the superior ESD robustness. Various spaces between contact holes to polysilicon gate edge (CP) are designed. The spaces are traditionally defined in controlling the non-silicide region at drain side; in this experiment, the non-silicide width is equal to CP-0.2 um. It is also clearly found that the ESD robustness of both N- and P-MOSFETs is increased as the space is enlarged [7,8]. Fig. 5 shows an improvement of the

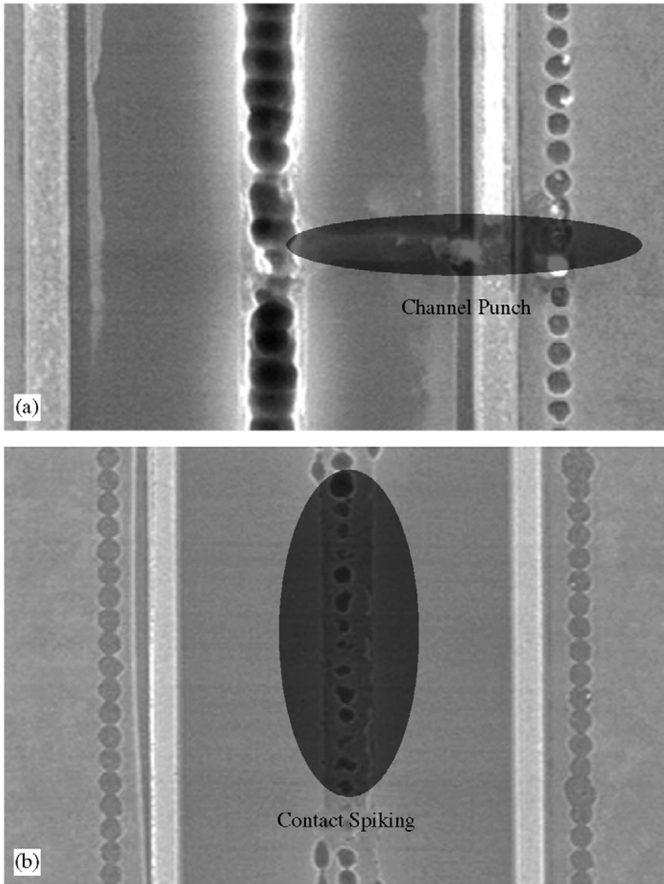


Fig. 6. The SEM exhibits different devices failure mode of (a) gate grounded and (b) floating gate NMOSFETs.

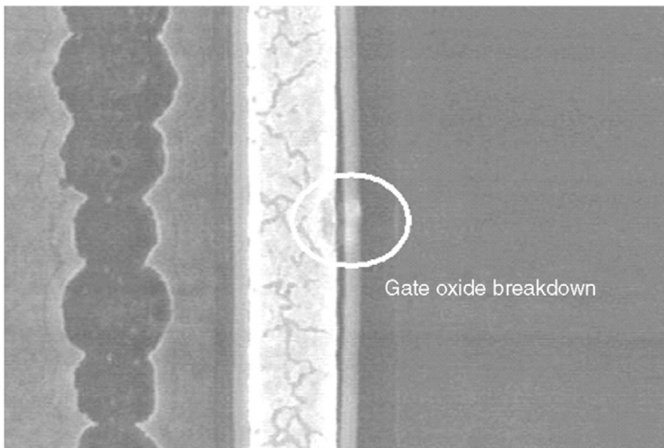


Fig. 7. The SEM image of the gate oxide breakdown of the grounded gate MOSFET.

floating gate structures; especially for the devices have a larger CP. An enlargement of CP makes the gate grounded devices having a slight ESD robustness enhancement; on the other hand, it strengthens the floating gate ones. The ESD robustness of the floating gate devices is dominated by the devices strength of parasitic BJT. The strength of BJT is corresponding to the area of collect. A larger the collect junction area contributes an improved the ESD robustness.

Difference between the gate grounded and the floating gate can be further inspected from SEM images shown in Fig. 6. From the SEM images, shown in Fig. 6, it is found that the major failure mechanisms of the gate grounded and the floating gate devices are quite different. The channel punch through is responsible for ESD failure of the gate grounded device; on the contrast, the contact spiking dominates devices breakdown of the floating gate one. The floating structure suppresses the channel electric field and reduce damage and high temperature at channel region. The floating gate structure is also keeping device away from gate oxide breakdown. Fig. 7 shows the gate

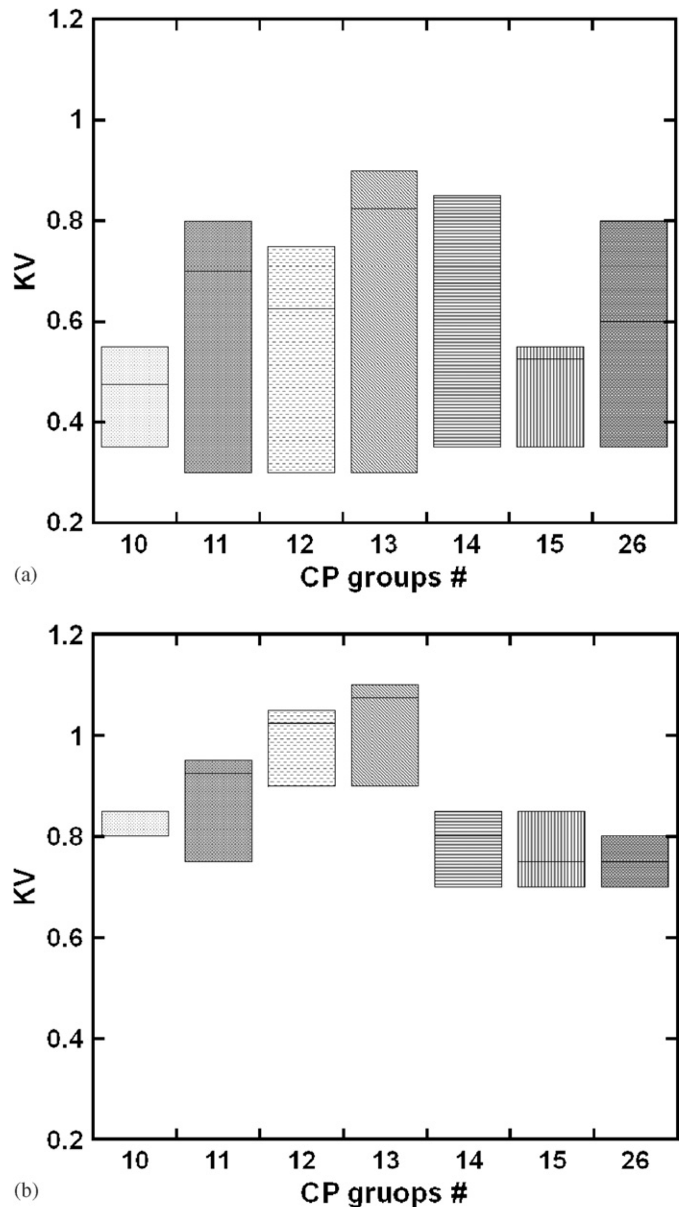


Fig. 8. The ESD robustness distributions in (a) the gate grounded NMOSFETs and (b) the floating gate NMOSFETs.

oxide breakdown during the ESD stressing of the gate grounded device. The effect is found for a 7.0 nm thickness of gate oxide. We believe that it takes place frequently when the device is with a more thinner thickness of gate oxide.

The gate oxide breakdown of the grounded gate devices will result in an issue of ESD design. Because it has an unexpected device and circuit failure under ESD testing. The failure randomly appears and is a difficulty in qualification of ESD robustness. Fig. 8 shows the ESD robustness distribution in the grounded gate and the floating gate devices. Comparison between these two figures shows that the floating gate device has a tight ESD distribution, which reflects a better consistence between ESD devices. It also corresponds to a lower uncertainty in ESD protection circuit design and qualifications. A wider ESD distribution presented in the gate grounded devices.

## 4. Switch circuit for floating gate

The floating status will cause a high-leakage characteristic of the circuit. Therefore, a switch circuit is needed to monitor and change the gate status from floating in ESD protection to grounded state for the leakage control. Comparison between Figs. 1 and 9 shows the different among the gate grounded, gate floating, and gate changeable MOSFET for the usage of ESD protection. The switch circuit for the NMOSFET protection device is the device with its gate tied to power line through a resistor. Similar design is also observed in PMOSFET. We note that the switch circuit is useful for the ESD robustness enhancement.

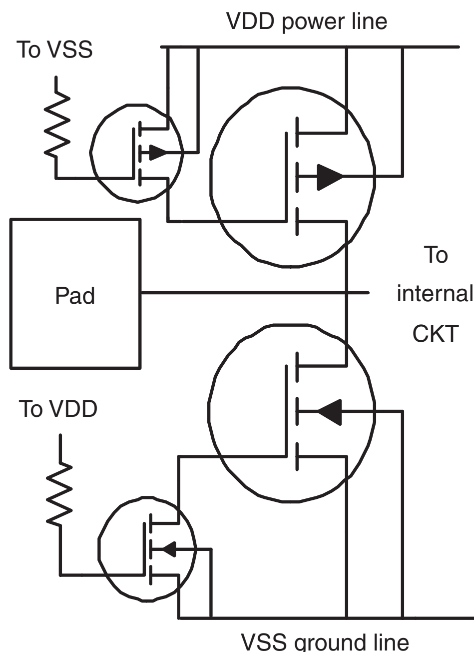


Fig. 9. A schematic plot of the switched gate ESD protection circuit.

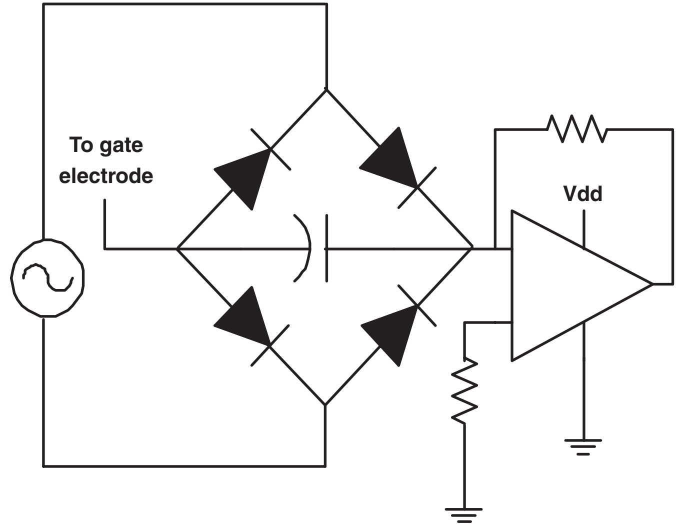


Fig. 10. The proposed negative biased circuit.

We have discussed leakage problem for the scaled down devices. The major issue is caused from the fact that threshold voltage becomes lowering while the sub-threshold swing keeping unchanged. Accordingly, the minimum leakage current does not occur at zero biased gates, but for a small negatively biased gate. Fig. 10 is a proposed circuit for generation of negative voltage. The circuit could be embedded into VLSI circuit by using standard CMOS technology. In addition, we do not have to put this negatively biased circuit into each ESD protection device. We design one biased circuit and it is connected to all the ESD devices through metal lines. Voltage level of the negative biased circuit can be controlled by the amplitude of the AC signal. There are two approaches in designing the ESD protection devices with changeable gate states of floating and negatively biased. The first one is directly connecting the negatively biased circuit to the gate of the ESD protection devices. The other one is tying the negatively biased circuit through a switch of MOSFET device. For the negatively biased circuit can be connected to many ESD protection devices; therefore, a switch added approach is recommended to reduce cross talk among ESD devices.

## 5. Conclusions

In this paper, a new approach to ESD protection circuit design with a changeable gate status has been proposed. The proposed ESD protection worked as a floating gate state to obtain an easier triggered on and a better ESD robustness by adding a switch and a negatively biased circuit. It has been found that the device leakage current was suppressed through a negatively gate bias. This technique has demonstrated robust and reliable characteristics for the designed ESD protection circuit without any

complicated additional circuits. System-on-a-chip (SOC) features an integration of advanced VLSI circuits and sub-systems on a chip. Therefore, it complicates the design issues and fabrication processes, in particular the ESD is becoming a challenge for nanodevice and SOC era. The work presented here for ESD protection circuit provides an alternative for VLSI circuit design and SOC applications with sub-100 nm CMOS devices.

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