Effect of Gate Sinking on the Device Performance of the InGaP/AlGaAs/InGaAs Enhancement-Mode PHEMT

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***Abstract*—An enhancement-mode InGaP/AlGaAs/InGaAs pseudomorphic high-electron mobility transistor using platinum (Pt) as the Schottky contact metal was investigated for the first time. Following the Pt/Ti/Pt/Au gate metal deposition, the devices were thermally annealed at 325 °C for gate sinking. After the annealing, the device showed a positive threshold voltage ($V_{\rm th}$) shift from 0.17 to 0.41 V and a very low drain leakage current from 1.56 to 0.16 μA/mm. These improvements are attributed to the Schottky barrier height increase and the decrease of the gate-to-channel distance as Pt sinks into the InGaP Schottky layer during gate-sinking process. The shift in the $V_{\rm th}$ was very uniform across a 4-in wafer and was reproducible from wafer to wafer. The device also showed excellent RF power performance after the gate-sinking process.**

***Index Terms*—Buried gate, enhancement-mode (E-mode), InGaP, platinum (Pt), pseudomorphic high-electron mobility transistor (PHEMT), single voltage supply.**

I. Introduction

ADVANCED wireless communication systems require high RF performance power amplifiers with low supply voltage, high power-added efficiency (PAE), and long stand-by time. Enhancement-mode pseudomorphic high-electron mobility transistor (E-mode PHEMT) is getting popular as a power device for wireless communication due to single-voltage operation, low knee voltage, and high PAE at low drain bias. The E-mode PHEMTs also have an adequate low drain leakage current during stand-by time and can be used with the elimination of the negative bias voltage; all these can extend the battery life time used in the E-PHEMT power amplifiers [1]–[4].

The InGaP/AlGaAs/InGaAs PHEMTs take the advantages of the high energy band gap of InGaP and the excellent etching selectivity between InGaP and GaAs. These advantages result in higher breakdown voltage, low gate leakage current, and high etching selectivity for the device. Furthermore, the use of InGaP/AlGaAs/InGaAs structure enhances the conduction band discontinuity between the spacer and the channel layer than that of the conventional InGaP/InGaAs structure which improves the carrier confinement and results in higher current density of the devices [5], [6]. The Hall mobility of the InGaP/AlGaAs/InGaAs PHEMTs is also higher than that of the InGaP/InGaAs PHEMTs due to the smoothness of the AlGaAs/InGaAs interface [7].

In this letter, platinum (Pt) buried gate technology is used in E-mode InGaP PHEMT fabrication. The motivations are more flexible to reduce source resistance (R_s) [8] and a high Schottky-barrier height demonstrated in the Pt/InGaP [9]. In addition, the Schottky-barrier height increases as Pt diffused into the Schottky layer, which also caused the gate leakage current reduction [10]. However, the use of Pt buried gate on GaAs-based E-mode PHEMT fabrication was never reported. In this letter, the Pt buried gate technology was used to fabricate the InGaP/AlGaAs/InGaAs E-mode PHEMTs.

II. Device Fabrication

The E-mode InGaP/AlGaAs/InGaAs PHEMT structure was grown by metal–organic chemical vapor deposition on a 4-in GaAs substrate. The active area of the device was defined by wet chemical mesa etching. The Au/Ge/Ni/Au ohmic contacts were formed by electron-beam (e-beam) evaporation. After rapid thermal annealing at 350 °C for 1 min, the contact resistance measured by the transfer length method was 0.1448 $\Omega \cdot$ mm. The bilayer resists that consisted of polymethylmethacrylate (PMMA), and PMMA-methacrylic acid was used for gate formation. Citrate acid/H_2O/H_2O_2 solution was used for gate recess, and the recess etching was stopped at the InGaP layer due to the high selectivity between InGaP and GaAs. The gate metals consist of Pt(20 nm)/Ti(100 nm)/Pt(100 nm)/Au(300 nm), which were deposited by e-beam evaporator. After T-gate formation, 100-nm thick silicon nitride film was deposited by plasma-enhanced chemical vapor deposition at 250 °C for 10 min as the passivation layer. Finally, thermal annealing at 325 °C for 1 min was performed for gate sinking to further reduce the drain and gate leakage currents.

III. Pt and InGaP Interfacial Reactions

In order to understand the interfacial reaction between the Pt contact metal and the InGaP layer, samples with Pt/Ti/Pt/Au

Manuscript received September 5, 2006; revised November 7, 2006. This work was supported by the National Science Council, Taiwan, R.O.C., under Contract NSC 95-2752-E-009-001-PAE and Contract NSC 95-EC-17-A-05-S1-020. The review of this letter was arranged by Editor J. del Alamo.

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Digital Object Identifier 10.1109/LED.2006.889238

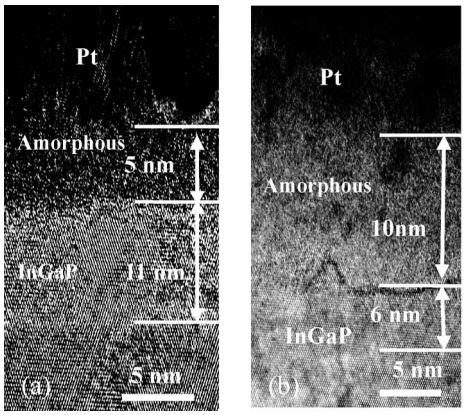

Fig. 1. (a) Cross-sectional TEM image of the as-deposited Pt/InGaP interface. (b) Cross-sectional TEM image of Pt/InGaP interface after 325 °C annealing for 1 min. The epilayers consist of, from bottom to top, GaAs buffer layer, AlGaAs/GaAs supper-lattice layers, 200-Å $Al_{0.24}Ga_{0.76}As$ layer, lower Si δ-doped layer, followed by undoped 30-Å $Al_{0.24}Ga_{0.76}As$ spacer, 150-Å $In_{0.2}Ga_{0.8}As$ channel, 20-Å $Al_{0.24}Ga_{0.76}As$ spacer, 20-Å undoped $In_{0.49}Ga_{0.51}P$, upper Si δ-doped layer, 160-Å undoped $In_{0.49}Ga_{0.51}P$ Schottky layer, and 750- Å heavily doped n^+ GaAs cap layer.

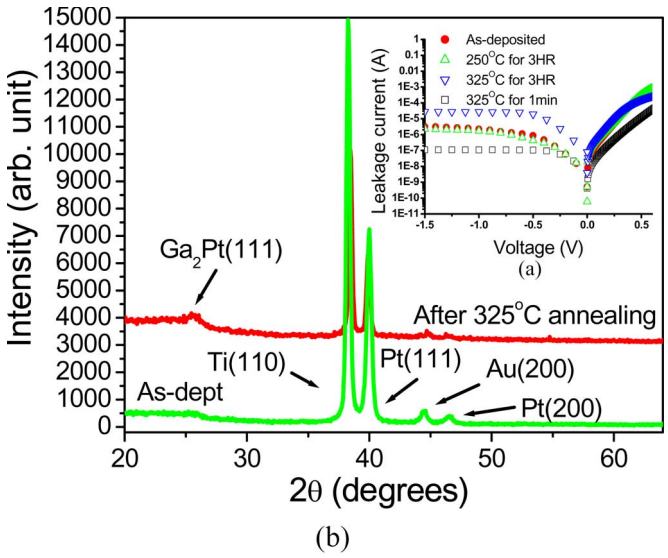

Fig. 2. (a) I–V characteristics of the diodes before and after annealing. (b) XRD spectra of the Pt/Ti/Pt/Au and InGaP/AlGaAs/InGaAs PHMET sample before and after annealing at 325 °C for 3 h. Main component: Ti, Pt, Au, Ga_2Pt (JCPDS PDF 44-1288, 04-0802, 04-0784, 03-1007).

metals deposited on the InGaP layer without SiN deposition were prepared for transmission electron microscopy (TEM) analysis and the energy dispersive X-ray analysis. The cross-sectional TEM image of the as-deposited sample, showing the Pt and InGaP interface, is shown in Fig. 1(a). About 5-nm-thick amorphous layer exists in the InGaP layers, and this amorphous layer was formed during the deposition of Pt. Earlier reports on Pt/GaAs system showed that amorphous layers were also found in the as-deposited Pt/GaAs interfaces [11], [12]. After annealing at 325 °C for 1 min, the amorphous layer which consists of Pt and InGaP mixture (the ratio of Pt is 51.83%) increased to 10 nm, i.e., the InGaP layer thickness decreased by 5 nm due to the amorphous layer thickness increase as shown in Fig 1(b).

Fig. 2(a) shows the current–voltage (I–V) characteristics of the diodes before and after annealing. The Schottky barrier

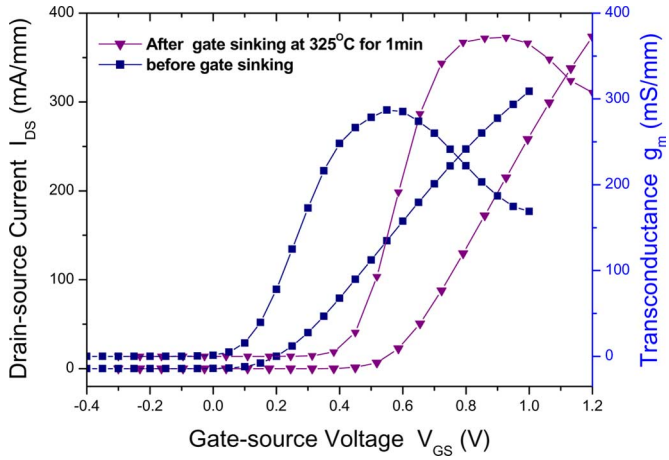

Fig. 3. Transconductance and the drain-source current versus V_{GS} curves of the 0.7 × 240-μm E-mode PHEMT at $V_{DS} = 2$ V with 20-nm thick-Pt before and after gate sinking at 325 °C for 1 min.

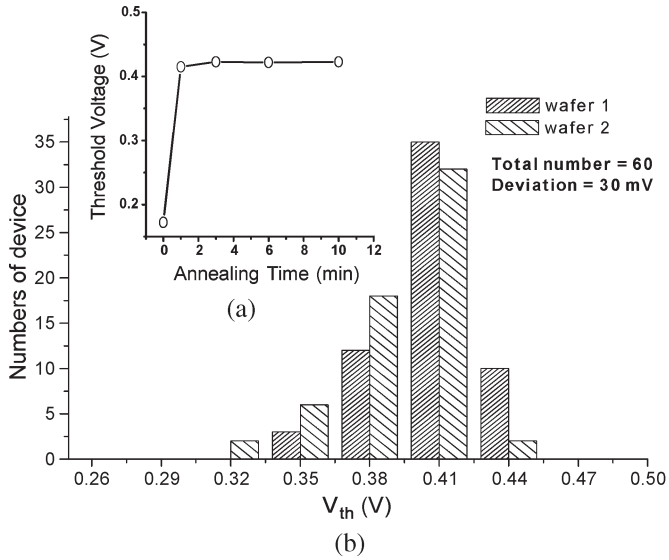

Fig. 4. (a) Threshold voltage of the Pt/Ti/Pt/Au E-mode PHEMT versus annealing time when annealed at 325 °C. (b) Distribution of V_{th} for the E-mode PHEMT across 4-in wafer for two different wafers.

height, which was evaluated by I–V measurement, increased from 0.78 to 0.84 eV, and the ideality factor changed from 1.09 to 1.12, after annealing. After 325 °C annealing for 3 h, new phase of $Ga_2Pt(111)$ formed as indicated by the X-ray diffraction (XRD) data in Fig. 2(b) and device performance degraded. This implies that after sufficient thick amorphous layer was formed at 325 °C, the thermal energy received from the annealing was used for the nucleation and the formation of the new crystalline phase. This process will limit further the interdiffusion of the Pt into the InGaP layer. In addition, the formation of the amorphous layer caused the gate capacitance increase due to the decrease of the gate-to-channel distance [13].

IV. DC Characteristics

Fig. 3 shows the transconductance and the drain-source current versus V_{GS} of the 0.7 × 240-μm E-mode PHEMT before

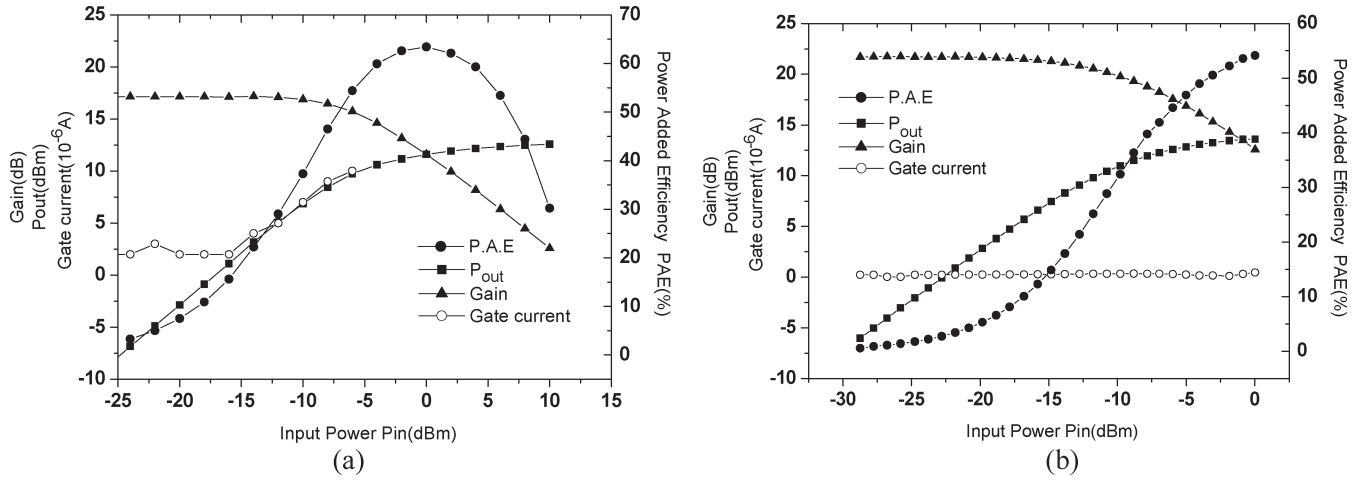

Fig. 5. (a) Power performance and gate leakage current of the 0.7 × 240-μm E-mode PHEMT before gate sinking. (b) Power performance and gate leakage current of the 0.7 × 240-μm E-mode PHEMT after gate sinking.

and after annealing at 325 °C for 1 min. The peak transconductance of the device measured before annealing was 287 mS/mm at $V_{\rm DS} = 2$ V and the $V_{\rm th}$ was 0.17 V. After annealing, the peak transconductance was increased to 373 mS/mm and $V_{\rm th}$ was increased to 0.41 V when $V_{\rm DS} = 2$ V. The threshold voltage is defined as $V_{\rm GS}$ when the $I_{\rm DS}$ reaches 1 mA/mm. After annealing, the gate leakage current slightly reduced from -1.3 to -0.79 μA/mm when biased at $V_{\rm DS} = 2$ V and $V_{\rm GS} = 0$ V. Therefore, the drain leakage current also decreased from 1.56 to 0.16 μA/mm when biased at $V_{\rm DS} = 2$ V and $V_{\rm GS} = 0$ V.

The threshold voltage can be obtained by solving Poisson's equation in one dimension [9]. After annealing, the measured Schottky barrier height and effective distance between the gate and the channel region changed. We believe that the threshold voltage increases related to the Schottky barrier height increase and the decrease in the distance between the gate and the channel layer. As a result, the device can be biased at higher forward gate voltage due to lower gate leakage current, and it has higher saturation current even though the current density is lower at the same gate bias point as compared to the devices without gate sinking.

The threshold voltage $(V_{\rm th})$ versus annealing temperature is shown in Fig. 4(a). The threshold voltage stabilized after 1-min annealing and remained almost the same after 325 °C annealing for 10 min. The threshold voltage of the HEMT device was very uniform after the gate-sinking process, and it demonstrated good reproducibility as shown in Fig. 4(b). The $V_{\rm th}$ of the devices has a small standard deviation of 30 mV across the 4-in wafer. For the two wafers under study, the range of the standard deviation of $V_{\rm th}$ remained almost the same.

V. RF Performance

The S parameters of the E-mode PHEMTs were measured by on-wafer testing from 1 to 40 GHz. The calculated best f_T and $f_{\rm max}$ of the before and after annealed E-mode PHEMT were measured. Before annealing, the calculated f_T and $f_{\rm max}$ were 18 and 29 GHz, respectively, when device was biased at $V_{\rm GS} =$ 0.6 V and $V_{\rm DS} = 2$ V. After annealing, the calculated f_T and $f_{\rm max}$ were 21 and 38 GHz, respectively, when device was biased at $V_{\rm GS} = 0.8$ V and $V_{\rm DS} = 2$ V. The RF performance improvement after gate sinking was due to the transconductance increase which was caused by the Pt sinking into the InGaP layer after annealing.

The power performances of the 0.7 × 240-μm^2 device were measured at 2 GHz and tuned for maximum PAE match. Fig. 5 shows the RF performance before and after annealing. From Fig. 5(a), it is clearly observed that for the device before annealing, the gate current increased drastically with RF input level, which in turn could imply worse RF reliability under highly driven operation for such devices. Fig. 5(b) shows the power performance after annealing; the $P_{\rm out}$ was 13.59 dBm (95.23 mW/mm) with 54% PAE and 21.77-dB linear gain, when biased at $V_{\rm DS} = 2$ V, $I_{\rm DS} = 20$ mA. In contrast to the device before annealing, the gate current was quite low and remained almost constant over the whole input power range up to 10-dB compression, implying a much better RF reliability performance.

VI. Conclusion

The use of the Pt buried gate technology on the fabrication of the InGaP/AlGaAs/InGaAs E-mode PHEMT was realized successfully. The fabricated E-mode PHEMT device with gate sinking showed excellent RF performance, good threshold voltage uniformity, and reduced gate and drain leakage currents. The use of the gate-sinking technology is believed to be very useful for the E-mode InGaP/AlGaAs/InGaAs PHEMTs fabrication.

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