Fabrication of 0.15-μm Γ-Shaped Gate $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ Metamorphic HEMTs Using DUV Lithography and Tilt Dry-Etching Technique

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***Abstract*—An $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ metamorphic high-electron mobility transistor (MHEMT) with 0.15-μm Γ-shaped gate using deep ultraviolet lithography and tilt dry-etching technique is demonstrated. The developed submicrometer gate technology is simple and of low cost as compared to the conventional E-beam lithography or other hybrid techniques. The gate length is controllable by adjusting the tilt angle during the dry-etching process. The fabricated 0.15-μm $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ MHEMT using this novel technique shows a saturated drain–source current of 680 mA/mm and a transconductance of 728 mS/mm. The f_T and f_{max} of the MHEMT are 130 and 180 GHz, respectively. The developed technique is a promising low-cost alternative to the conventional submicrometer E-beam gate technology used for the fabrication for GaAs MHEMTs and monolithic microwave integrated circuits.**

***Index Terms*—Deep ultraviolet (DUV) lithography, metamorphic high-electron mobility transistors (MHEMTs), tilt dry-etching technique, Γ-shaped gate.**

I. Introduction

FOR HIGH-SPEED wireless communications, metamorphic high-electron mobility transistors (MHEMTs) have received much attention recently due to its capability of combining the advantages of a high-performance InP-based structure and a low-cost high-mechanical-strength GaAs substrate. MHEMTs with excellent high-frequency performance comparable to the InP-based HEMTs have also been demonstrated [1], [2]. MHEMTs have been considered as a cost-effective alternative to the conventional lattice-matched or pseudomorphic InAlAs/InGaAs/InP HEMTs (InP-HEMTs). The gain and noise characteristics of the MHEMTs at high frequencies are strongly dependent on gate length L_g and the gate resistance; therefore, T- or Γ-shaped gates with small footprint and wide tee-top are commonly used for HEMTs to maximize the device performance. A wide variety of lithography methods have been used for the fabrication of submicrometer gates with T, Γ, or Y shapes to improve device performance [3]–[5]. Fabrications of submicrometer gates using angle and angled-shadow evaporation processes have been reported [6], [7]. A multilayer deep ultraviolet (DUV) photoresist process has been used to obtain 0.2-μm T-shaped gates [8]. A hybrid method using E-beam lithography and reflowed-resist technology to shrink the gate length down to 0.1 μm was also demonstrated [9]. I-line lithography combined with a chemical shrinking process has shown the capability of fabricating 0.1-μm-gate InP HEMTs [10]. However, tightly controlled process conditions, complicated process steps, or expensive E-beam lithography tools are required for these processes.

For cost-effective production of submicrometer MHEMTs, a 0.15-μm Γ-shaped-gate MHEMT technology using DUV lithography and a tilt dry-etching technique was developed and demonstrated for the first time. The final gate length of the Γ gate was mainly controlled by the top photoresist opening, the total resist thickness, and the tilt angle for the anisotropic dry etching. Comparing with the previously reported gate fabrication techniques, the tilt dry-etching gate process is a relatively simple, inexpensive, and flexible process for the fabrication of submicrometer GaAs MHEMTs and monolithic microwave integrated circuits (MMICs) for high-frequency applications.

II. Experiment

The MHEMT structure was grown on a (100) GaAs substrate by molecular beam epitaxy. The structure is given as follows: A 15-nm $In_{0.6}Ga_{0.4}As$ channel layer was grown on top of the InAlAs buffer layer. The top and bottom Si-δ-doping layers were separated from the channel layer by the upper and lower i-InAlAs spacers, respectively. The Schottky layer was a 15-nm-thick i-$In_{0.52}Al_{0.48}As$. The 15-nm-thick n-$In_{0.52}Ga_{0.48}As$ cap (2×10^{18} cm^{-3}) layer was finally grown on the top. For the device fabrication, the mesa was done by wet etch, and the ohmic contacts were formed by evaporating Au/Ge/Ni/Au on the n-InGaAs cap layer and then alloyed at 300 °C to achieve a low contact resistance of 0.05 Ωmm. The process for fabricating the Γ gate is illustrated in Fig. 1. The bilayer resists consisting of the bottom 150-nm polymethyl

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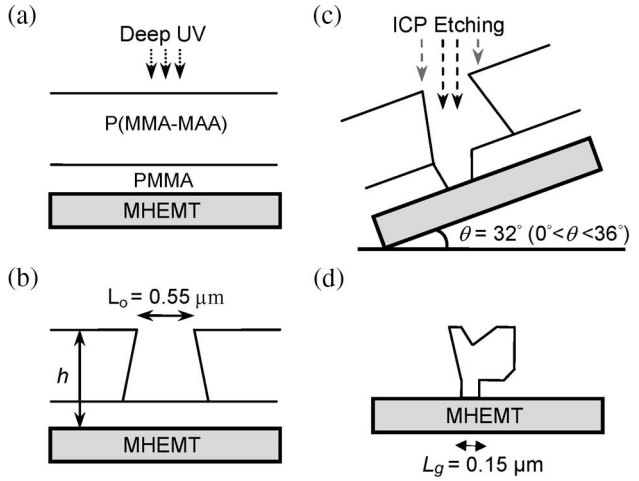

Fig. 1. DUV lithography and tilt dry-etching process steps for fabricating the submicrometer Γ-gate MHEMT. (a) DUV exposure. (b) Selective development of the top layer. (c) Tilt dry etching of the bottom layer. (d) Γ-gate profile after gate metal lift-off.

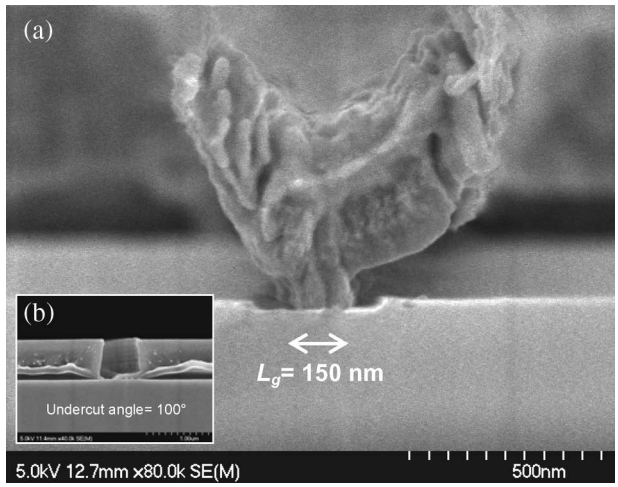

Fig. 2. Cross-sectional SEM images of a (a) 0.15-μm Ti/Pt/Au Γ gate and (b) resist profile after the tilt dry-etching process.

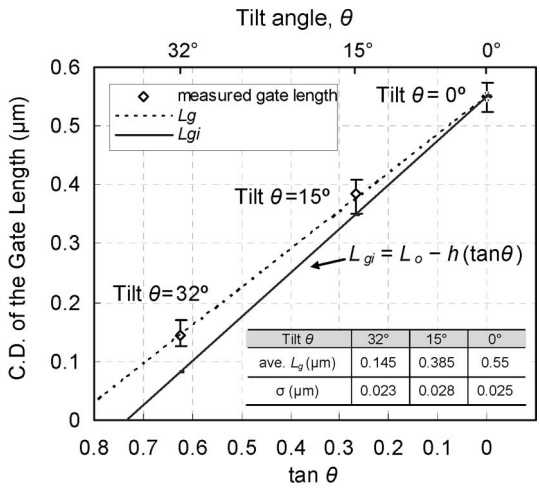

Fig. 3. CD of the measured gate length L_g and the ideal gate length $L_{\rm gi}$ as a function of the tangent of tilt angle θ.

methacrylate (PMMA) and the top 600-nm PMMA-methacrylic acid [P(MMA-MAA)] were coated sequentially. In Fig. 1(a), the opening of 0.55 μm on the top layer was defined by DUV$(\lambda = 254$ nm$)$ exposure for 3 min using a contact aligner with a high-intensity light source. The exposure dose $(1600$ mJ/cm$^2)$ was carefully adjusted so that only the P(MMA-MAA) resist layer was opened. The selective development was realized easily due to the high sensitivity ratio of P(MMA-MAA) to PMMA ($\sim$5 : 1). In Fig. 1(b), the undercut profile of the P(MMA-MAA) trench was due to the surface rate retardation during development. After the development, the wafer was tilted at an angle and was etched using inductive coupled plasma (ICP) ion etching with SF_6/Ar etching gases. A low RF power of 50 W was applied to both the ICP source and the chuck to minimize the etch-induced damage for the underlying InGaAs layer. A set of tilt angles θ, i.e., 0°, 15°, and 32°, was chosen to obtain the desired feature size in the bottom PMMA layer [Fig. 1(c)]. The optimum gas ratio $SF_6 : Ar = 1 : 1$ was used to achieve highly anisotropic etching, and the etch rate of PMMA was 160 nm/min. After the tilt dry-etching process, gate recess was performed using a succinic acid$/H_2O_2/NH_4OH$ solution, and then, a Ti/Pt/Au gate metal was deposited. A lift-off process was performed after the gate metal deposition to form the 0.15-μm Γ gate [Fig. 1(d)]. The cross-sectional scanning electron microscopy (SEM) images of the 0.15-μm Γ gate and the resist profile just after the 32° tilt dry-etching process are shown in Fig. 2(a) and (b), respectively.

III. Result and Discussion

Fig. 3 shows the critical dimension (CD) of the measured gate length L_g as a function of the tangent of the tilt angle during the dry-etching process. The statistic data of the average gate length L_g and the standard deviation σ were estimated by using SEM observation. The data are shown in the inset table in Fig. 3. In this figure, the measured gate length L_g was decreased by increasing the dry-etching angle θ. A line of the predicted ideal gate length $(L_{\rm gi} = L_o - h \times \tan\theta)$ was also plotted in the same figure for comparison. L_o (0.55 μm) is the initial opening of the top P(MMA-MAA) layer, and the total resist thickness h is 0.75 μm, as indicated in Fig. 1(b). There is a difference (ΔL) between the $L_{\rm gi}$ and the L_g. ΔL increased with increasing tilt angle, which is due to the etching of the sidewall of the resist trench when the tilt angle is applied. ΔL is about 0.06 μm when θ is 32°. The maximum allowed tilt angle is about $\tan^{-1}(L_o/h) = 36°$. When θ was increased to 32°, a gate length L_g of 0.15 μm was achieved. This condition was applied for the MHEMT fabrication in this letter. In addition, the InGaAs cap layer exposed to the plasma was removed by the wet gate recess after the tilt dry etching. Therefore, the etch-induced damages had little influence on the device performance. This can be clearly seen from the electrical measurement data.

The drain–source current $I_{\rm ds}$ versus drain–source voltage $V_{\rm ds}$ curves and the transconductance g_m versus gate–source voltage $V_{\rm gs}$ curves of the 0.15-μm Γ-gate MHEMT are shown in Fig. 4(a) and (b), respectively. The 2 × 50-μm-wide device

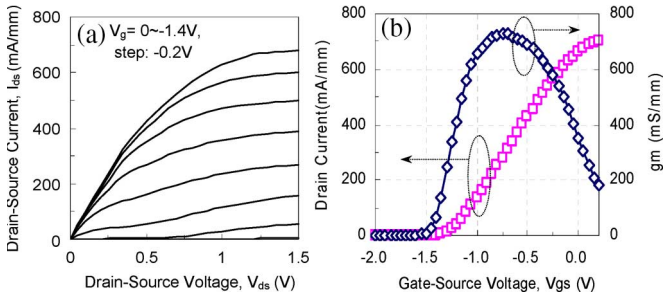

Fig. 4. (a) Drain–source current versus drain–source voltage curves and (b) transconductance versus gate–source voltage of the 0.15-μm Γ-gate MHEMT.

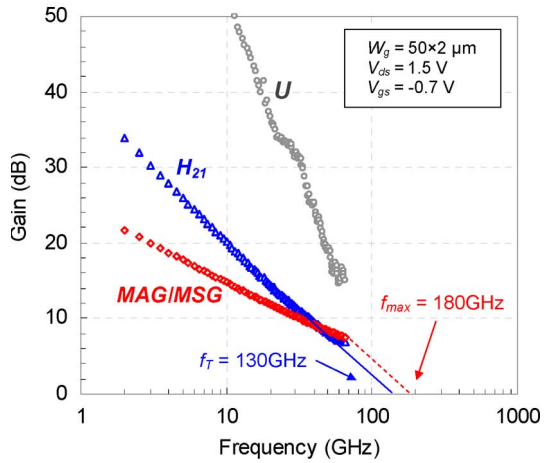

Fig. 5. Frequency dependence of the current gain H_{21}, the power gain MAG/MSG, and the unilateral gain U of the 0.15-μm Γ-gate MHEMT. The frequency range was from 2 to 65 GHz, and the device was biased at $V_{\rm ds} = 1.5$ V and $V_{\rm gs} = -0.7$ V.

exhibited good pinchoff characteristics, and the saturation $I_{\rm ds}$ was 680 mA/mm. The maximum g_m of the device at a $V_{\rm ds}$ of 1.5 V was 728 mS/mm, and the pinchoff voltage was −1.3 V. The gate–drain breakdown voltage $V_{\rm BR}$ of the MHEMT was 7.5 V (defined at a gate–drain current of 1 mA/mm), which is the same as that of the device manufactured with a conventional E-beam T-gate. Based on the gate breakdown characteristics of the device, the etch-induced damages were minimized in this letter.

The S-parameters for the MHEMT were measured from 2 to 65 GHz using on-wafer 100-μm-pitch ground–signal–ground probes. The gate resistance R_g of the device using the tilt dry-etching process extracted from an S-parameter was 8.27 Ω. Fig. 5 shows the frequency dependence of the current gain H_{21}, the power gain "MAG/MSG," and the unilateral gain U of the MHEMT measured at $V_{\rm ds} = 1.5$ V and $V_{\rm gs} = -0.7$ V. The current gain cut-off frequency f_T and the maximum oscillation frequency $f_{\rm max}$ obtained for the 2×50 μm MHEMT were 130 and 180 GHz, respectively. The f_T of the 0.15-μm Γ-gate MHEMT in this letter is comparable to that of the devices reported by other groups with the same gate length [11], [12] and that of the device fabricated by E-beam lithography in our previous work [9]. The excellent dc and RF performances of the devices demonstrate that the developed tilt dry-etching gate technology is a promising alternative to the conventional gate fabrication technology using E-beam direct writing or hybrid techniques.

IV. Conclusion

A 0.15-μm Γ-gate $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As$ MHEMT fabricated on GaAs substrate using DUV lithography and a tilt dry-etching technique is demonstrated for the first time in this letter. The developed technology is simple, of low cost, and flexible for the submicrometer Γ-gate fabrication. The 100-μm-wide MHEMT with 0.15-μm Γ gate fabricated with a dry-etching tilt angle of 32° shows a saturation $I_{\rm ds}$ of 680 mA/mm and a g_m of 728 S/mm. The MHEMT also exhibits an f_T of 130 GHz and an $f_{\rm max}$ of up to 180 GHz. The excellent device performance shows that the developed 0.15-μm Γ-gate technology can practically be used for high-performance MHEMT devices and MMIC manufacturing.

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