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Characteristics of low-temperature pulse-laser-deposited (Pb,Sr)TiO_3 films in metal/ferroelectric/silicon structure

Jyh-Liang Wang[1], Yi-Sheng Lai[2], Trent Gwo-Yann Lee[1], Bi-Shiou Chiou[1], Chun-Chien Tsai[1], Huai-Yuan Tseng[1], Chueh-Kuei Jan[1] and Huang-Chung Cheng[1]

[1] Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 30010, Taiwan, Republic of China
[2] Department of Materials Science and Engineering, National United University, Miaoli 36003, Taiwan, Republic of China

E-mail: joewang666@gmail.com

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Abstract
In this study, pulsed-laser deposited (Pb,Sr)TiO_3 (PSrT) films on p-type Si were studied at low substrate temperatures ranging from 300 to 450 °C for metal/ferroelectric/semiconductor applications. The substrate temperature strongly enhances film crystallinity without significant inter-diffusion at the PSrT/Si interface and affects the electrical properties. As the substrate temperature increases, the films have smaller leakage currents, fewer trap states at the electrode interfaces, clockwise capacitance versus applied field hysteresis loops and larger memory windows correlated with superior crystallinity. Conversely, 300 °C-deposited films exhibit a small and counterclockwise loop with a positive shift of the flatband voltage, attributed to more negative trap charges within the films. However, the high substrate temperature (450 °C) may produce serious Pb–O volatilization, incurring more defects and leakage degradation. The analyses of fixed charge density and flatband voltage shift reveal the trap status and agree well with the leakage characteristic. An electron band model of the Pt/PSrT/Si electronic structure is proposed to explain the electrical behaviour. The excellent fatigue endurance with a small variation of memory windows (<11%) after 10^{10} switching is also demonstrated.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Ferroelectric based gate insulator field-effect transistors (FETs) have been investigated as future non-destructive read-out (NDRO) non-volatile memory devices [1–8]. Among several kinds of ferroelectric gate FET structures, a metal/ferroelectric/semiconductor (MFS) configuration is particularly promising due to the advantages of simple fabrication processes, low power consumption (without the voltage drop across the buffer insulator) and small memory cell size compared with its alternatives. MFS-FET exploits the ferroelectric field effect, which is the modulation of conductivity by the electrostatic charges induced by ferroelectric polarization, and thus requires the direct deposition of ferroelectric thin films on silicon (Si) wafer. Thin films of various ferroelectric materials, such as Pb(Zr,Ti)O_3 (PZT), $YMnO_3$ (YMO), $SrBi_2Ta_2O_9$ (SBT), $Bi_4Ti_3O_{12}$ (BIT) and $CaBi_2Nb_2O_9$ (CBN), have been investigated for MFS-FET devices [2–8]. These materials are usually processed at high temperatures (>600 °C) to obtain the good crystallinity of a perovskite structure [2–7]. However, the high-temperature process will cause the diffusion of constituent elements and/or the chemical reactions between the ferroelectric film and the underlying silicon [9–11], which

produces undesirably high density of interfacial trap states [3–8]. In addition, the volatilization of Pb–O in lead-titanate-based films and the loss of Bi content in bismuth-titanate-based films, processing at high temperatures, always degrade the microstructure and the reliability of ferroelectric devices [11–13]. Hence, a relatively low-temperature process is indeed required for the deposition of ferroelectric thin films for MFS-FET applications.

(Pb,Sr)TiO_3 (PSrT) is feasible for memory applications due to its large electric-field-dependent dielectric constant and composition-dependent Curie temperature [14–16]. The (Pb,Sr)TiO_3 (PSrT) solid-solution film is constituted by $PbTiO_3$ and $SrTiO_3$. The effect of lead (Pb) substituted by strontium (Sr) in the $PbTiO_3$ film will decrease the crystallization temperature and offers a good control of dielectric properties at room temperature [14, 15]. To deposit PSrT films, the pulsed-laser deposition (PLD) technique is applied, which is feasible for fabricating films with complex compounds and capable of growing a wide variety of stoichiometric oxide films without subsequent high-temperature annealing. Hence, PLD is a potential technique, which could be integrated into low-temperature semiconductor processing. To date, much less is known about the properties of PLD PSrT films deposited on Si substrates. In our work, the low-temperature PLD process can avoid these problems as stated and make several improvements in film properties. Thus, a high-quality MFS structure without a buffer layer between PSrT films and Si substrates has been developed.

2. Experimental

Si (1 0 0) has the lowest surface state density, which is superior to Si (1 1 0) and Si (1 1 1). In order to reduce the effect of surface states, (1 0 0) orientation p-type Si wafers were employed as the substrates in this study. After the initial RCA cleaning process, thin PSrT films (200 nm thick) were then deposited on p-type Si substrates by a PLD system (Lambda Physik LPX 200i) utilizing KrF excimer laser ($\lambda = 248$ nm) radiation. A set of optical lens was used to focus the laser beam over the $(Pb_{0.6}Sr_{0.4})TiO_3$ target in vacuum. The vacuum chamber was pumped down to a base pressure of 0.1 mTorr and then refilled with O_2 as a reactive gas. The vaporized species of the target were transferred and deposited on the substrate heated by a thermal heater. The deposition temperature (substrate temperature, T_s) was used as a variable from 300 to 450 °C, calibrated at the wafer upper surface. The target-to-substrate distance was 4 cm. During the PLD process, the oxygen ambient pressure was 80 mTorr. The laser pulsed rate and the average energy fluence were 5 Hz and 1.55 J cm^{-2} per pulse, respectively.

An Auger electron spectroscope (AES) (Auger 670 PHI Xi, Physical Electronics) was used to analyse the elemental depth profile of the PSrT films. The crystallinity of the films was analysed by an x-ray diffractometer (D5000, Siemens). The optical properties of the refraction index (n) and extinction coefficient (κ) were investigated using an n&k Technology 1280 analyser. The n and κ are influenced by the electronic structure and/or the crystallinity of the film. After the physical examination, patterned platinum (Pt) top electrodes, with a thickness of 100 nm and a diameter of 75 μm, were deposited by a sputtering process to form a Pt/PSrT/Si (MFS) capacitor structure. The noble metal platinum, with low resistivity, is considered as the electrode of Pt/PSrT/Si capacitor because of its small leakage current, low power consumption, small RC delay and good thermal stability to lead-based perovskite materials [11]. Then, the native oxide on the backside of the Si wafer was removed by HF etching. An aluminium (Al) film (500 nm thick) was sequentially deposited on the wafer backside to form a Si/Al bottom electrode. The combination of a semiconductor parameter analyser (4156C, Agilent Technologies) and a probe station was used to measure the leakage current (I–V characteristics). A capacitance–voltage (C–V) analyser (Package 82 system C–V 590, Keithley) was also used to measure C–V curves at 100 kHz. A pulse generator (8110A, Hewlett Packard) and a pulse/function generator (8116A, Hewlett Packard) were connected together with low noise BNC cables to generate a +3 V/-3 V bipolar wave pulsed at 1 MHz, confirmed by an oscilloscope (54645A, Hewlett Packard), as an input signal for the measurement of polarization switching degradation (fatigue).

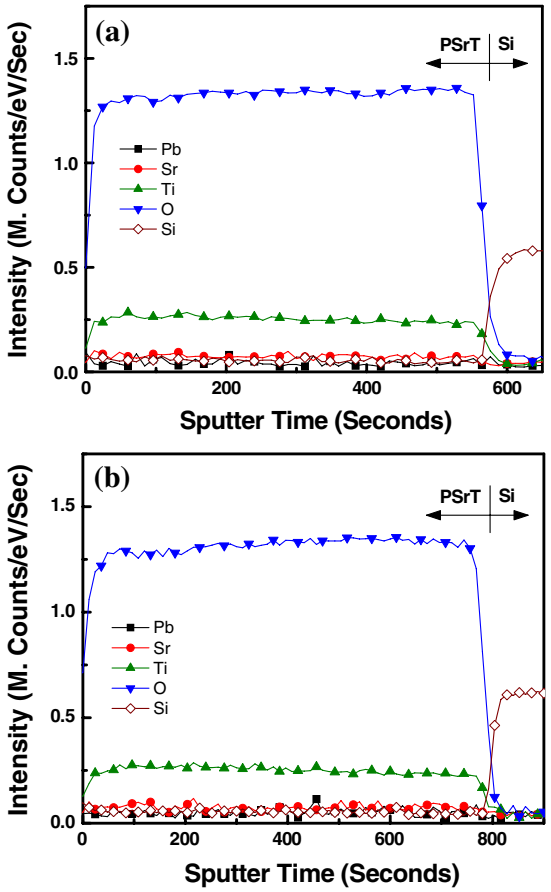

Figure 1. AES depth profiles of PLD PSrT films deposited on Si (1 0 0) wafers at (*a*) 300 °C and (*b*) 450 °C.

3. Results and discussion

Figure 1 reveals the AES depth profiles of the PLD PSrT films deposited on Si (1 0 0). Without standard samples to calibrate the sensitivity factor, the count intensity of elements

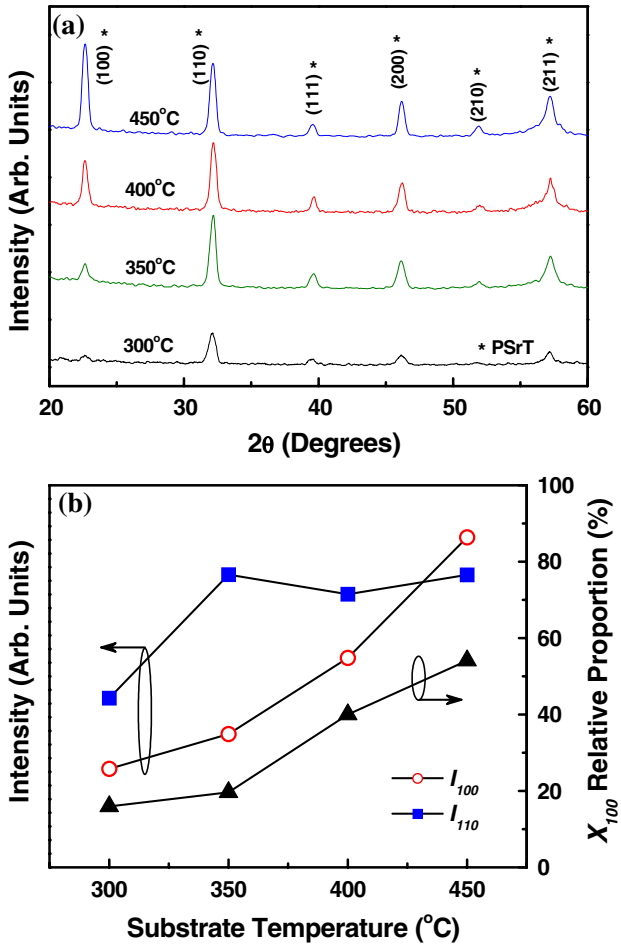

Figure 2. (*a*) X-ray diffraction patterns and (*b*) texture characteristics of PLD PSrT films deposited on Si at various substrate temperatures.

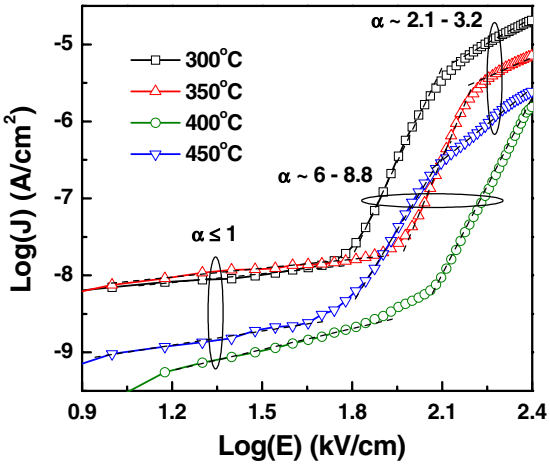

Figure 3. Current density versus applied field (log (J)–log (E)) curves of Pt/PSrT/Si capacitors prepared at various substrate temperatures. The corresponding slopes in different regions are denoted as α.

presented here can only be semi-quantitative, but not absolute. No evident difference is observed between the depth profiles of the films deposited at 300 and 450 °C. As can be seen from the abrupt interface profile, no significant inter-diffusion of oxygen, titanium and silicon between the PSrT films and the Si substrate occurs at such low temperatures. Figure 2(*a*) presents the x-ray diffraction patterns of the PSrT films deposited at various T_s. All the diffraction peaks of these data are indexed as (1 0 0), (1 1 0), (1 1 1), (2 0 0), (2 1 0) and (2 1 1) planes of $(Pb_{1-x}Sr_x)TiO_3$ perovskite phases [14–17]. The crystalline PSrT films appear at such low temperatures because (i) the addition of strontium makes the crystallization temperature of PSrT lower than that of PZT [14], and (ii) the PLD technique could preserve the crystalline phases and the stoichiometric composition of the target material at low T_s [15]. Moreover, the intensities of the (1 0 0), (1 1 1), (2 0 0), (2 1 0) and (2 1 1) orientations increase significantly with the increasing T_s. Figure 2(*b*) quantizes the XRD spectral analysis, using the following formula:

$$X_{100} = I_{100}/(I_{100} + I_{110}), \tag{1}$$

where X_{100} is the relative proportion of the (1 0 0) orientation, I_{100} is the integrated area under the (1 0 0)-oriented peak, and I_{110} is the integrated area under the (1 1 0)-oriented peak.

The X_{100} increases as T_s increases and shows the maximum at $T_s = 450$ °C, indicative of a strong (1 0 0) preferred orientation. It infers that the intensity of the (1 0 0)-oriented peak of the PSrT films is strongly enhanced by using the Si (1 0 0) substrate as opposed to that on $Pt/SiO_2/Si$ (not shown here).

The Pt/PSrT/Si capacitor with an aluminium backside electrode is used as a MFS configuration for electrical measurements. These MFS devices require the ferroelectric film to be deposited on the silicon surface directly, and utilize their remnant polarization to control the surface potential of silicon. Thus the interfacial states and the leakage current are very important for normal FET operations. Figure 3 displays the curves of current density versus applied field (J–E) and an extraction of the slope, α, in different regions of log(J)–log(E) plots, which gives an idea of the conduction process involved under the influence of varying electrical fields. Initially, the leakage current shows an ohmic behaviour at low fields ($\alpha \leqslant 1$). At slightly higher electrical fields ($\alpha \sim$ 6–8.8), it shows an onset of the linear region, attributed to the space charge limited conduction (SCLC) mechanism [6, 7]. The inhibited leakage current observed in PSrT films deposited at 300–400 °C is correlated with fewer structural defects because of the enhanced crystallinity as shown in figure 2. Comparing the data at $T_s = 400$ °C and $T_s = 450$ °C, the increasing current density may correspond to more chemical defects due to the more serious volatilization of Pb–O of the PSrT films at a higher temperature ($\geqslant$ 450 °C) [11, 12]. Figure 4 reveals the experimental and fitted log(J/T^2) versus $E^{1/2}$ (Schottky emission) plots of Pt/PSrT/Si capacitors applied at a positive/negative bias. If the leakage current follows the Schottky emission behaviour, a log(J/T^2) against $E^{1/2}$ plot should be linear and the dashed lines work as the fitted results. It is noted that figures 4(*a*) and (*b*) reveal a similar tendency. The decreasing values of log(J/T^2) against $E^{1/2}$ present the inhibited interfacial trap states as T_s increases from 300 to 400 °C. As T_s increases to 450 °C, however, the increasing values of log(J/T^2) against $E^{1/2}$ indicate more trap states at both the electrode interfaces. A strong polarity dependence of the leakage current is noted due to the different materials used for the top (Pt) and bottom (Si) electrodes as shown in

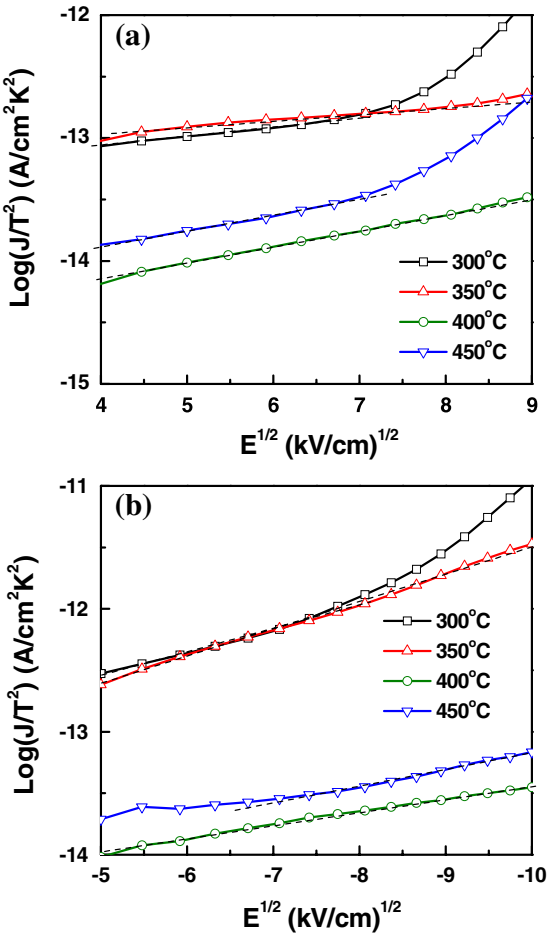

Figure 4. Experimental and fitted $\log(J/T^2)$ versus $E^{1/2}$ (Schottky emission) plots of Pt/PSrT/Si capacitors at (*a*) positive bias and (*b*) negative bias.

figures 4(*a*) and (*b*) [8]. The polarity dependence is connected with the different Schottky barrier heights (φ_{b1} and φ_{b2}) at the Pt/PSrT and PSrT/Si interfaces, expressed as the following relations [18, 19]:

$$\varphi_{b1} = \varphi_m - q\chi_f, \tag{2}$$

$$\varphi_{b2} = \varphi_{Si} - q\chi_f = \chi_{Si} + \frac{1}{2}E_{Sig} + kT\ln(N_a/n_i) - q\chi_f, \tag{3}$$

where φ_m is the work function of the Pt electrode (φ_m = 5.3 eV), χ_f is the electron affinity of the PSrT films, φ_{Si} is the work function of the Si substrate, χ_{Si} is the electron affinity of Si (χ_{Si} = 4.05 eV), q is the unit charge, E_{Sig} is the energy gap of Si (E_{Sig} = 1.12 eV), k is the Boltzmann's constant, T is the absolute temperature, n_i is the intrinsic carrier concentration of Si, and the doping concentration (N_a) is about 2×10^{15} cm^{-3}, according to the p-type Si resistivity of 5–10 Ω cm [18–20]. The values of the electron affinity of PZT, BST and $SrTiO_3$ are reported as χ_{PZT} = 3.5 eV, χ_{BST} = 4.0 eV and χ_{STO} = 4.1 eV, accordingly [20, 21]. Thus, the electron affinity of PSrT, χ_f, may be roughly assumed as 3.8 eV. Hence, the Schottky barrier heights could be calculated as φ_{b1} = 1.3 eV and φ_{b2} = 0.8 eV. In addition, the more interfacial trap states result in more charge accumulation and a severe image-force effect at the edge of the

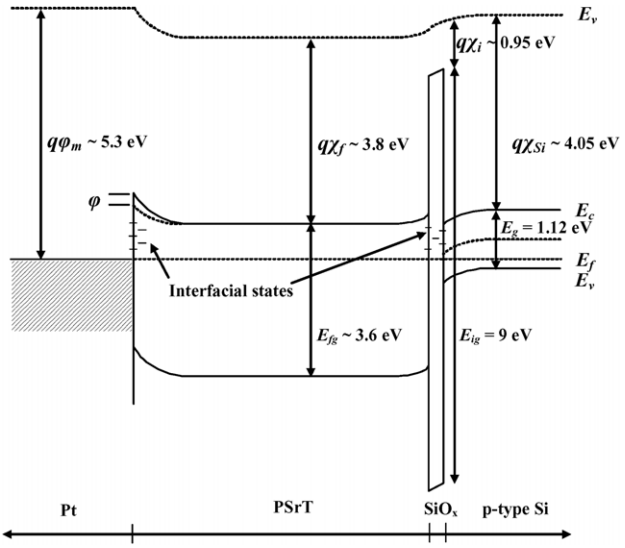

Figure 5. Schematic drawing of the electron energy band for the Pt/PSrT/Si structure.

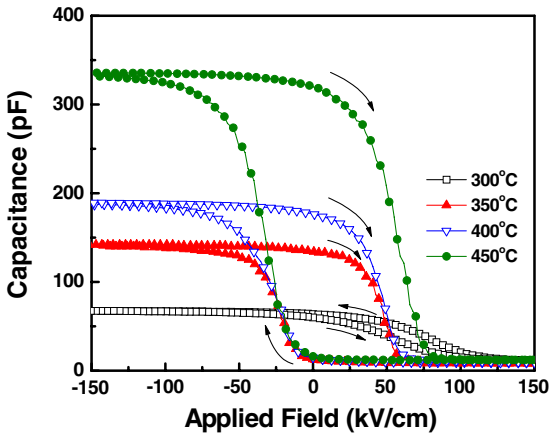

Figure 6. Capacitance-applied field (C–E) hysteresis loops of Pt/PSrT/Si capacitors prepared at various substrate temperatures.

electrodes, leading to the decrease in Schottky barrier height. The image-force lowering ($\Delta\phi$) can be expressed as [22, 23]

$$\Delta\varphi = (N_c q E/4\pi\varepsilon_s\varepsilon_0)^{1/2}, \tag{4}$$

where N_c is the charge amount and ε_s is the static dielectric constant of the ferroelectric material. Figure 5 illustrates the schematic drawing of the electron energy band for Pt/PSrT/Si. In general, the electron energy band at the interfaces of the electrodes reveal that the PSrT films act as n-type semiconductors due to the generation of oxygen vacancies in ABO_3 perovskites [22–24]. The band gap of the PSrT films, E_{fg}, is measured as 3.52–3.66 eV by optical investigation of the refraction index (n) and the extinction coefficient (κ). The values of E_{fg} are approximately close to the reported value of 3.6 eV for $PbTiO_3$ [21].

Figure 6 displays the capacitance versus applied field (C–E) hysteresis loops of Pt/PSrT/Si capacitors deposited at various T_s, sweeping at 0.05 V/100 ms from a negative bias to a positive bias and reversing it again. The capacitance of the hysteresis loops presents the series properties of the capacitor

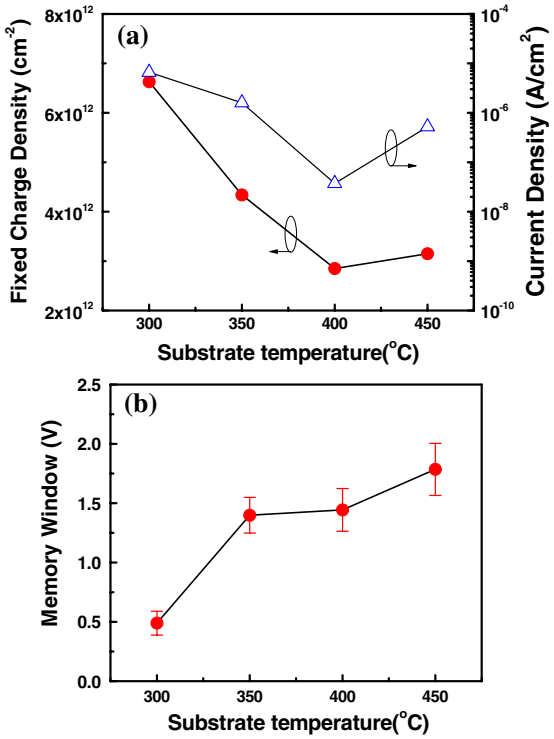

Figure 7. (*a*) Fixed charge density (N_{fc}) and leakage current density (at +150 kV cm^{-1}) as a function of substrate temperatures for Pt/PSrT/Si structures. (*b*) Memory window (V_m) of Pt/PSrT/Si capacitors prepared at various T_s.

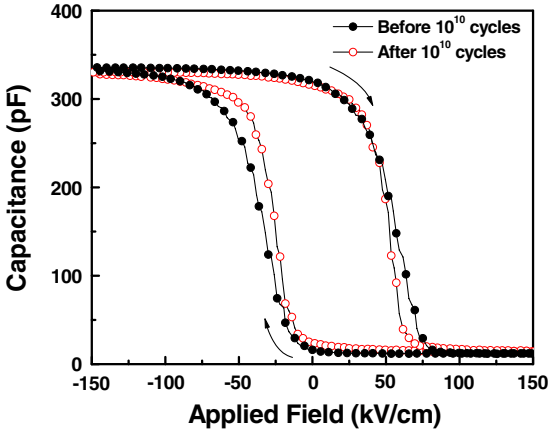

Figure 8. *C*–*E* hysteresis loops of Pt/PSrT/Si capacitors prepared at 450 °C before/after 10^{10} fatigued switching cycles.

of the Si depletion region and the capacitor of the ferroelectric films (C_{PSrT}). It is seen that the C_{PSrT} and the width of the hysteresis loops increase as T_s increases, which could be ascribed to the enhanced crystallinity of the film (figure 2). In addition, films deposited at higher T_s ($\geqslant$ 350 °C) show the clockwise hysteresis loops, whereas those deposited at 300 °C reveal the counterclockwise loop. The clockwise hysteresis means that ferroelectric dipole switching governs the surface potential of p-type Si, which is the desired switching mode for the operation in MFS-FET devices [6, 8, 25]. In contrast, the counterclockwise loop could be attributed to the numerous border trap states induced by the poor-quality interfacial native oxide (SiO_x) between the ferroelectric film and Si, since SiO_x can be found anywhere in the MFS capacitors [3, 4, 6, 25]. Moreover, 300 °C-deposited films indicates a positive voltage shift of *C*–*E* loops compared with those deposited at higher T_s ($\geqslant$ 350 °C). The negative charge causes the shift toward positive voltage and dominates the electrical properties of the PSrT/Si interface. Furthermore, the fixed charge density (N_{fc}) could be estimated from the *C*–*E* loops by the following formula [6, 7]:

$$N_{fc} = C_{PSrT}(V_{fb} - \varphi_{ms})/(qA), \tag{5}$$

where V_{fb} is the flatband voltage, φ_{ms} is the effect function remainder between the metal (Pt) electrode and the semiconductor (Si) substrate and A is the electrode area. Figure 7 (*a*) points out the minimum N_{fc} of $\sim 2.85 \times 10^{12}$ cm^{-2} for films deposited at 400 °C. It is found that the trend of N_{fc} is consistent with that of the leakage current density biased at +150 kV cm^{-1} (evaluated from figure 3), where the conduction is dominated by the SCLC mechanism. Figure 7 (*b*) presents the memory windows (V_m), extracted from figure 5, of Pt/PSrT/Si capacitors prepared at various T_s. The value of V_m increases as T_s increases and shows the maximum of 1.785 V for 450 °C-deposited films, which is associated with the larger C_{PSrT} and the enhanced crystallinity. The V_m can be linked to twice the coercive voltage ($2V_c$) and severely narrows down by the charge injection into the border traps of SiO_x located at the PSrT/Si interface, which can be described as [3, 4]

$$V_m = 2V_c + V_{ci}, \tag{6}$$

where V_{ci} is the flatband voltage shift due to charge injection. Here, the $2V_c$ are 2.06 V, 1.7 V, 1.8 V and 2.4 V, respectively, which could be referred to the polarization versus electric field (*P*–*E*) curves of Pt/PSrT/Pt capacitors prepared at T_s = 300–450 °C (not shown in this work). From equation (6), the V_{ci} shows the minimum value of ~ -1.57 V for films deposited at 300 °C and the maximum value of ~ -0.3 V for films deposited at 350–400 °C. In addition, the V_{ci} changes slightly to -0.61 V as T_s increases from 400 to 450 °C. Consequently, the evolution of V_{ci} agrees well with the N_{fc}, the shift of the *C*–*E* loop and leakage currents as mentioned above.

Figure 8 demonstrates the fatigue properties of *C*–*E* hysteresis loops for Pt/PSrT/Si capacitors prepared at 450 °C before/after 10^{10} switching cycles. The variation of memory windows is less than 11% before/after the fatigued switching cycles. In summary, it suggests that PLD PSrT films deposited at suitable substrate temperatures could be promising for MFS-FET devices.

4. Conclusions

PLD PSrT films, deposited on p-type Si wafers at low substrate temperatures (T_s) from 300 to 450 °C, exhibit the perovskite phases without significant inter-diffusion at the PSrT/Si interface. The T_s strongly enhances the film crystallinity and affects the electrical properties of Pt/PSrT/Si capacitors. As T_s increases, the films have smaller leakage current and fewer interfacial trap states at both the electrode interfaces due to fewer structural defects correlated with enhanced crystallinity. It also reveals the higher ferroelectric gate capacitance, the

larger width of C–E hysteresis loops and larger memory windows (V_m) as T_s increases. In contrast, films deposited at lower T_s (300 °C) exhibit small and counterclockwise loops with the positive voltage shift, which is ascribed to the more negative charges in the trap states. However, films deposited at high T_s (450 °C) may produce serious volatilization of Pb–O compounds, incurring more chemical defects and the leakage degradation. Besides, the fixed charge density (N_{fc}) shows the minimum value of $\sim 2.85 \times 10^{12}$ cm^{-2} for films deposited at 400 °C. The trend of N_{fc} is consistent with the flatband voltage shift (V_{ci}) and the leakage current density is dominated by space-charge limited conduction (SCLC). Furthermore, 450 °C-deposited films disclose excellent fatigue endurance before/after 10^{10} switching cycles with less than 11% variation of V_m. As a consequence, the high-quality MFS structure without a buffer layer between the PSrT films and the Si substrate could be realized by the low-temperature PLD.

Acknowledgments

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