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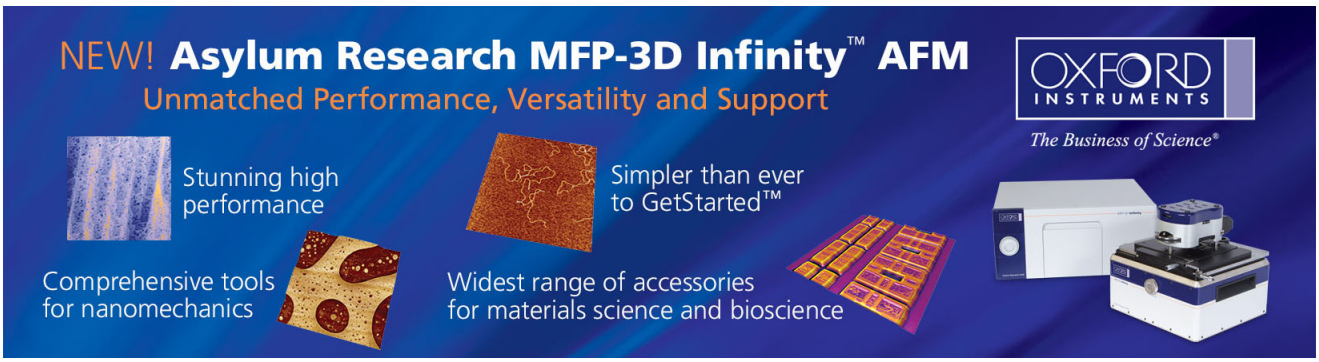

Ultrathin Si capping layer suppresses charge trapping in HfO_xN_y/Ge metal-insulator-semiconductor capacitors

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In this study the authors investigated the Ge outdiffusion characteristics of HfO_xN_y/Ge metal-insulator-semiconductor capacitors to determine their charge trapping behavior. Capping the Ge substrate with an ultrathin Si layer inhibits the incorporation of Ge into the high-*k* bulk dielectric in the form of GeO_x, thereby diminishing the resultant oxide charge trapping. The thermal stability of the entire capacitor structure was also improved after performing an additional Si passivation process. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2430629]

Great progress has been made in the deposition of high-*k* materials, enabling renewed interest in germanium (Ge) substrate as a transport channel in combination with various high-*k* dielectrics. Surface pretreatment under either an NH_3 or SiH_4 ambient was employed to further improve the electrical properties of different high-*k*/Ge systems;[1,2] in particular, SiH_4-passivated samples exhibit relatively lower interface state densities and improved gate leakage distributions.[3] We suggest that the incorporation of nitrogen atoms may lead to incomplete passivation of the dangling bonds on the Ge surface; such a surface would not fully inhibit the growth of GeO_x because of the lower thermal stability of Ge–N bonds.[4] In this letter, we report that the Si_2H_6 passivation of Ge surfaces, in which several monolayers of Si exist between the gate dielectric and Ge substrate, is a useful technique for inhibiting the formation of GeO_x and suppressing hysteresis phenomena in high-*k*/Ge metal-insulator-semiconductor (MIS) capacitors; we also present an energy band diagram to explain the charge trapping model.

n-type Ge substrates, which were doped with Sb dopant at a concentration of $\sim 1\times 10^{14}$ cm^{-3}, were precleaned through a cyclic rinse involving a diluted HF dip and deionized water. Subsequently, thermal desorption at 550 °C for 10 min through ultrahigh-vacuum chemical vapor deposition was performed to remove the native GeO_x, followed by *in situ* passivation of a Si capping layer upon annealing under a Si_2H_6 ambient at the same substrate temperature; the thicknesses—evaluated using angle-resolved x-ray photoelectron spectroscopy (XPS)—were ~8 and ~13 Å for annealing durations of 1 and 2 min, respectively. After the following deposition of high-*k* film and metallization process, the Pt/HfO_xN_y/Ge MIS capacitor structure can be obtained; the detailed deposited conditions and fabrication procedures can be found in the previous study.[5] We studied the chemical configurations of each structure through the use of secondary ion mass spectroscopy (SIMS) and *ex situ* XPS using an Al $K\alpha$ source (1486.6 eV).

Figure 1 displays the SIMS depth profiles of the chemical species present in the HfO_xN_y films on the Ge substrates (a) in the absence and (b) presence of the Si capping layer. We estimate that the overall thicknesses of the bulk HfO_xN_y and interfacial layer (IL) were ~90 and >100 Å before and after Si passivation, respectively; the probable chemical composition is also identified. An important feature of the HfO_xN_y layer was that the distribution profile of Ge was U shaped; the subsequent postdeposition annealing (PDA) process enhanced the incorporation behavior, provided that the Si_2H_6 passivation was not performed. The amount of incorporated Ge was reduced approximately fourfold after capping with the ~8-Å-thick Si layer; further retardation of Ge chemical species into the overlying high-*k* dielectric was achieved after subsequent annealing under the same condi-

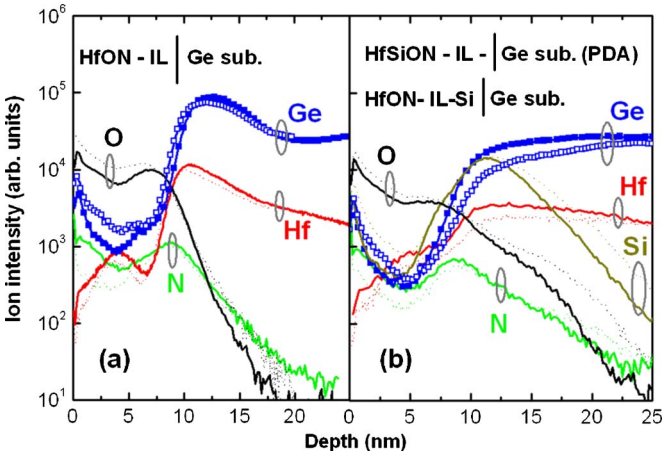

FIG. 1. (Color online) SIMS profiles of HfO_xN_y thin films deposited on Ge substrates (a) without and (b) with Si passivation. The solid lines (—) and solid squares (■) refer to the as-deposited samples; the dotted lines (---) and open squares (□) refer to the annealed samples (500 °C, 5 min).

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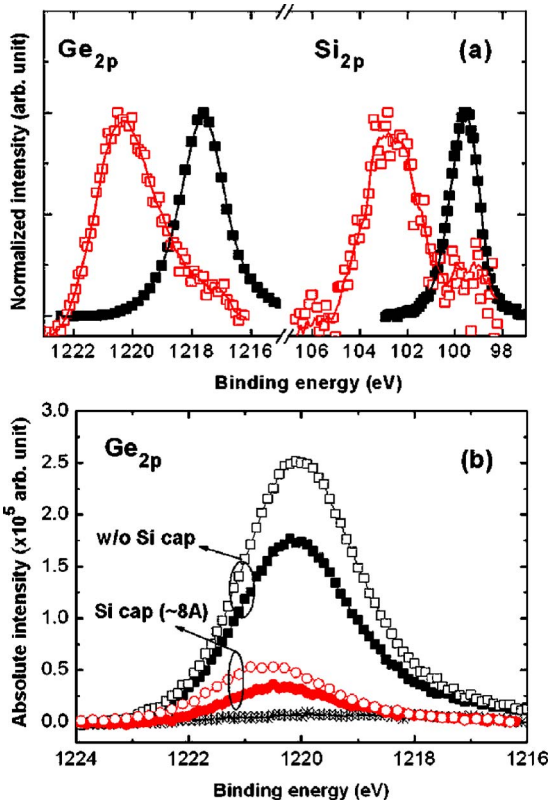

FIG. 2. (Color online) (a) XPS spectra displaying the Si $2p$ and Ge $2p$ core levels for Ge samples capped with a Si layer (~8 Å) before (■) and after (□) deposition of the HfO_xN_y high-k film. (b) Ge $2p$ spectra of $Pt/HfO_xN_y/Ge$ gate stacks before (solid symbols) and after (open symbols) dielectric annealing at 500 °C for 5 min. Note that the lowest curve (*) indicates that no Ge was incorporated into the high-k film when thermal processing—PDA and PMA—was not undertaken.

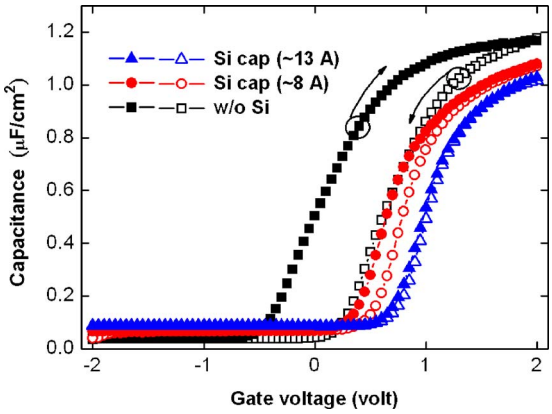

FIG. 3. (Color online) Bidirectional sweep (1 MHz) C-V curves of $Pt/HfO_xN_y/Ge$ gate stacks lacking and containing a Si capping layer. HfO_xN_y was the as-deposited thin film and the capacitors were only subjected to 400 °C PMA. C-V measurement was performed by using an HP4284 *LCR* meter.

tions. This finding provides strong evidence that employing a Si capping layer on a Ge substrate improves the thermal stability of HfO_xN_y/Ge gate stacks.

Figure 2(a) displays the Si $2p$ and Ge $2p$ core-level XPS spectra of the Ge substrate having the Si capping layer both before and after deposition of Pt/HfO_xN_y bilayers. Prior to deposition, two well-resolved peaks—originating from the signals of the Si capping layer and the Ge substrate, respectively—appeared in the corresponding core-level spectra, i.e., the native oxide was absent. After completing the entire MIS fabrication process, most of the Si atoms have transformed into Si dioxide and Hf silicate, with some nitrogen-related bonds formed; meanwhile, GeO_x ($x \leqq 2$) emerged at the top surface and also in the bulk of the high-k layer. Next, we compared [Fig. 2(b)] the relative intensities of the Ge $2p$ levels of the four SIMS samples in Figs. 1(a) and 1(b), respectively; because of the lack of sputtering yield information for Ge in the HfO_xN_y layer, we performed XPS analyses to evaluate the amounts of incorporated Ge. We estimate Ge concentrations of ~13% and ~4.3% for the nonannealed samples lacking and containing the Si capping layer, respectively, with these values increasing to ~19.6% and ~6.1%, respectively, after dielectric annealing. The nonannealed high-k dielectric sample lacking the surface passivation layer exhibited a severe degree of Ge diffusion into the top HfO_xN_y film even when postmetallization annealing (PMA) was performed at only 400 °C. Because the Ge $2p$ core level displays higher surface sensitivity,[6] the GeO_x species detected in the Ge $2p$ spectrum arose possibly through one of two incorporation mechanisms: (a) outdiffusion of gaseous GeO species from the substrate and downward into the high-k layer through airborne transportation[7] and (b) GeO volatilization from the IL and top surface of the Ge substrate. From the viewpoint that the same GeO desorption rate would be expected for mechanism (a), it is reasonable to attribute the obvious increase in the GeO_x intensity of the sample lacking the Si capping layer, with respect to that of the sample containing one, to contamination of GeO in the bulk of the high-k layer; this hypothesis is in agreement with the SIMS data.

Figure 3 displays the bidirectional sweep (1 MHz) C-V curves of the $Pt/HfO_xN_y/Ge$ gate stacks lacking and containing Si capping layers. We found that increasing the capping layer thickness suppressed the hysteresis width dramatically; its value reduced to ~20 mV upon increasing the thickness of the Si capping layer to ~13 Å. This tendency is quite consistent with the recent results reported by Wu *et al.*[8] Moreover, the flatband voltage (V_{FB}) returned to the work-function difference of ~0.8 eV between the Pt gate and the n-Ge substrate or undoped Si layer, indicating that the addition of the Si capping layer also eliminated the fixed positive charges in the gate dielectric. Our explanation for these phenomena is that it is more likely that SiO_x and its silicate will form, rather than GeO_x, after deposition and annealing when the Si capping layer is present because Si–O bonds have larger Gibbs free energies and higher thermodynamical stabilities.[9] Therefore, the formation of GeO at the interface and its outdiffusion are suppressed significantly upon increasing the thickness of the Si layer. Also, we believe that the exacerbated hysteresis width might be due to the high density of charge trapping sites at the high-k/GeO_x interface and/or within the defective GeO_x IL. We found that the increased inversion bias did lead to an increased hysteresis width, but the increased accumulation bias did not (not shown), implying that the hole trapping mechanism was dominant. Figure 4 displays our proposed charge trapping model for the $Pt/HfO_xN_y/GeOx/Ge$ gate stack, the energy band gaps of each material and their corresponding electron affinities are literature data.[10–13] As seen in Fig. 4(a), the minority carriers (in this case, holes for n-type Ge) tunnel from the Ge substrate and become trapped at the inner interface and/or within the deficient GeO_x interlayer. This phe-

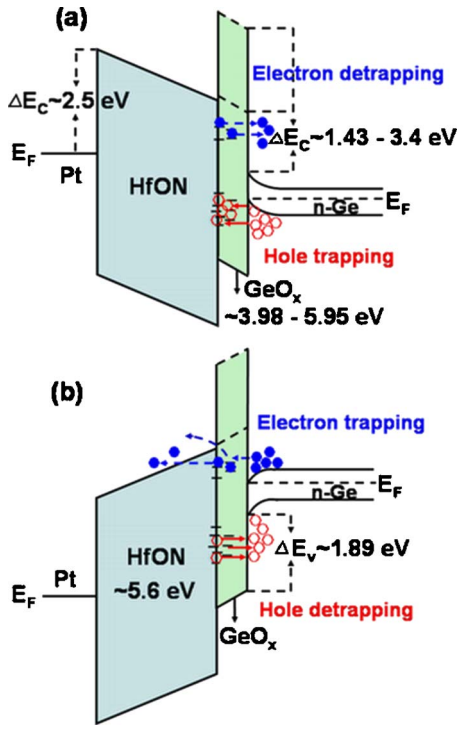

FIG. 4. (Color online) Schematic energy band diagram displaying the charge trapping model for a Pt/HfO_xN_y/GeOx/Ge gate stack upon (a) sweeping from the inversion bias ($V_g = V_{FB} - 1$ V) and (b) sweeping from the accumulation bias ($V_g = V_{FB} + 1$ V). Note that the value of V_{FB} was ~0.5 V.

nomenon causes the $C-V$ curve to shift negatively, and the value of V_{FB} to deviate, when the voltage was swept further from the negative side. In contrast, the $C-V$ curve exhibited its own value of V_{FB} without being trapped when the voltage was swept from accumulation to inversion. These results were further confirmed by the larger gate leakage current observed in the accumulation regime, with respect to that in the inversion regime, because of the higher probability for Fowler-Nordheim tunneling and thermionic emission to occur, as indicated in Fig. 4(b).

We have used physical and electrical characterization to study the effect that the passivation of an ultrathin Si layer has on Ge outdiffusion characteristics in HfO_xN_y/Ge MIS capacitors. Capping an ultrathin Si layer onto a Ge substrate retarded GeO volatilization and suppressed oxide charge trapping in the MIS structures, and thus enhanced the thermal stabilities of the entire HfO_xN_y/Ge MIS structures. We provide herein a schematic energy band diagram to explain the resultant charge trapping behavior in these systems.

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