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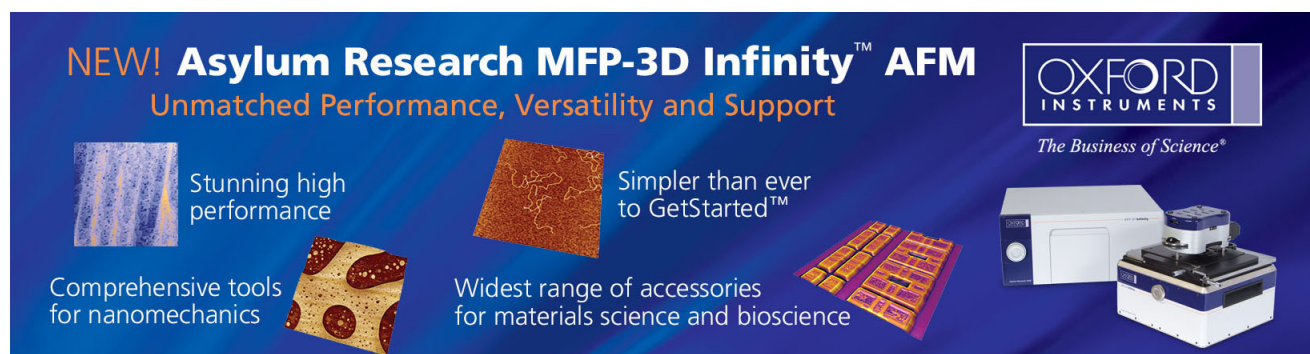
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Transparent ZnO thin film transistor fabricated by sol-gel and chemical bath deposition combination method

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Top-gate thin film transistors with *n*-type ZnO active channel were performed under 230 °C. Especially, ZnO film was deposited by a combined method of sol-gel and chemical bath deposition without any preactivation for film growth. Silicon nitride and indium tin oxide were used as the gate insulator and the conducting electrodes (source, drain, and gate). These transistors were highly transparent in the visible spectrum, with transmittance as high as 75% to approximately 85% at wavelength from 500 to 700 nm. The optimum device has field-effect mobility of 0.67 cm²/V s and an on-off ratio more than 10⁷. © 2007 American Institute of Physics. [DOI: 10.1063/1.2404590]

Transparent electronics are nowadays a crucial technology for the next generation of optoelectronic devices. Oxide-based transistors have recently been proposed as active channel.¹⁻⁷ Among them, wurtzite structured ZnO thin films have been studied as the active layer in the thin film transistors (TFTs) because of its low cost, low photosensitivity, no environmental concerns, and especially high mobility.

Other wide band-gap semiconductors, including GaN (Ref. 8) and SiC (Ref. 9) have been explored as transparent field-effect transistors. In fact, among these semiconductive oxides, ZnO has the greatest potential to grow high quality crystalline zinc oxide at low temperature. This is particularly advantageous for electronic drivers, which need to be processed at temperature that is low enough to be compatible with plastic substrates. Besides, because of their high transparency, high mobility, simple processing method, and low cost, ZnO-based semiconductors have been also applied to be active layers of TFTs. Nowadays, TFTs based on *a*-Si:H have presented some limitations, such as light sensitivity, light degradation, and low mobility. On the contrary, TFTs based on ZnO are transparent in the visible region of the spectra and less light sensitive. ZnO is presently attracting much attention due to its possibilities for replacing amorphous Si that has been widely used as the channel layer in conventional TFTs.²⁻⁴ Therefore, the future of ZnO holds great promise for applications in flexible displays and other optoelectronic devices.

A recent attempt to fabricate a ZnO-TFT utilizes chemical solution method which requires annealing steps above 600 °C.⁸ Bottom-gate configuration is widely used for ZnO-TFTs in order to maintain processing compatibility of *a*-Si:H TFTs.^{2-4,9,10} In the crystal structure of ZnO, the defects of columnar grains may be reduced by increasing the film thickness. Therefore, high mobility is more likely to be

achieved in the top-gate configuration rather than in the bottom-gate configuration.

Following these backdrops, the purpose of this letter is to demonstrate a *n*-type field-effect thin film transistor which is highly transparent in the visible region and to synthesize the ZnO thin films by a combination of sol-gel method at lower temperature and chemical bath deposition without other metal ions preactivation.

In the process of fabricating the active channel layer of ZnO films, the first layer was coated with sol-gel solution,¹¹ which has molar ratio of 2-methoxyethanol and zinc acetate Zn(CH₃COO)₂·2H₂O equal to 1.0, and the concentration of zinc acetate equal to 0.5 mol/l. The spin-on method was used for the film coating. The preheating and the postheating temperatures were, respectively, 100 and 230 °C on hotplate. In order to reduce grain boundary thus improve electron mobility, the columnar grain size must be increased. This approach was accomplished by optimizing the chemical bath deposition (CBD) for the second layer of ZnO film. The CBD solution contained 0.1 mol/l zinc nitrate and 0.03 mol/l dimethylamineborane, and the substrate was immersed in the soak solution for the film growth at 60 °C.¹² Then the ZnO film was patterned using standard lithography and wet etching process.

The ZnO-TFT, a simple top-gate configuration, was fabricated onto a Corning 1737 glass substrate, as shown in Figs. 1(a) and 1(b). The optimized ZnO semiconductor films were fabricated, which the source and drain were coated with 100-nm-thick layer of indium tin oxide (ITO) by sputtering (patterned by lift-off technique). Each source-drain pair was defined of a channel width $W=500\ \mu\text{m}$ and channel length $L=10\ \mu\text{m}$. A silicon nitride (SiN_x) film is used for the gate dielectric which thickness was 300 nm and patterned by shadow mask. The ITO film of 100 nm was used as the gate electrodes.

Scanning electron microscopy (SEM, Hitachi 4700) is employed to characterize the device structure and morphol-

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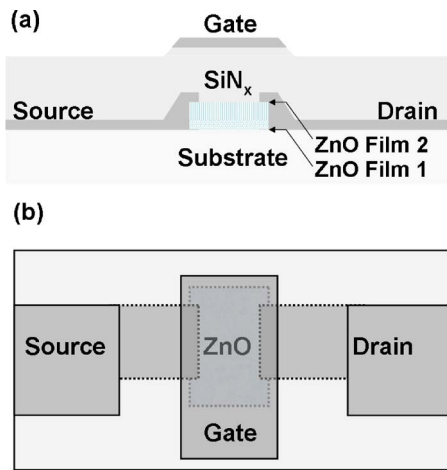


FIG. 1. (Color online) Top-gate structure of ZnO-TFT in which (a) is cross-sectional schematic and (b) is top view schematic.

ogy of the prepared films. Figure 2 shows the morphology of ZnO film and local image of ZnO-TFT device, which indicate that through chemical bath deposition grains can be grown on the sol-gel film compactly without any surface treatment and the mean thickness is 200 nm [as shown insert (a) of Fig. 2]. The grains of upper layer are larger than those of the lower layer obviously, even though there exists an unclear interface between the upper and lower layers. We predicted that the ZnO film by CBD can anchor and self-align on the preformed particles of sol-gel layer. The films of

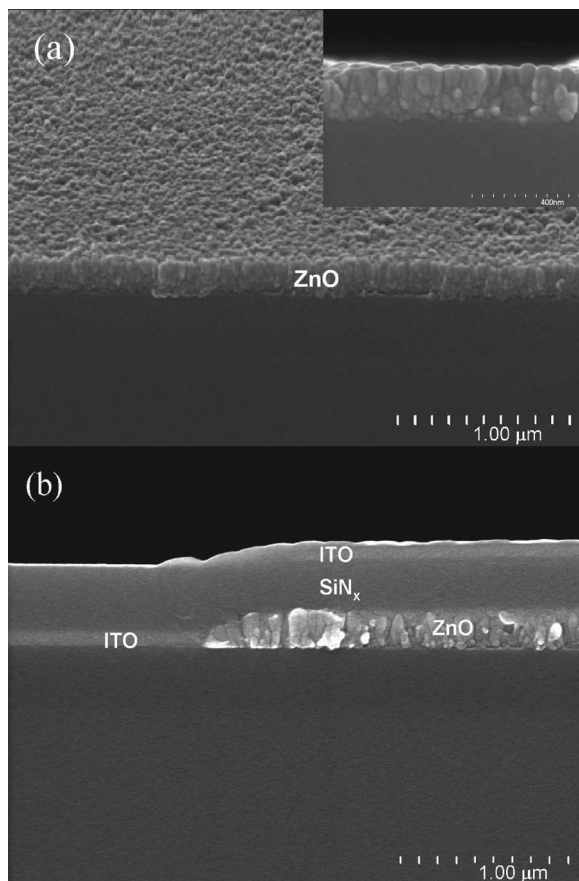


FIG. 2. SEM images of (a) ZnO films on Corning 1737 glass substrate by 45° tilt angle, the insert is a cross section view of scale up from the local of ZnO film with a 400 nm scale. (b) Local cross section view of ZnO-TFT on Corning 1737 glass substrate.

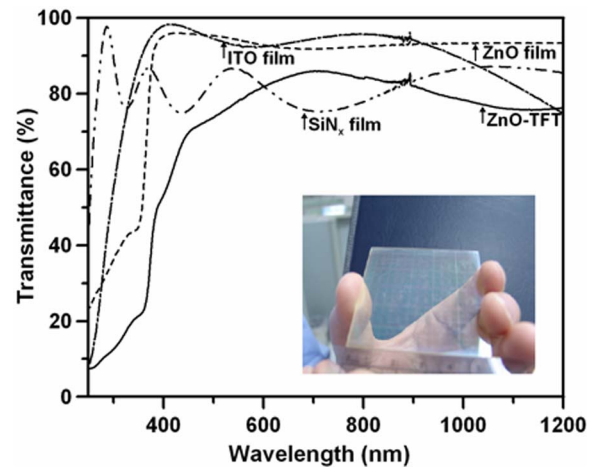


FIG. 3. (Color online) Optical transmission spectra for the top-gate structure of ZnO-TFT (except substrate) through the ITO film (gate), SiNx (gate insulator), and (ZnO film) channel region, and the thicknesses are 100, 300, and 200 nm, respectively. The insert shows a 5 × 5 cm² substrate with 75 devices of ZnO-TFT on Corning 1737 glass substrate.

the Fig. 2(a), with regular and compact amassment grains vertical to the substrate, prove that the inference to be true. Moreover, we emphasize that film defects of columnar grains may be reduced with larger size of grains. Therefore, mobility improvement is achieved in the top-gate configuration for the current growth method of ZnO films. The ZnO-TFT devices are demonstrated [refer to insert (b) of Fig. 2].

All the optical transmittance of the deposited films was measured using an UV-visible-NIR scanning spectrophotometer (Shimadzu UV-3101PC) at wavelengths from 250 to 1200 nm. Figure 3 shows optical transmission spectra through the ZnO-TFT (except substrate), which includes the ITO film (gate), SiNx (gate insulator), and (ZnO film) channel region, of thicknesses 100, 300, and 200 nm, respectively. The transistors were highly transparent in the visible range, with transmittance as high as 75% to approximately 85% at wavelengths from 500 to 700 nm. The photo of the Fig. 3 inserted shows a clearly visible 5 × 5 cm² glass substrate with 75 devices of ZnO-TFT.

The transistor devices were analyzed with an Agilent 4155B semiconductor parameter analyzer at room temperature and were measured in the dark room. Typical I_D - V_D curve and I_D - V_G curve of a ZnO-TFT are shown in the Fig. 4. Current-voltage properties measured through the gate infer that the ZnO channel is n -type enhancement mode device due to a positive gate voltage are required to induce a conducting channel, and the current increases with increasing positive gate bias. Figure 4(a) shows the drain current (I_D) as a function of source-drain voltage (V_D) for gate voltage (V_G) between 0 and 40 V for the device. The slope of each I_D curve is flat for large V_D , indicating hard saturation, which possesses large output impedance that is desirable for most circuit application. Figure 4(b) shows the corresponding transfer characteristic of I_D vs V_G at a fixed V_{DS} of 20 V for the same TFT device. The I_D - V_G curve reveals a drain current with on to off ratio of more than 10⁷. The threshold voltage (V_{th}) and saturation mobility were defined by fitting a straight line to the plot of the square root of I_D vs V_G , calculated by the formula of saturated regions:

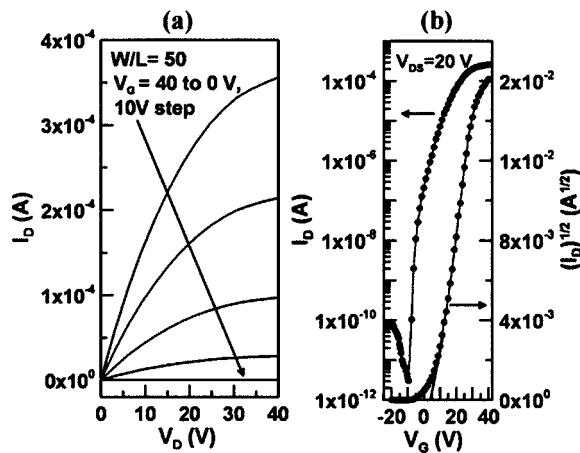


FIG. 4. (a) Drain current-drain voltage (I_D - V_D) curves at gate voltage (V_G) between 0 and 40 V for a ZnO-TFT with channel width to length ratio (W/L) of 50. (b) Transfer characteristics, I_D vs V_G at $V_{DS}=20$ V for the same ZnO-TFT. It is also indicated the square root of drain current vs the gate voltage from which is determined the threshold voltage.

$$I_{DS} = \mu_{FEsat}(W/2L)C_I(V_{GS} - V_{th})^2,$$

where W and L are the channel width and length, respectively, and C_I is the capacitance per unit area of gate insulator. The V_{th} is 6 V and saturated region mobility (μ_{FEsat}) was calculated of $0.67 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

We have demonstrated a method of fabricating highly transparent ZnO-TFT by sol-gel and CBD combined method at a relatively low temperature without any other metal ion preactivation or surface treatment. Especially, for the growth of the ZnO films, we do not require a vacuum atmosphere. ZnO is one of a few oxides that can be grown as a crystalline

film by solution method, on a variety of surfaces,^{1,7,13} such as amorphous glasses, plastics, and crystalline films. It can also be grown on its preformed nanocrystalline films. This result particularity extends the application of ZnO in electronics field.

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