An Output Buffer for 3.3-V Applications in a 0.13-μm 1/2.5-V CMOS Process

Shih-Lun Chen, *Student Member, IEEE*, and Ming-Dou Ker, *Senior Member, IEEE*

***Abstract*—With a 3.3-V interface, such as PCI-X application, high-voltage overstress on the gate oxide is a serious reliability problem in designing I/O circuits by using only 1/2.5-V low-voltage devices in a 0.13-μm CMOS process. Thus, a new output buffer realized with low-voltage (1- and 2.5-V) devices to drive high-voltage signals for 3.3-V applications is proposed in this paper. The proposed output buffer has been fabricated in a 0.13-μm 1/2.5-V 1P8M CMOS process with Cu interconnects. The experimental results have confirmed that the proposed output buffer can be successfully operated at 133 MHz without suffering high-voltage gate-oxide overstress in the 3.3-V interface. In addition, a new level converter that is realized with only 1- and 2.5-V devices that can convert 0/1-V voltage swing to 1/3.3-V voltage swing is also presented in this paper. The experimental results have also confirmed that the proposed level converter can be operated correctly.**

***Index Terms*—Gate-oxide reliability, level converter, mixed-voltage I/O, output buffer.**

I. Introduction

As the semiconductor process is scaled down, the thickness of the gate oxide becomes thinner in order to decrease the core power supply voltage (VDD) [1]. This results in lower power consumption. However, the board voltage (VCC) is still kept as high as 3.3 V (or 5 V), such as in a PCI-X interface [2]. There are three problems on a MOSFET when the operating voltage is higher than its normal voltage. Higher drain-to-source voltage V_{ds} may cause serious hot-carrier effect, which results in long-term lifetime issue [3]. Drain-to-bulk p-n junction breakdown may occur if the operating voltage is too high. High-voltage overstress across the thinner gate oxide could also destruct the gate oxide [4], [5]. Therefore, I/O circuits must be designed carefully to overcome these problems, especially high-voltage gate-oxide overstress [6]–[10].

Recently, dual-oxide (thin oxide and thick oxide) processes have been supported by some manufacturing companies [11]–[13]. For example, the thin-oxide devices are 1- or 1.2-V devices, and the thick-oxide devices are 1.8-, 2.5-, or 3.3-V devices in a 0.13-μm CMOS process [12], [13]. The thin-oxide devices are used to design digital circuits to decrease silicon area and power consumption. The thick-oxide devices are used to design analog circuits to improve circuit performance or I/O circuits to avoid the gate-oxide reliability issue. Fig. 1 shows a conventional tristate I/O buffer codesigned with thin- and thick-oxide devices. As shown in Fig. 1, transistors P1 and N1 are thick-oxide devices, which can sustain the voltage level of VCC to avoid the gate-oxide reliability issue. Since the core circuits are operated at VDD, the voltage swing of signals IN, EN, and ENB is from GND to VDD. However, the voltage swing of the output signal is from GND to VCC. Thus, the level converter is required to convert the GND-to-VDD signal to a GND-to-VCC signal in order to prevent the high-voltage overstress across the core devices. The conventional level converter codesigned with thin- and thick-oxide devices is shown in Fig. 2, where transistors P1, P2, N1, and N2 are thick-oxide devices, but transistors P3 and N3 are thin-oxide devices. The voltage swing of signals IN and INB is from GND to VDD, whereas the voltage swing of signal OUT is from GND to VCC. If the voltage gap between VDD and VCC is too large, such conventional level converter cannot be operated correctly. Some techniques have been reported to solve this problem [14]–[17]. The use of precharging devices to increase the pull-up capacity was reported in [14]. A boosting technique was reported to pump the input voltage swing of the level converter [15], [16]. The zero-Vt (also called native-Vt) n-channel MOS (NMOS) transistor was used to design the level converter for higher driving capability [17].

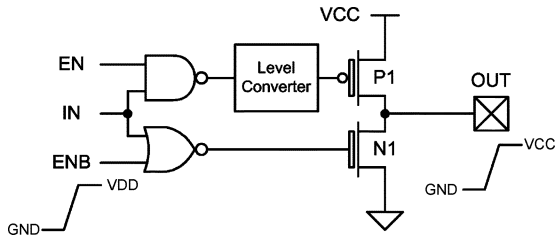

Fig. 1. Conventional tristate output buffer codesigned with thin- and thick-oxide devices.

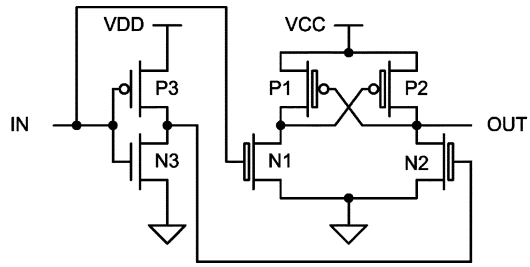

Fig. 2. Conventional level converter codesigned with thin- and thick-oxide devices.

Manuscript received February 3, 2005; revised March 3, 2006. This work was supported in part by the National Science Council, Taiwan, R.O.C., under Contract NSC 95-2221-E-009-290. This paper was recommended by Associate Editor R. Puri.

The authors are with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: mdker@ieee.org).

Digital Object Identifier 10.1109/TCSII.2006.883202

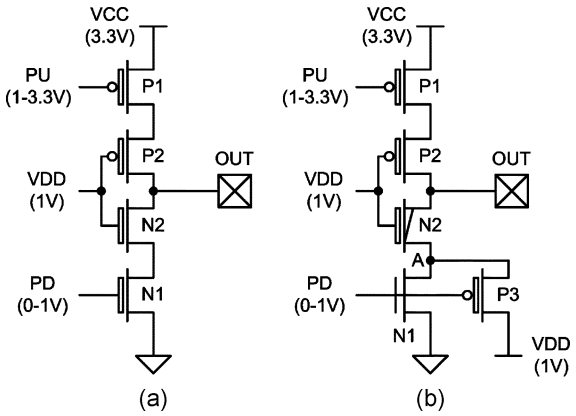

Fig. 3. New proposed output stages realized in a 0.13-μm 1/2.5-V CMOS process with (a) all 2.5-V normal-Vt transistors and (b) 2.5-V native-Vt transistor N2 and 1-V normal-Vt transistor N1.

Due to the high-integration trend of system-on-chip, a system including digital circuits and analog circuits may be integrated into a single chip. For example, the digital part of a chip is designed with 1-V devices to decrease its power dissipation, the analog part is designed with 2.5-V devices to improve the circuit performance, and the chip-to-chip interface is a 3.3-V PCI-X interface in a 0.13-μm 1/2.5-V CMOS process. In [18], an input buffer in a 0.13-μm 1/2.5-V CMOS process is reported to receive 3.3-V input signals. However, how to drive 3.3-V output signals by 1- and 2.5-V devices was not reported yet.

In this brief, a new output buffer is designed in a 0.13-μm 1/2.5-V CMOS process to drive 3.3-V output signals without the gate-oxide reliability issue [19]. Besides, a new level converter that can convert 0/1-V signals to 1/3.3-V signals is also presented in this paper. The proposed output buffer and level converter have been successfully verified in the 0.13-μm 1/2.5-V CMOS process without gate-oxide reliability issue.

II. New Proposed Output Buffer

A. Output Stage Design

Because the proposed output buffer is designed in a 0.13-μm 1/2.5-V CMOS process, the gate-to-source and gate-to-drain voltages of the thin-oxide devices cannot exceed 1 V. The gate-to-source and gate-to-drain voltages of the thick-oxide devices cannot exceed 2.5 V. However, the VCC of the PCI-X specification is 3.3 V [2]. Therefore, the output stage must be stacked, and the gate voltages must be well controlled to prevent high-voltage overstress on their gate oxides. The new proposed output stages are shown in Fig. 3. To avoid body effect, which results in lower driving capacity, the bulks of the transistors in Fig. 3 are connected to their sources individually. In Fig. 3(a), the pull-up and pull-down paths have two stacked 2.5-V p-channel MOS (PMOS) transistors (P1 and P2) and 2.5-V nMOS transistors (N1 and N2), respectively. Since the gate voltages of transistors P2 and N2 are biased at VDD (1 V), the extra bias generator is not required. Because the gate voltages of transistors P2 and N2 are biased at 1 V, the gate-to-source voltages $V_{\rm gs}$ and the gate-to-drain voltages $V_{\rm gd}$ of transistors P2 and N2 do not exceed 2.5 V. The maximum $V_{\rm gs}$ and $V_{\rm gd}$ of transistors P2 and N2 are about 2.3 V $(3.3-1=2.3)$. Transistors P2 and N2 are used to protect transistors P1 and N1 against the high-voltage gate-oxide overstress, respectively. However, the source voltage of transistor P1 is 3.3 V. In this design, the minimum voltage level of signal PU cannot be lower than 0.8 V $(3.3-2.5=0.8)$. The voltage swing of signal PU can be designed between 1 V (VDD) to 3.3 V (VCC) to control the gate of transistor P1. Hence, a level converter that can convert 0/1-V voltage swing to 1/3.3-V voltage swing is demanded for the proposed output buffer.

In Fig. 3(a), transistors N1 and N2 are 2.5-V normal-Vt nMOS transistors with a threshold voltage of 0.6 V, which is still too high for high-speed operation when the $V_{\rm gs}$ of the normal-Vt nMOS transistor is only 1 V. Hence, the driving capability of the pull-down path in Fig. 3(a) needs to be improved. Therefore, a modified version of the output stage is shown in Fig. 3(b). Transistor N2 in Fig. 3(b) is a 2.5-V native-Vt nMOS transistor, which has a threshold voltage of -0.1 V [20]. Transistor N1 in Fig. 3(b) is a 1-V nMOS transistor. The native-Vt nMOS transistor is one of the standard devices in a 0.13-μm CMOS process without extra process modification [12]. Therefore, the driving capability of the output buffer in Fig. 3(b) can be increased. Because the gate of transistor N2 is biased at 1 V, transistor N1 in Fig. 3(b) can be safely operated without suffering high-voltage gate-oxide overstress. However, since transistor N2 is a native-Vt nMOS transistor, the subthreshold leakage current could be serious. If the voltage on node OUT in Fig. 3(b) is 3.3 V, the subthreshold current of transistor N2 may occur. Thus, the voltage on node A in Fig. 3(b) may exceed 1 V. An extra pMOS transistor P3 is added in Fig. 3(b) to keep the maximum voltage on node A at 1 V. When signals PU and PD are at logic "0" (1 and 0 V), the voltage on node OUT is VCC (3.3 V). Because signal PD is at 0 V, transistor P3 is turned on to keep the voltage on node A at 1 V. Hence, the high-voltage gate-oxide overstress caused by the subthreshold leakage of transistor N2 can be avoided. Because transistor P3 is a weak device that keeps the voltage on node A at 1 V, it can be a 2.5-V normal-Vt pMOS transistor. Fig. 4 shows the simulated waveforms of the output stages in a 0.13-μm CMOS process with 1- and 2.5-V devices. In this simulation, the transistor sizes of these two output stages are kept the same. As shown in Fig. 4, the driving speed of the output stage in Fig. 3(b) is better than that of the output stage in Fig. 3(a).

B. Level Converter Design

Fig. 5 shows the new proposed level converter that can convert 0/1-V voltage swing to 1/3.3-V voltage swing. In Fig. 5, the bulks of the transistors are connected to their sources, respectively, because of the body effect issue. Transistors N1A and N1B are 1-V normal-Vt nMOS transistors, whereas transistors N2A and N2B are 2.5-V native-Vt nMOS transistors, so the driving capability can be increased. The other transistors are all 2.5-V normal-Vt transistors. Transistors P3A can keep the voltage on node A1 at 1 V when the voltage on node B1 is 3.3 V. Similarly, transistor P3B is used to keep the voltage on node A2 at 1 V when the voltage on node B2 is 3.3 V. The voltage swing of input signals IN and INB is from 0 to 1 V. When signal IN is 1 V and signal INB is 0 V, the voltage on node B1 is pulled

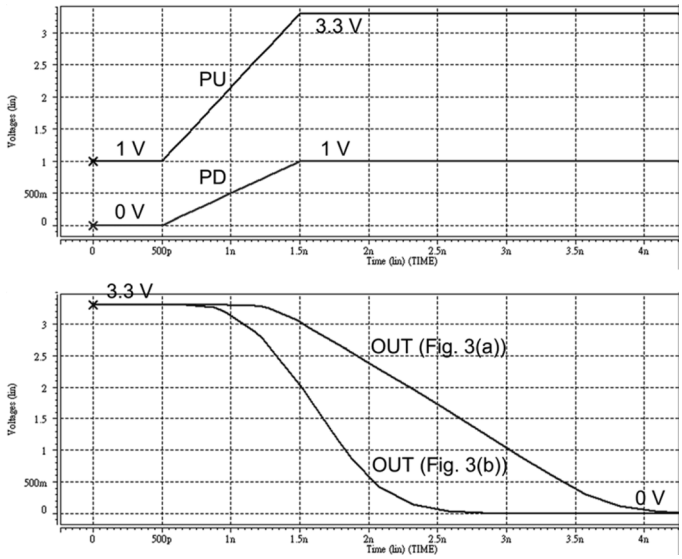

Fig. 4. Simulated waveforms of the output stages.

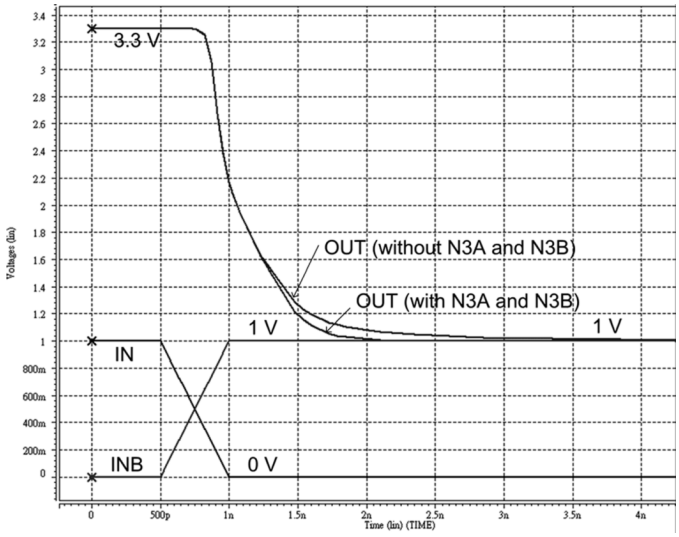

Fig. 6. Simulated waveforms of the new proposed level converter with or without transistors N3A and N3B.

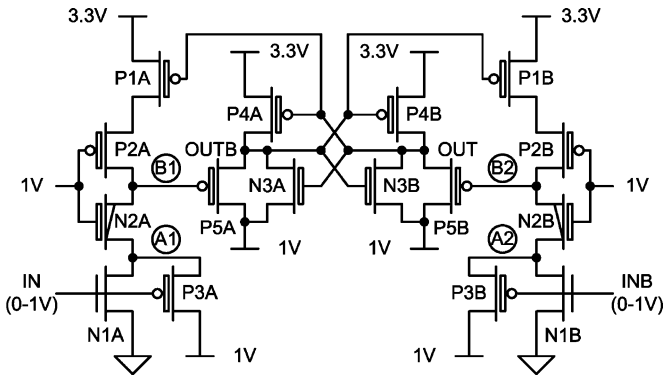

Fig. 5. New proposed level converter that can convert 0/1-V signal swing to 1/3.3-V signal swing.

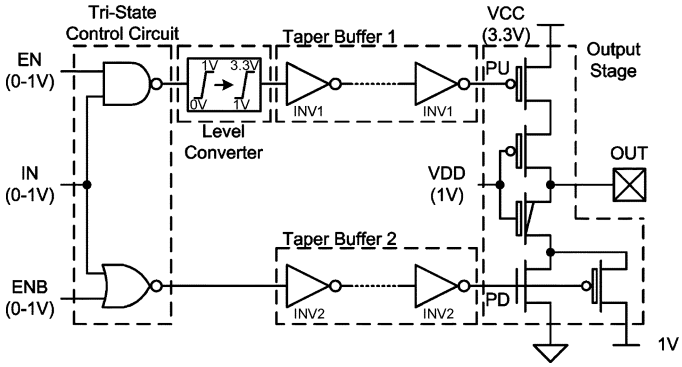

Fig. 7. Whole output buffer that drives the 3.3-V output signal in the 0.13-μm CMOS process with only 1- and 2.5-V devices.

down to 0 V, and transistor P5A is turned on. After transistor P5A is turned on, the voltage on node OUTB is pulled down to 1 V, and then, transistors P4B and P1B are turned on. Therefore, the voltages on nodes OUT and B2 are both pulled up to 3.3 V.

When signal IN is 0 V and signal INB is 1 V, the voltage on node B2 is pulled down to 0 V, and transistor P5B is turned on. After transistor P5B is turned on, the voltage on node OUT is pulled down to 1 V, and then, transistors P4A and P1A are turned on. Therefore, the voltages on nodes OUTB and B1 are both pulled up to 3.3 V.

Because using pMOS transistors to pull down nodes OUT and OUTB could be too slow, two cross-coupled nMOS transistors N3A and N3B are added to increase the pull-down speed. Fig. 6 shows the simulated waveforms of the new proposed level converter in a 0.13-μm 1/2.5-V CMOS process. The pull-down speed of the proposed level converter with transistors N3A and N3B is faster than that of the level converter without N3A and N3B.

C. Whole Output Buffer

Fig. 7 depicts the whole output buffer, which consists of an output stage, a level converter, a tristate control circuit, and two

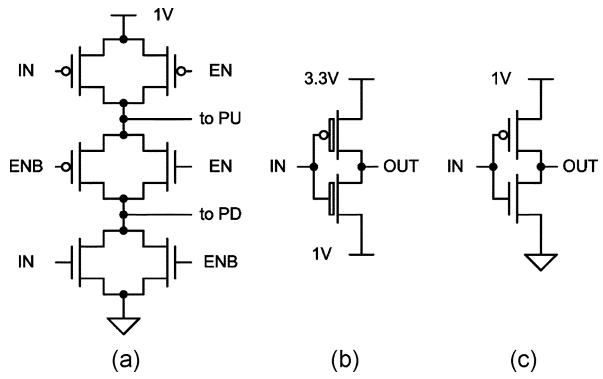

Fig. 8. Circuit implementation to realize the (a) tristate control circuit, (b) INV1, and (c) INV2 in the whole output buffer.

kinds of taper buffers (taper buffer 1 and taper buffer 2). In Fig. 7, a CMOS NAND gate and a NOR gate are used to implement the tristate control circuit. When control signal EN is 0 V and control signal ENB is 1 V, the output buffer is in the high-impedance state. When control signal EN is 1 V and control signal ENB is 0 V, the output buffer drives the output pad according to signal IN from the core circuits. Fig. 8(a) shows

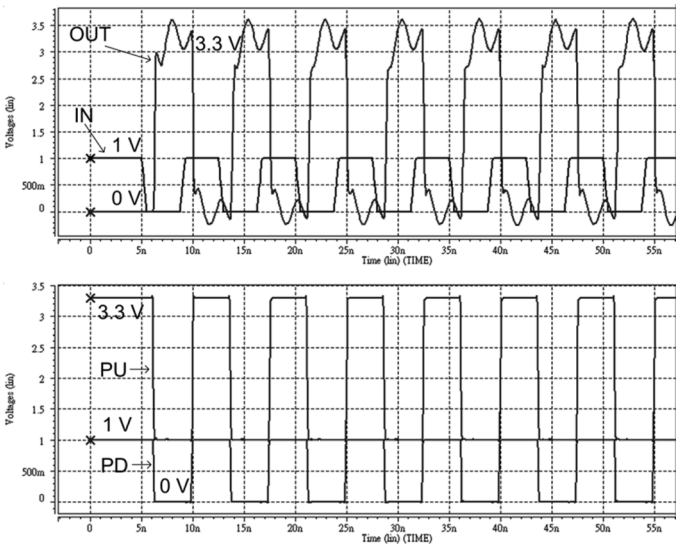

Fig. 9. Simulated waveforms of the proposed output buffer operating with a 133-MHz 3.3-V output signal in a 0.13-μm CMOS process with only 1- and 2.5-V devices.

TABLE I
SIMULATION RESULTS OF THE PROPOSED OUTPUT BUFFER

Rising Delay Time ($T_{d\text{-}rising}$)	1.15 ns
Falling Delay Time ($T_{d\text{-}falling}$)	1.08 ns
Rising Time (T_{rising})	0.85 ns
Falling Time ($T_{falling}$)	0.73 ns
Output Low Current (I_{OL})	59.3 mA
Output High Current (I_{OH})	39.4 mA
Power Consumption	29.77 mW

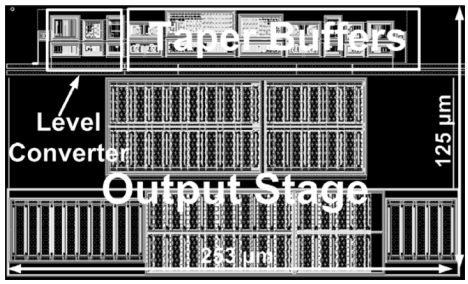

Fig. 10. Layout of the whole output buffer in a 0.13-μm 1/2.5-V CMOS process with Cu interconnects.

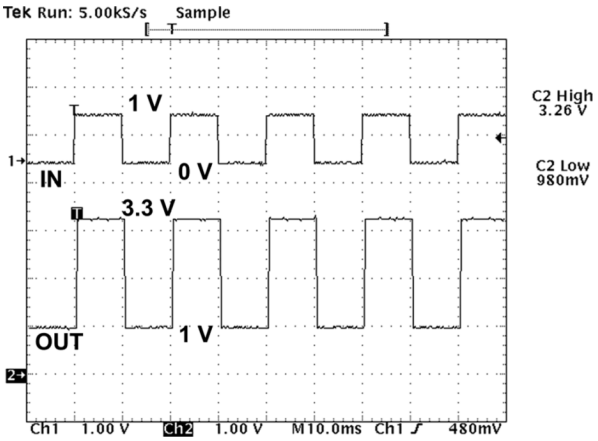

Fig. 11. Measured waveforms of the new proposed level converter, which convert the 0/1-V signal to a 1/3.3-V signal.

another tristate control circuit, which consists of only six transistors [21]. Compared with the traditional tristate control circuit in Fig. 7, the circuit in Fig. 8(a) may have smaller silicon area and input capacitance. Thus, the tristate control circuit in Fig. 8(a) can be used to replace the traditional tristate control circuit in Fig. 7. The output stage of this whole output buffer is the same as that in Fig. 3(b). The level converter that can transfer the signal swing from 0/1 to 1/3.3 V has been shown in Fig. 5. Taper buffer 1 and taper buffer 2 are demanded to drive the output stage because the transistors in the output stage are large-size devices. Because the voltage swing of signal PU is from 1 to 3.3 V, the INV1 in taper buffer 1 is shown in Fig. 8(b). The pMOS and nMOS transistors of INV1 are 2.5-V normal-Vt devices. Because the voltage swing of signal PD is from 0 to 1 V, the INV2 in taper buffer 2 is shown in Fig. 8(c), where the pMOS and nMOS transistors of INV2 are 1-V normal-Vt transistors. In order to keep signals PU and PD in phase, the delay of taper buffer 1 and the level converter must be adjusted equal to that of taper buffer 2. In Fig. 8, the bulks of the transistors are connected to their sources, respectively, because of the body effect.

Fig. 9 shows the simulated waveforms on nodes IN, OUT, PU, and PD in the proposed output buffer operating with a 133-MHz 3.3-V output signal in a 0.13-μm 1/2.5-V CMOS process. The output load is 10 pF in this simulation. Because the parasitic inductance (15 nH) of the bond wire has also been included in this simulation, the overshoot and undershoot of the output waveform can be found in Fig. 9. Table I shows the other simulation results of the proposed output buffer. The delay times are measured from the input signal (IN) of 0.5 $\times$ VDD (0.5 V) voltage level to the output signal (OUT) of 0.5 $\times$ VCC (1.65 V) voltage level. As shown in Table I, the simulated rising delay time $T_{\mathrm{d-rising}}$ and falling delay time $T_{\mathrm{d-falling}}$ are 1.15 and 1.08 ns, respectively. The output rising time T_{rising} and falling time T_{falling} are defined from 0.1 $\times$ VCC (0.33 V) to 0.9 $\times$ VCC (2.97 V) and from 0.9 $\times$ VCC (2.97 V) to 0.1 $\times$ VCC (0.33 V), respectively. As shown in Table I, the simulated T_{rising} and T_{falling} are 0.85 and 0.73 ns, respectively. The output low current I_{OL} is defined when the output voltage is at 0.1 $\times$ VCC (0.33 V). The output high current I_{OH} is defined when the output voltage is at 0.9 $\times$ VCC (2.97 V). As shown in Table I, the simulated I_{OL} and I_{OH} are 59.3 and 39.4 mA, respectively. The simulated power consumption is 29.77 mW when the proposed output buffer is operated at 133 MHz with a 10-pF capacitive load at the pad. In this simulation, the proposed output buffer successfully drives the pad according to the input signal IN.

III. EXPERIMENTAL RESULTS

The proposed output buffer has been fabricated in a 0.13-μm 1/2.5-V 1P8M CMOS process with Cu interconnects. Fig. 10 shows the layout of the proposed output buffer. The layout area of the proposed output buffer is around 125 μm $\times$ 253 μm. Besides, the test chip also includes the stand-alone level converter to verify its logic functions and voltage levels. Fig. 11 shows the measured waveforms of the new proposed level converter. As

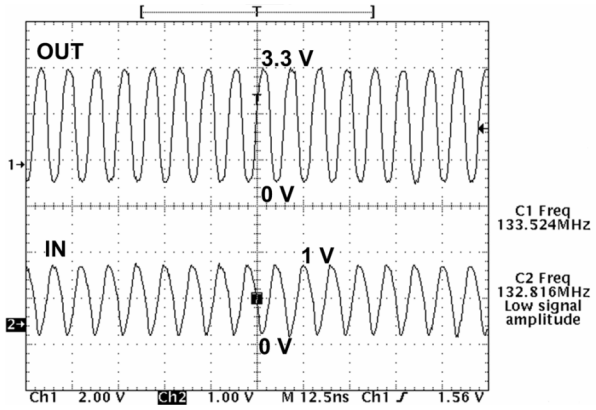

Fig. 12. Measured waveforms of the proposed whole output buffer operating with a 133-MHz 3.3-V output signal in a 0.13-μm CMOS process with only 1- and 2.5-V devices.

shown in Fig. 11, the proposed level converter can successfully transfer the voltage swing from 0/1 to 1/3.3 V. Fig. 12 shows the measured waveforms of the proposed whole output buffer operating with a 133-MHz 3.3-V output signal. As shown in Fig. 12, the proposed output buffer can successfully drive the output pad without gate-oxide overstress. Besides, the measured $I_{\rm OL}$ and $I_{\rm OH}$ of the proposed output buffer are 69.2 and 44.1 mA, respectively. Due to process variation, the measured $I_{\rm OL}$ and $I_{\rm OH}$ are slightly different from the simulated $I_{\rm OL}$ and $I_{\rm OH}$.

IV. Discussion

The hot-carrier degradation and drain-to-bulk breakdown issues are the other reliability issues in the high-voltage-tolerant circuits. To avoid the hot-carrier degradation, the drain-to-source voltage $V_{\rm ds}$ of the device operated in the saturation region cannot be higher than the normal operating voltage [3]. For example, the $V_{\rm ds}$ of the 1-V (2.5-V) device cannot be higher than 1 V (2.5 V). The maximum $V_{\rm ds}$ of 1- and 2.5-V devices in the proposed output buffer are about 1 and 2.3 V, respectively. Thus, the proposed output buffer not only considers the gate-oxide reliability issue but also the hot-carrier degradation issue. In general, the drain-to-bulk breakdown voltage is at least twice the normal operating voltage in the standard CMOS process [12], [13]. Hence, the drain-to-bulk breakdown issue can be ignored in the proposed output buffer.

V. Conclusion

An output buffer realized with low-voltage devices to drive high-voltage output signals is presented in this paper. The proposed output buffer has been fabricated in a 0.13-μm 1/2.5-V CMOS process to drive 3.3-V signals without suffering high-voltage gate-oxide overstress. The experimental results have shown that the proposed output buffer can be successfully operated with a 133-MHz 3.3-V output signal. Moreover, a new level converter that can convert 0/1-V signal swing to 1/3.3-V signal swing, has also been verified in this paper. The proposed output buffer and level converter are suitable for mixed-voltage interface applications in the nanometer CMOS processes.

References

[1] Semiconductor Industry Association, International Technology Roadmap for Semiconductors 2003.
[2] PCI Special Interest Group (PCI-SIG), PCI-X 1.0 Specification 1999.
[3] I.-C. Chen, J. Y. Choi, and C. Hu, "The effect of channel hot-carrier stressing on gate-oxide integrity in MOSFETs," *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 2253–2258, Dec. 1988.
[4] R. S. Scott, N. A. Dumin, T. W. Hughes, D. J. Dumin, and B. T. Moore, "Properties of high-voltage stress generated traps in thin silicon oxide," *IEEE Trans. Electron Devices*, vol. 43, no. 7, pp. 1133–1143, Jul. 1996.
[5] T. Furukawa, D. Turner, S. Mittl, M. Maloney, R. Serafin, W. Clark, L. Longenbach, and J. Howard, "Accelerated gate-oxide breakdown in mixed-voltage I/O circuits," in *Proc. IEEE Int. Reliab. Phys. Symp.*, 1997, pp. 169–173.
[6] M. J. M. Pelgrom and E. C. Dijkmans, "A 3/5 V compatible I/O buffer," *IEEE J. Solid-State Circuits*, vol. 30, no. 7, pp. 823–825, Jul. 1995.
[7] M.-D. Ker and C.-H. Chung, "Electrostatic discharge protection design for mixed-voltage I/O buffers," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1046–1055, Aug. 2002.
[8] M.-D. Ker and C.-S. Tsai, "Design of 2.5 V/5 V mixed-voltage CMOS I/O buffer with only thin oxide device and dynamic n-well bias circuits," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2003, vol. 4, pp. 97–100.
[9] C.-H. Chuang and M.-D. Ker, "Design on mixed-voltage-tolerant I/O interface with novel tracking circuits in a 0.13-μm CMOS technology," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2004, vol. 2, pp. 577–580.
[10] M.-D. Ker and S.-L. Chen, "Mixed-voltage I/O buffer with dynamic gate-bias circuit to achieve 3 × VDD input tolerance by using 1 × VDD devices and single VDD power supply," in *Proc. IEEE Int. Solid-State Conf. Dig. Tech. Papers*, 2005, pp. 524–525, 614.
[11] M. Hargrove, S. Crowder, E. Nowak, R. Logan, L. K. Han, H. Ng, A. Ray, D. Sinitsky, P. Smeys, F. Guarin, J. Oberschmidt, E. Crabbé, D. Yee, and L. Su, "High-performance sub-0.08 μmCMOS with dual gate oxide and 9.7 ps inverter delay," in *IEDM Tech. Dig.*, 1998, pp. 627–630.
[12] K.-K. Young *et al.*, "A 0.13 μm CMOS technology with 93 nm lithography and Cu/low-k for high performance applications," in *IEDM Tech. Dig.*, 2000, pp. 563–566.
[13] C. S. Chang *et al.*, "Extended 0.13 μmCMOS technology for ultra high-speed and MS/RF application segments," in *Proc. Symp. VLSI Technol. Dig. Tech. Papers*, 2003, pp. 68–69.
[14] C.-C. Yu, W.-P. Wang, and B.-D. Liu, "A new level converter for low-power applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2001, vol. 1, pp. 113–116.
[15] N. Otsuka and M. A. Horowitz, "Circuit techniques for 1.5-V power supply flash memory," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1217–1230, Aug. 1997.
[16] Y. Kanno, H. Mizuno, K. Tanaka, and T. Watanabe, "Level converter with high immunity to power-supply bouncing for high-speed sub-1-V LSIs," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, 2000, pp. 202–203.
[17] W.-T. Wang, M.-D. Ker, M.-C. Chiang, and C.-H. Chen, "Level shifters for high-speed 1-V to 3.3-V interfaces in a 0.13-μm Cu-interconnection /low-k CMOS technology," in *Proc. IEEE Int. Symp. VLSI Tech., Syst., Appl.*, 2001, pp. 307–310.
[18] S.-L. Chen and M.-D. Ker, "A new Schmitt trigger circuit in a 0.13-μm 1/2.5-V CMOS process to receive 3.3-V input signals," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 7, pp. 361–365, Jul. 2005.
[19] ——, "A new output buffer for 3.3-V PCI-X application in a 0.13-μm 1/2.5-V CMOS process," in *Proc. IEEE Asia-Pacific Conf. Adv. Syst. Integr. Circuits*, 2004, pp. 380–383.
[20] Taiwan Semiconductor Manufacturing Company, TSMC 0.13 μm Logic 1P8M Salicide 1.0V/2.5V, 1.2V/2.5V, 1.0V/3.3V, 1.2V/3.3V Design Rule rev. 1.5, 2003.
[21] D.-Y. Chen, "Design of a mixed 3.3V and 5V PCI I/O buffer," in *Proc. IEEE Int. Conf. ASIC*, 1996, pp. 336–339.