Ultra-High-Voltage Charge Pump Circuit in Low-Voltage Bulk CMOS Processes With Polysilicon Diodes

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***Abstract*—An on-chip ultra-high-voltage charge pump circuit realized with the polysilicon diodes in the low-voltage bulk CMOS process is proposed in this work. Because the polysilicon diodes are fully isolated from the silicon substrate, the output voltage of the charge pump circuit is not limited by the junction breakdown voltage of MOSFETs. The polysilicon diodes can be implemented in the standard CMOS processes without extra process steps. The proposed ultra-high-voltage charge pump circuit has been fabricated in a 0.25-μm 2.5-V standard CMOS process. The output voltage of the four-stage charge pump circuit with 2.5-V power-supply voltage ($\mathrm{VDD} = 2.5$ V) can be pumped up to 28.08 V, which is much higher than the n-well/p-substrate breakdown voltage ($\sim$18.9 V) in a 0.25-μm 2.5-V bulk CMOS process.**

***Index Terms*—Charge pump circuit, high-voltage generator, polysilicon diode.**

I. Introduction

CHARGE pump circuits can generate the dc voltages those are higher than the normal power-supply voltage (VDD) or lower than the ground voltage (GND). Charge pump circuits are usually applied to the nonvolatile memories, such as EEPROM and flash memories, to write or to erase the floating-gate devices [1]. Besides, charge pump circuits can be also used in some low-voltage designs to improve the circuit performance [2]. In the applications of MEMS (micro-electro-mechanical systems) and electroluminescent display, the charge pump circuit must provide the output voltage higher than 15 V, even up to 60 V [3]–[7]. Early, the p-n-junction diodes were applied in the charge pump circuit. However, it is difficult to implement the fully independent p-n-junction diodes in the common silicon substrate. The charge pump circuit realized with transistors in the diode-connected style was reported by Dickson [8], [9]. Owing to the body effect, the pump efficiency of the Dickson charge pump circuit is degraded as the number of the stages increases. Several modified charge pump circuits based on the Dickson charge pump circuit were reported to enhance the pumping efficiency [10], [11].

As the semiconductor process is scaled down, the normal circuit operation voltage (VDD) of the integrated circuits (ICs) is also decreased. The reliability issue must be considered to design the charge pump circuit in the deep-sub-micron CMOS processes, such as the gate-oxide overstress problem [11]. Fig. 1(a) shows the cross section of the $\mathrm{p+/n}$-well diode in the grounded p-substrate with the shallow-trench isolation (STI). The $\mathrm{p+/n}$-well diode is one kind of the p-n-junction diodes in the bulk CMOS process. In Fig. 1(a), an undesired parasitic p-n junction exists between the n-well and the grounded p-type substrate. If the voltage on the cathode of the $\mathrm{p+/n}$-well diode is larger than the junction breakdown voltage between the n-well and the grounded p-substrate, the charges on the cathode will leak to ground through the parasitic p-n junction. Fig. 1(b) shows the cross section of the diode-connected nMOS, whose gate and drain are connected together, in the grounded p-substrate. In Fig. 1(b), an undesired p-n junction parasitizes between the $\mathrm{n+}$ region (source/drain) and the grounded p-type substrate. Similarly, if the voltages on the cathode or anode of the diode-connected nMOS are larger than the junction breakdown voltage between the $\mathrm{n+}$ region and the grounded p-type substrate, the charges on the cathode or anode will also leak to ground through the parasitic junction. Thus, whenever the $\mathrm{p+/n}$-well (p-n junction) diodes or the diode-connected MOSFETs are used to design the charge pump circuit, the maximum output voltage will be limited by the breakdown voltage of the undesired junctions in the standard CMOS process. In the silicon-on-insulator (SOI) CMOS process, the devices are isolated to others by the insulator layer. Thus, the charge pump circuits realized in the SOI process can pump the output voltage higher without the limitation of the parasitic p-n junctions [3], [4]. However, the SOI CMOS process is more expensive than the bulk CMOS process.

In this work, an on-chip ultra-high-voltage charge pump circuit realized with the polysilicon diodes is proposed. The polysilicon diodes have been used in the negative charge pump circuit [12] and the on-chip electrostatic discharge (ESD) protection circuit [13]. Because the anode and the cathode of the polysilicon diodes are fully isolated from the silicon substrate, the voltages on the anode or the cathode of the polysilicon diodes are not limited by the breakdown voltage of the undesired parasitic p-n junction. The proposed on-chip ultra-high-voltage charge pump circuit with the polysilicon diodes has been successfully implemented and verified in a 0.25-μm 2.5-V standard (bulk) CMOS process.

II. Polysilicon Diodes

A. Device Structure of Polysilicon Diodes

The gates of pMOS and nMOS are both realized with the n-type doped polysilicon in the early standard CMOS processes.

Manuscript received September 8, 2005; revised February 25, 2006. This work was supported by National Science Council (NSC), Taiwan, R.O.C., under Contract NSC 95-2221-E-009-290. This paper was recommended by Associate Editor T. Ueta.

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Digital Object Identifier 10.1109/TCSII.2006.882854

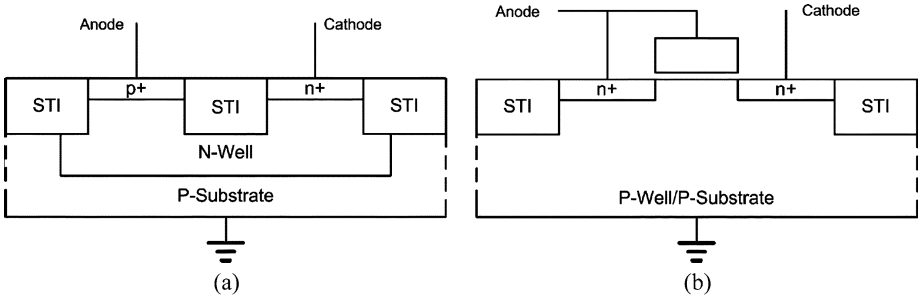

Fig. 1. Schematic cross sections of (a) the p + /n-well diode, and (b) the diode-connected nMOS, in grounded p-type substrate.

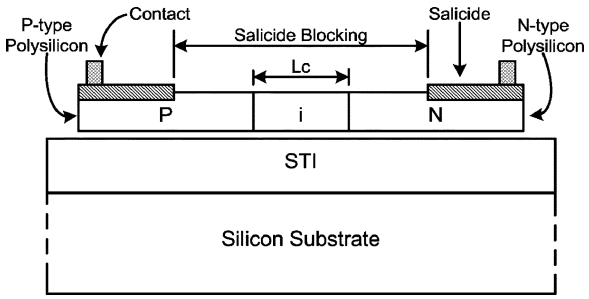

Fig. 2. Schematic cross section of the polysilicon diode in the bulk CMOS process.

Due to the work function consideration, the gate of pMOS and the gate of nMOS are realized with the p-type doped polysilicon and the n-type doped polysilicon, respectively, in the recent sub-quarter-micron standard CMOS processes. In order to implement the different types of the polysilicon gates, the intrinsic polysilicon layer is deposited first, and then the p-type and n-type impurities are doped into the intrinsic polysilicon layer to form the pMOS gate and the nMOS gate, respectively. Hence, the diode can be realized on the polysilicon layer in the recent standard CMOS processes those have separated doping impurities for pMOS and nMOS gates.

Fig. 2 depicts the cross section of the polysilicon diode in the bulk CMOS process. As shown in Fig. 2, the STI layer is located above the silicon substrate. The polysilicon layer is deposited on the STI layer. Then, the p-type and n-type highly doped regions on the polysilicon are doped with the same process step of the pMOS and nMOS source/drain ion implantation, respectively. Thus, the polysilicon diode is fully compatible to the standard CMOS process without any extra process modification. Because the polysilicon diode is implemented on the STI layer, it is isolated from the silicon substrate. The charges on the anode and the cathode of the polysilicon diode don't leak to the silicon substrate. Therefore, the polysilicon diodes can be applied to the charge pump circuit without the limitation of the parasitic junctions. In the polysilicon diode, an extra un-doped (intrinsic) polysilicon region (i) can be inserted between the p-type and n-type doped polysilicon regions. The length (Lc) of the un-doped region can be used to adjust the *I–V* characteristics of the polysilicon diode.

B. Characteristics of Polysilicon Diodes

The polysilicon diodes with different lengths (Lc) of the un-doped region have been fabricated in a 0.25-μm 2.5-V bulk CMOS process, where the Lc is changed from 0.25 to 1.5 μm. Fig. 3 shows the measured *I–V* curves of the polysilicon diodes

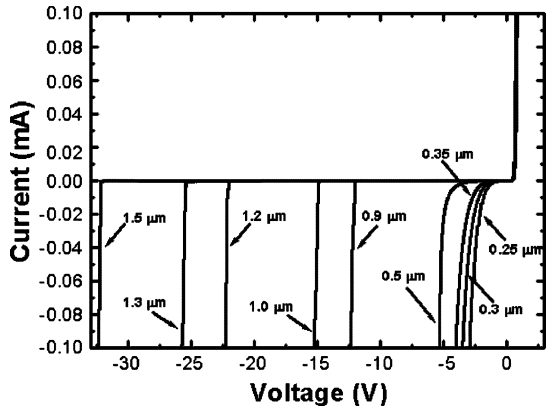

Fig. 3. Measured *I–V* curves of the polysilicon diodes with different lengths (Lc) of the un-doped region.

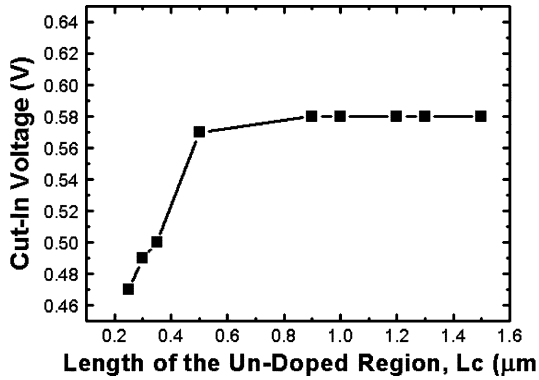

Fig. 4. Measured cut-in voltages of the polysilicon diodes with different lengths (Lc) of the un-doped region. The cut-in voltages are defined at the 1-μA forward biased current.

with different Lc. Fig. 4 shows the measured cut-in voltages of the polysilicon diodes with different Lc, where the cut-in voltages are defined at the 1-μA forward biased current. In Fig. 4, the cut-in voltages of these polysilicon diodes vary from 0.47 to 0.58 V. As the length of the un-doped region is larger than 0.9 μm, the cut-in voltage saturates at around 0.58 V.

Fig. 5 shows the measured reverse breakdown voltages and reverse leakage currents of the polysilicon diodes with different lengths (Lc) of the un-doped center region, where the reverse breakdown voltages are defined at the 1-μA reverse biased current and the reverse leakage currents are defined at the 2.5-V reverse biased voltage. In Fig. 5, the reverse breakdown voltage increases when the Lc increases. As the Lc is longer than 1.2 μm, the reverse breakdown voltage of the polysilicon diode is higher than 20 V. Moreover, the reverse breakdown voltage is

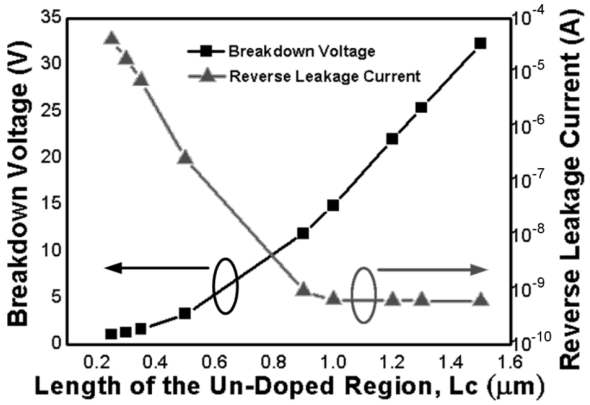

Fig. 5. Measured reverse breakdown voltages (@ 1-μA reverse biased current) and the reverse leakage currents (@ 2.5-V reverse biased voltage) of the polysilicon diodes with different lengths (Lc) of un-doped region.

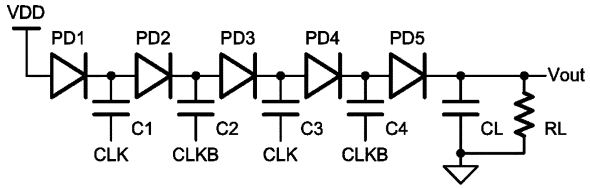

Fig. 6. Four-stage charge pump circuit realized with 5 polysilicon diodes.

33 V when the length of the un-doped region is 1.5 μm. Hence, the reverse breakdown voltage of the polysilicon diode can be adjusted by changing the length (Lc) of the un-doped center region for different applications.

III. Charge Pump Circuit With Polysilicon Diodes

A. Circuit Implementation

Fig. 6 depicts the four-stage charge pump circuit designed with 5 polysilicon diodes (PD1 $\sim$ PD5), where the clock signals, CLK and CLKB, are out-of-phase with the amplitude levels of VDD. *RL* and CL in Fig. 6 represent the output resistance and capacitance loading, respectively. A larger CL can make the output voltage of the charge pump circuit more stable. As shown in Fig. 6, the charge pump circuit uses the polysilicon diodes as the charge transfer devices. The charges are pushed from the power supply (VDD) to the output node (Vout), stage by stage, in every clock cycle. The voltage fluctuation between each stage can be expressed as

$$\Delta V = V_{\rm clk} \cdot \frac{C_{\rm pump}}{C_{\rm pump} + C_{\rm par}} - \frac{I_o}{f \cdot (C_{\rm pump} + C_{\rm par})} \qquad (1)$$

where $V_{\rm clk}$ is the voltage amplitude of the clock signals (CLK and CLKB), $C_{\rm pump}$ is the pumping capacitance (C1 $\sim$ C4), $C_{\rm par}$ is the parasitic capacitance at each pumping node, I_o is the output current, and f is the clock frequency. The output voltage of the charge pump circuit can be expressed as

$$\mathrm{Vout} = (\mathrm{VDD} - \mathrm{V_D}) + \mathrm{n} \cdot (\Delta V - \mathrm{V_D}) \qquad (2)$$

where $\mathrm{V_D}$ is the cut-in voltage of the polysilicon diode and n is the number of stages in the charge pump circuit. If $C_{\rm par}$ and I_o are small enough and $C_{\rm pump}$ is large enough, $C_{\rm par}$ and I_o can be ignored in (1). Because $V_{\rm clk}$ is usually with the same voltage level as VDD, the voltage fluctuation in each stage can be simply expressed as

$$\Delta V \approx V_{\rm clk} = \mathrm{VDD}. \qquad (3)$$

Hence, (2) can be simplified as

$$\mathrm{Vout} = (\mathrm{n}+1) \cdot (\mathrm{VDD} - \mathrm{V_D}). \qquad (4)$$

The power efficiency of the charge pump circuit is defined as [14], [15]

$$\mathrm{Efficiency} = \frac{\mathrm{Vout} \cdot Io}{\mathrm{VDD} \cdot I_{\rm VDD}}. \qquad (5)$$

In (5), $I_{\rm VDD}$ is the total current flowing from the power supply (VDD). $I_{\rm VDD}$ can be derived as [14]

$$I_{\rm VDD} = \left[(n+1) + \frac{Cpar}{C_{\rm pump}} \cdot \frac{\mathrm{n}^2 \cdot (\mathrm{VDD} - \mathrm{V_D})}{(\mathrm{n}+1) \cdot (\mathrm{VDD} - \mathrm{V_D}) - \mathrm{Vout}}\right] \cdot Io. \qquad (6)$$

The power efficiency of the charge pump circuit can be calculated from the (5) and (6).

B. Experimental Results

The four-stage, eight-stage, and 12-stage charge pump circuits with 10-pF on-chip metal-insulator-metal (MIM) pumping capacitors and the polysilicon diodes of 0.5-μm and 1-μm un-doped region have been fabricated in a 0.25-μm 2.5-V bulk CMOS process. The photograph of the four-stage charge pump circuit realized with 5 polysilicon diodes ($\mathrm{Lc} = 0.5\ \mu\mathrm{m}$) is shown in Fig. 7. The independent polysilicon diodes with different lengths of the un-doped region are also implemented in this testchip.

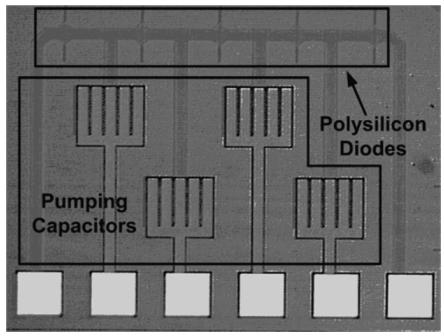

Fig. 7. Photograph of the four-stage charge pump circuit with five polysilicon diodes (Lc=0.5 μm) fabricated in a 0.25-μm 2.5-V bulk CMOS process.

Fig. 8 shows the measured waveforms of the 12-stage charge pump circuit with the polysilicon diodes ($\mathrm{Lc} = 0.5\ \mu\mathrm{m}$) to drive the capacitive output load. In Fig. 8, the power-supply voltage (VDD) and the amplitude of the clock signals (CLK and CLKB) are 2.5 V, and the clock frequency is 1 MHz. As shown in Fig. 8, the output voltage of the charge pump circuit to drive the capacitive load is as high as 28.08 V, which is much higher than the n-well/p-substrate breakdown voltage ($\sim$18.9 V) in the given 0.25-μm 2.5-V bulk CMOS process.

Fig. 9 shows the measured output voltages of the four-stage, eight-stage, and 12-stage charge pump circuits with the polysilicon diodes of 0.5-μm or 1-μm un-doped region (Lc). In Fig. 9,

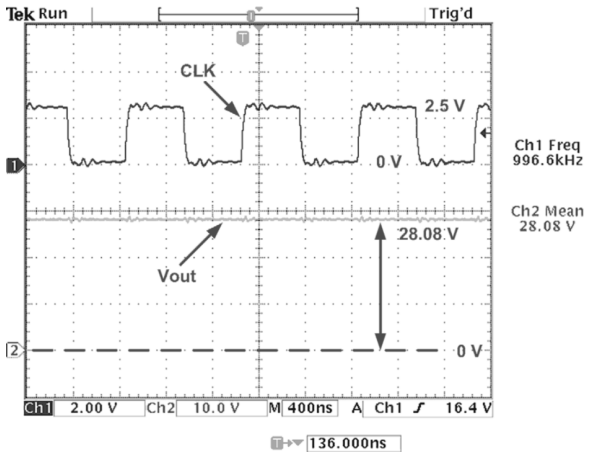

Fig. 8. Measured waveforms (CLK and Vout) of the 12-stage charge pump circuit with the polysilicon diodes ($\mathrm{Lc} = 0.5\ \mu\mathrm{m}$) to drive capacitive output load. The clock frequency is 1 MHz and VDD is 2.5 V.

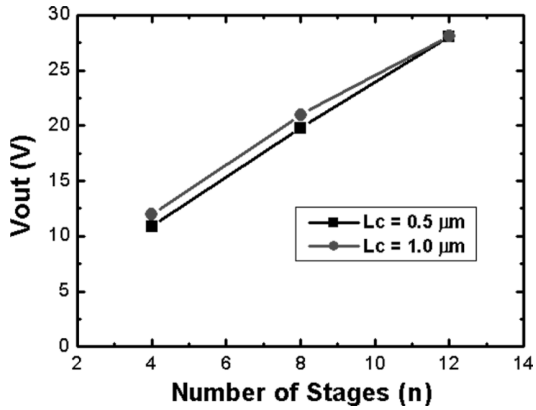

Fig. 9. Measured output voltages of the four-stage, eight-stage, and 12-stage charge pump circuits with the polysilicon diodes of 0.5-μm and 1-μm un-doped region to drive capacitive load. The clock frequency is 1 MHz and VDD is 2.5 V.

the proposed charge pump circuits drive only the capacitive loads with the clock frequency of 1 MHz and the power-supply voltage (VDD) of 2.5 V. As shown in Fig. 9, the measured output voltages of the proposed charge pump circuits with the polysilicon diodes ($\mathrm{Lc} = 0.5$ or 1 μm) are almost the same. The length of the un-doped region (Lc) doesn't obviously affect the output voltage of the proposed charge pump circuit because the voltage across each polysilicon diode doesn't exceed VDD (2.5 V), which is much smaller than the reverse breakdown voltages of the polysilicon diodes ($\mathrm{Lc} = 0.5$ or 1 μm).

Fig. 10 shows the measured output voltages of the four-stage charge pump circuit with the polysilicon diodes ($\mathrm{Lc} = 1\ \mu\mathrm{m}$) under different clock frequencies, where the power-supply voltage (VDD) is 2.5 V. When the clock frequency is increased, the output voltages of the charge pump circuit are also increased. But, when the clock frequency is low, the output voltages of the charge pump circuit are degraded, especially with a small RL. In Fig. 10, the charge pump circuit can pump the output voltage close to the ideal value in (4) when the *RL* is large and the clock frequency is high.

Fig. 11 compares the measured output voltages of the four-stage charge pump circuits with the polysilicon diodes of 0.5-μm and 1-μm un-doped region under different power-supply voltages (VDD). In Fig. 11, the charge pump circuits drive only the capacitive loads, and the clock frequency

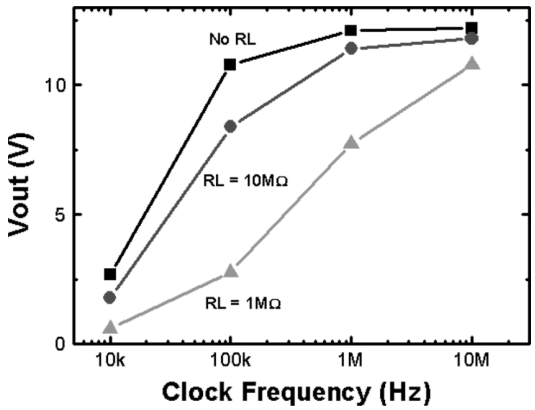

Fig. 10. Measured output voltages of the four-stage charge pump circuit ($\mathrm{Lc} = 1\ \mu\mathrm{m}$) with the output loading of 1 MΩ, 10 MΩ, or without the output resistor under different clock frequencies. The power-supply voltage (VDD) is 2.5 V.

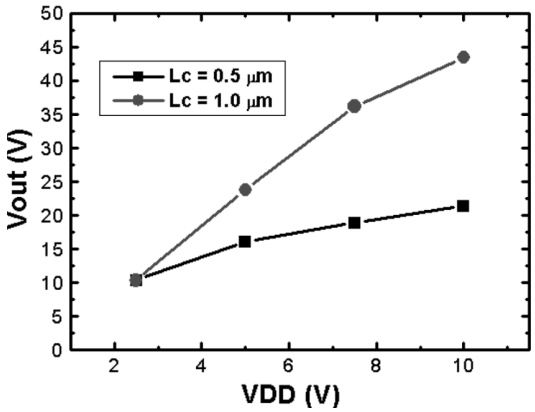

Fig. 11. Measured output voltages of the four-stage charge pump circuits with the polysilicon diodes of 0.5-μm and 1-μm un-doped region to drive capacitive loads under different VDD. The clock frequency is 100 kHz.

is 100 kHz. As shown in Fig. 11, the polysilicon diode with long length ($\mathrm{Lc} = 1\ \mu\mathrm{m}$) can generate a higher output voltage level than that with short length ($\mathrm{Lc} = 0.5\ \mu\mathrm{m}$). As the power-supply voltage (VDD) is higher than the breakdown voltage of the polysilicon diode with 0.5-μm un-doped region but still lower than that of the polysilicon diode with 1-μm un-doped region, the charge pump circuit with the polysilicon diode of 1-μm un-doped region still pumps the output voltage higher, but the output voltage of the charge pump circuit with the polysilicon diode of 0.5-μm un-doped region is degraded.

Fig. 12 shows the measured output voltage of the four-stage charge pump circuit ($\mathrm{Lc} = 1\ \mu\mathrm{m}$) with the output resistors of 1 MΩ, 10 MΩ, and without the output resistor when the clock frequency is 100 kHz. As shown in Fig. 12, the output voltage is degraded when the *RL* is small.

C. Discussion

Comparisons among the charge pump circuits realized with the polysilicon diodes (this work), p-n-junction diodes, and MOS diode (Dickson) [8] are shown in Table I. The voltage fluctuations of each stage in the charge pump circuits realized with polysilicon diodes, p-n-junction diodes, and MOS diodes (diode-connected MOSFETs) are $\mathrm{VDD} - \mathrm{V_{D-Poly}}$, $\mathrm{VDD} - \mathrm{V_{D-p-n}}$, and $\mathrm{VDD} - \mathrm{V_t}$, respectively. $\mathrm{V_{D-Poly}}$ and $\mathrm{V_{D-PN}}$ are the cut-in voltages of the polysilicon and p-n-junction diodes, respectively. $\mathrm{V_t}$ is the threshold voltage of

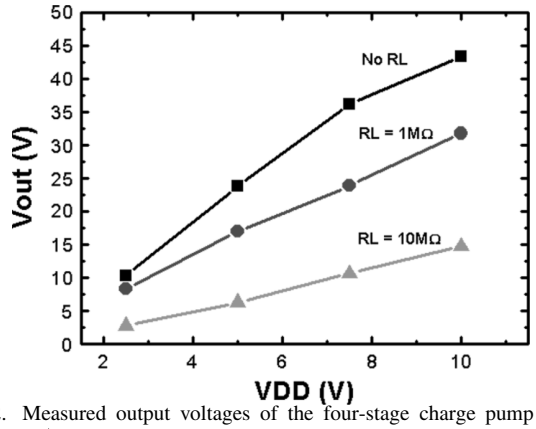

Fig. 12. Measured output voltages of the four-stage charge pump circuits ($\mathrm{Lc} = 1\ \mu\mathrm{m}$) with the output resistors of 1 and 10 MΩ and without the output resistor under different VDD. The clock frequency is 100 kHz.

TABLE I
COMPARISONS AMONG CHARGE PUMP CIRCUITS REALIZED WITH POLYSILICON DIODES (THIS WORK), P-N-JUNCTION DIODES AND MOS DIODES

	Voltage Fluctuation	Power Efficiency	Layout Area	Maximum Output Voltage*
Polysilicon diode	VDD-$V_{D\text{-}Poly}$	Better	Same	>43 V
pn-junction diode	VDD-$V_{D\text{-}PN}$	Good	Same	<18.9 V
MOS diode	VDD-V_t	Good	Same	<7.4 V

*In the given 0.25-μm bulk CMOS process.

the MOS device. However, $\mathrm{V_t}$ increases due to the body effect while the number of pumping stages increases. The differences of power efficiencies among the charge pump circuits realized with polysilicon diodes, p-n-junction diodes, and MOS diodes mainly depend on the parasitic capacitance $(C\mathrm{par})$ at each stage, if the charge pump circuits are realized with the same number (n) of stages, the same pumping capacitance $(C\mathrm{pump})$, and the same clock frequency (f) [15]. The parasitic capacitance of the polysilicon diode formed on the STI layer has been studied in [13], which is smaller than those of p-n-junction diode and MOS diode. Thus, the power efficiency of the chare pump circuit realized by polysilicon diodes is better than that of the charge pump circuit realized by p-n-junction diodes or MOS diodes. The area of the charge pump circuit is dominated by the on-chip pumping capacitors, so these three kinds of the charge pump circuits occupy almost the same chip area under the same pumping capacitors and the same number (n) of the stages. As described in the previous section, the output voltage of the charge pump circuit realized with p-n-junction diodes is limited by the breakdown voltage (∼18.9 V) of the parasitic n-well/p-substrate junction, and that of the charge pump circuit realized with MOS Diodes is limited by the breakdown voltage (∼7.4 V) of the parasitic $\mathrm{n+/p}$-substrate junction in the given 0.25-μm bulk CMOS process. However, the output voltage of the charge pump circuit realized with polysilicon diodes isn't limited by the breakdown voltages of the parasitic p-n junctions. As shown in Fig. 12, the output voltage of the charge pump circuit realized with the polysilicon diodes to drive the capacitive load can be up to ∼43 V.

IV. CONCLUSION

An ultra-high-voltage charge pump circuit realized with the polysilicon diodes has been successfully verified in a 0.25-μm 2.5-V bulk CMOS process. The polysilicon diodes are implemented on the STI layer, which are fully isolated from the silicon substrate. Therefore, the maximum output voltage of the proposed charge pump circuit with the polysilicon diodes isn't limited by the breakdown voltages of the parasitic p-n junctions. In addition, the polysilicon diodes are fully compatible to the bulk CMOS processes without any extra process modification. The four-stage, eight-stage, and 12-stage charge pump circuits with 10-pF on-chip pumping capacitors and the polysilicon diodes of 0.5-μm and 1-μm un-doped center region have been fabricated in a 0.25-μm 2.5-V bulk CMOS process. To drive the capacitive load, the measured results show that the four-stage charge pump circuit with the polysilicon diodes ($\mathrm{Lc} = 0.5\ \mu\mathrm{m}$) can pump the output voltage as high as 28.08 V, whereas the power-supply voltage (VDD) is 2.5 V. The output loading effect and the dependence of clock frequency on the output voltage of the proposed charge pump circuit have been also measured.

REFERENCES

[1] T. Tanzawa, Y. Takano, K. Watanabe, and S. Atsumi, "High-voltage transistor scaling circuit techniques for high-density negative-gate channel-erasing NOR flash memory," *IEEE J. Solid-State Circuits*, vol. 37, no. 10, pp. 1318–1325, Oct. 2002.

[2] J.-S. Wang, H.-Y. Li, C. Yeh, and T.-F. Chen, "Design technique for single-low-VDD CMOS Systems," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1157–1165, May 2005.

[3] M. R. Hoque, T. McNutt, J. Zhang, A. Mantooth, and M. Mojarradi, "A high voltage Dickson charge pump in SOI CMOS," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2003, pp. 493–496.

[4] M. R. Hoque, T. Ahmad, T. McNutt, A. Mantooth, and M. Mojarradi, "Design technique of an on-chip, high-voltage charge pump in SOI," in *Proc. IEEE Symp. Circuits Syst.*, 2005, pp. 133–136.

[5] M. R. Hoque, T. Ahmad, T. R. McNutt, H. A. Mantooth, and M. M. Mojarradi, "A technique to increase the efficiency of high-voltage charge pumps," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 5, pp. 364–368, May 2006.

[6] J. De Vos, H. De Smet, A. M. De Cubber, and A. Van Calster, "High-voltage CdSe-Ge TFT driver circuits for passive AC-TFEL Displays," *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 228–232, Feb. 1999.

[7] K. Muhlemann, "A 30-V row/column driver for flat-panel liquid crystal displays," *IEEE J. Solid-State Circuits*, vol. 23, no. 4, pp. 442–449, Apr. 1988.

[8] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. SC-11, no. 3, pp. 374–378, Jun. 1976.

[9] G. Palumbo and D. Pappalardo, "Charge pump circuits with only capacitive loads," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 2, pp. 128–132, Feb. 2006.

[10] J.-T. Wu and K.-L. Chang, "MOS charge pump for low-voltage operation," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 592–597, Apr. 1998.

[11] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage process," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1100–1107, May 2006.

[12] M.-D. Ker, C.-Y. Chang, and H.-C. Jiang, "Design of negative charge pump circuit with polysilicon diodes in a 0.25-μm CMOS process," in *Proc. IEEE Asia-Pacific Conf. Advanced Syst. Integr. Circuits*, 2002, pp. 145–148.

[13] Y.-D. Shiu, C.-H. Chunag, and M.-D. Ker, "Investigation on RF characteristics of stacked P-I-N polyslilcon diodes for ESD protection design in 0.18-μm CMOS technology," in *Proc. IEEE Int. Symp. VLSI Technol. Syst. Appl.*, 2006, pp. 56–57.

[14] G. Palumbo, D. Pappalardo, and M. Gaibotti, "Charge-pump circuits: power-consumption optimization," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 11, pp. 1535–1542, Nov. 2002.

[15] D. Baderna, A. Cabrini, G. Torelli, and M. Pasotti, "Efficiency comparison between doubler and Dickson charge pumps," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2005, pp. 1891–1894.