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Performance Enhancement of the nMOSFET Low-Noise Amplifier by Package Strain

W.-C. Hua, H.-L. Chang, T. Wang, C.-Y. Lin, C.-P. Lin, S. S. Lu, C. C. Meng, and C. W. Liu

***Abstract*—The package strain improves the noise figure (NF) of the low-noise amplifier (LNA). The maximum noise reduction is ∼0.53 dB (13%) at the operating frequency of 2.4 GHz under the biaxial tensile strain of 0.037%. The NF reduction of the strained LNA is mainly due to the enhanced transconductance and cutoff frequency of the individual nMOSFET device under the same strain and bias conditions.**

***Index Terms*—Biaxial strain, cutoff frequency, low-noise amplifier (LNA), noise factor, noise figure (NF), package strain, tensile, transconductance.**

I. Introduction

The strained-Si technology has attracted great attention due to the enhancement of the carrier mobility. There are three methods to obtain the strain in the Si channel of the MOSFET device, namely 1) substrate strain [1]–[4], 2) process strain [5]–[8], and 3) mechanical strain/package strain [9]–[12]. The shortages of the substrate strained-Si are high defect density, thermal budget limitation, and higher fabrication cost. Although the process strain technology can improve the current drive and mobility of both nMOSFET and pMOSFET devices with the advantage of simplicity and low cost, it can only be applied to very short-channel devices ($L_g < \sim 50$ nm). However, the package strain has the flexibility to apply the uniaxial or biaxial strain to the devices with different channel lengths. Package strain can be also applied to the circuits that already have built-in strain to further increase the circuit performance by the strain addition. The low cost, flexibility, and modular properties of the package strain make it attractive for future production. The performance enhancement of the strained-Si is proven not only at the transistor level but also at the circuit level. The performance enhancement of ring oscillators and transimpedance amplifiers by package strain has been reported previously [12].

In this brief, the noise figure (NF) reduction of the 0.35-μm nMOSFET low-noise amplifier (LNA) by external package strain is reported, and the theoretical analysis is also given to study the NF reduction.

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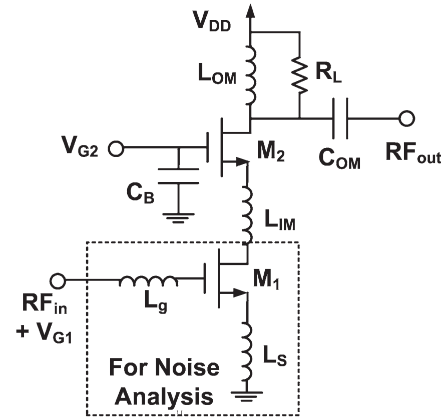

Fig. 1. Schematic of the LNA circuit and the circuit block for the noise analysis.

II. LNA Design

Fig. 1 shows the schematic of the LNA circuit. The designed central frequency of the LNA is 2.4 GHz. The geometries ($L \times W \times$ finger) of the nMOSFET devices in the LNA circuit are 0.35 μm × 20 μm × 8 and 0.35 μm × 20 μm × 4 for M1 and M2, respectively. The LNA consists of a common-source input stage cascaded with a common-gate (CG) output stage. The inductor $L_{\rm IM}$ is the interstage matching inductor.

III. Results and Discussion

The noise factor F of a cascaded two-stage LNA is given by [13]

$$F = F_1 + \frac{F_2 - 1}{G_1} \approx F_1 \tag{1}$$

where F_1, F_2, and G_1 denote the noise factor of the first stage, the noise factor of the second stage, and the gain of the first stage, respectively. The total noise factor is mainly determined by F_1 if G_1 is large enough.

Thus, the noise analysis of the LNA can be simplified to the circuit block of M1 with L_g and L_s (dashed block in Fig. 1). The noise factor of such LNA topology is given by [14]

$$F = 1 + \frac{R_g}{R_s} + \frac{R_l}{R_s} + \gamma\chi g_{d0} R_S \left(\frac{f_0}{f_T}\right)^2 \tag{2}$$

where R_s, R_g, and R_l are the source resistance (50 Ω), the gate resistance, and the parasitic resistance of L_g, respectively. γ, χ, g_{d0}, f_0, and f_T are the fitting parameter of the channel thermal noise, the scaling factor of the drain current noise, the zero-bias drain conductance of

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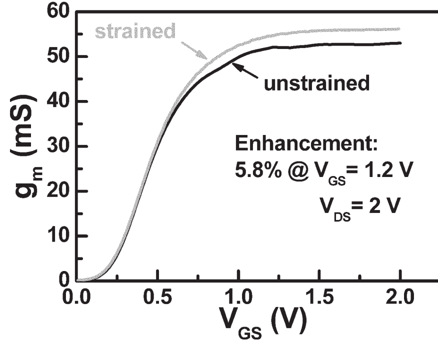

Fig. 2. Measured g_m versus V_{GS} of the individual device with the same size as M1 for the strained and unstrained conditions. The enhancement of g_m is ∼5.8% under the biaxial tensile strain of 0.037%.

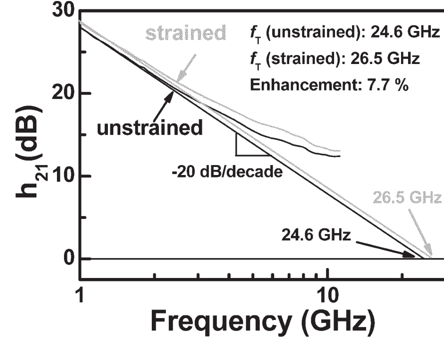

Fig. 3. Measured f_T of the device with the same size as M1 for the strained and unstrained conditions. The enhancement of f_T is ∼7.7% under the biaxial tensile strain of 0.037%.

M1, the operating frequency, and the cutoff frequency of M1. Since $\alpha = g_m/g_{d0}$ [14], the total noise factor can be simplified to

$$F = 1 + \frac{R_g}{R_s} + \frac{R_l}{R_s} + \frac{g_m}{f_T^2}A \tag{3}$$

by assuming $A = \gamma\chi R_s f_0^2/\alpha$. The transconductance (g_m) proportionality of the last term in (3) is due to the proportionality of the channel thermal noise to g_m, and the inverse f_T^2 of the last term in (3) is due to the referring of the drain current noise to the gate.

To calculate the noise factor reduction (ΔF) and NF reduction (ΔNF) of the LNA under package strain, we assume that A and the resistances R_s, R_g, and R_l remain unchanged under package strain. Since the last term in (3) is the most significant term [14], ΔF and ΔNF can be expressed as

$$\begin{aligned}\Delta F &= \frac{F - F_S}{F} \\ &= \frac{\frac{g_m}{f_T^2}A\left[1 - \frac{g_{m,S}}{g_m}\left(\frac{f_T}{f_{T,S}}\right)^2\right]}{F} \\ &\approx \frac{(F-1)\left[1 - \frac{g_{m,S}}{g_m}\left(\frac{f_T}{f_{T,S}}\right)^2\right]}{F}\end{aligned} \tag{4}$$

$$\begin{aligned}\Delta \mathrm{NF} &= \mathrm{NF} - \mathrm{NF}_S \\ &= 10\log F - 10\log F_S = 10\log(1-\Delta F) \\ &\approx 10\log\left\{1 - \frac{(F-1)\left[1 - \frac{g_{m,S}}{g_m}\left(\frac{f_T}{f_{T,S}}\right)^2\right]}{F}\right\}\end{aligned} \tag{5}$$

respectively. The parameters with a subscript of S are the values under package strain.

The package strain conditions for all the experiments in this brief are biaxial tensile strain of 0.037%. All the measurements for both LNA circuit and nMOSFET device under strained and unstrained conditions are on-wafer measurements without package bondwires. The chip of the LNA circuit is tightly glued to the Si wafer, which serves as the package substrate. The mechanical stress is applied to the package substrate, and the chip is stressed via the glue between the chip and the package substrate. The details of the strain mechanism can be found in the previous work [12]. More than ten samples have been characterized to ensure the repeatability of the performance enhancements of the LNA and nMOSFET device under package strain. The results of the typical samples are presented in this brief.

Fig. 2 shows the measured g_m versus gate–source voltage (V_{GS}) of the individual device with the same size as M1 for both strained and unstrained conditions. The measured g_m under strained and unstrained conditions at V_{GS} of 1.2 V and at drain voltage of 2 V are 54.8 and 51.8 mS, respectively. The enhancement of g_m is ∼5.8% at the same bias as M1 in Fig. 1. Fig. 3 shows the f_T of the individual device for both strained and unstrained conditions. The extrapolated f_T (−20 dB/dec) from the h_{21} data under strained and unstrained conditions are 26.5 and 24.6 GHz, respectively. The enhancement of f_T is ∼7.7% under the same strain and bias conditions as M1 in Fig. 1.

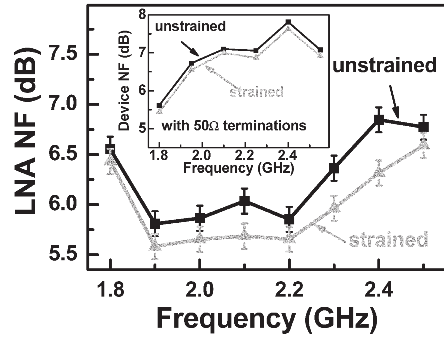

Fig. 4. Measured NF of the LNA circuit and the nMOSFET device under both strained and unstrained conditions. The inset shows the NF of the device with 50-Ω source and load terminations.

Fig. 4 shows the measured NF of the LNA circuit and the nMOSFET device under both strained and unstrained conditions. The inset of Fig. 4 shows the NF of the device with 50-Ω source and load terminations. The ΔNF of the strained device is about 0.2–0.3 dB as compared to the unstrained device. The NF of the device is larger than the NF of the LNA due to the nonoptimized source impedance. The statistical results of the LNA NF in Fig. 4 are obtained from 20 measurements of the same sample. The error bars stand for the standard deviation of the NF data, which result from the measurement error. The NF of the LNA at 2.4 GHz in this brief is relatively larger than the NF of the LNA in 0.35-μm CMOS device technology reported in the literatures (3.7–5.3 dB) [15]–[17]. The maximum ΔNF is 0.53 dB, which is equivalent to the ΔF of 13% at 2.4 GHz. The calculated ΔNF based on (5) are from 0.29 to 0.33 dB, whereas the measured ΔNF vary from 0.18 to 0.53 dB (1.8–2.5 GHz). The calculation agrees qualitatively with the experimental data, but there is a quantitative discrepancy between the analytical value and the experimental data. This discrepancy is probably due to the negligence of the noise contribution of the second CG stage since gain G_1 is not sufficiently large.

IV. Conclusion

The performance enhancement of the 0.35-μm nMOSFET LNA circuit is achieved by the external package strain. Due to the enhanced

g_m and f_T of the nMOSFET device under biaxial tensile strain, the NF (noise factor) of the LNA can be reduced to as high as 0.53 dB (13%) at 2.4 GHz. Theoretical analysis of the NF reduction based on the enhanced g_m and f_T is also proposed to study the noise reduction. The performance enhancement under biaxial tensile strain is expected for the LNA with the same topology despite of the technology node of the device.

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Analytical Charge and Capacitance Models of Undoped Cylindrical Surrounding-Gate MOSFETs

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***Abstract*—We present an analytical and continuous charge model for cylindrical undoped surrounding-gate MOSFETs, from which analytical expressions of all total capacitances are obtained. The model is based on a unified charge control model derived from Poisson equation. The drain current, charge, and capacitances are written as continuous explicit functions of the applied voltages. The calculated capacitance characteristics show excellent agreement with three-dimensional numerical device simulations.**

***Index Terms*—Compact device modelling, intrinsic capacitances, surrounding-gate (SGT) MOSFET.**

I. Introduction

The surrounding-gate (SGT) MOSFET is one of the most promising candidates for the downscale of CMOS technology toward the nanometer-channel-length range since the SGT architecture allows excellent control of the channel charge in the silicon film, reducing short-channel effects [1]–[5].

Compact models for SGT MOSFETs, which are adequate for circuit simulators, are necessary for the future use of these devices in integrated circuits. Circuit design requires a complete small-signal model, which consists of analytical expressions of transconductance and conductance (derived from a drain current expression) and also of the total capacitances.

In a previous work [6], a channel-current model, which is written in terms of the charge densities at the source and drain ends, was developed from a unified charge control model derived from the solution of one-dimensional (1-D) Poisson equation. In this brief, we present the development of analytical charge and capacitance models obtained from the unified charge control model. This results in a complete charge-based small-signal model. The charge and capacitance expressions are written in terms of explicit and infinitely continuous

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