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Introductory Invited Paper

Overview on ESD protection design for mixed-voltage I/O interfaces with high-voltage-tolerant power-rail ESD clamp circuits in low-voltage thin-oxide CMOS technology ☆

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Abstract

Electrostatic discharge (ESD) protection design for mixed-voltage I/O interfaces has been one of the key challenges of system-on-a-chip (SOC) implementation in nanoscale CMOS processes. The on-chip ESD protection circuit for mixed-voltage I/O interfaces should meet the gate-oxide reliability constraints and prevent the undesired leakage current paths. This paper presents an overview on the design concept and circuit implementations of ESD protection designs for mixed-voltage I/O interfaces with only low-voltage thin-oxide CMOS transistors. Especially, the ESD protection designs for mixed-voltage I/O interfaces with ESD bus and high-voltage-tolerant power-rail ESD clamp circuits are presented and discussed.

1. Introduction

With the scaled-down device dimension in advanced CMOS technology, the power supply voltage is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. However, most microelectronic systems nowadays consist of mixed semiconductor chips fabricated in different CMOS technologies, where the interfaces between semiconductor chips or sub-systems have different internal power supply voltages. For example, a 3.3 V I/O interface is generally required by the ICs realized in CMOS processes with the internal power-supply voltage of 2.5 V or 1.8 V. The traditional CMOS I/O buffer with V_{DD} of 2.5 V is shown in Fig. 1(a) with both output and input stages. When an external 3.3 V signal is applied to the I/O pad, the channel of the output PMOS (M_{p_out}) and the parasitic drain-to-well junction diode in the M_{p_out} cause the leakage current paths from the I/O pad to V_{DD}, as the dashed lines shown in Fig. 1(a). Moreover, the gate oxides of the output NMOS (M_{n_out}), the gate-grounded NMOS (M_{n1}) for input electrostatic discharge (ESD) protection, and the input inverter stage are over stressed by the 3.3 V input signal to suffer the gate-oxide reliability issue [1].

To avoid the leakage current paths from I/O pad to V_{DD}, the gate tracking circuit and the n-well self-biased circuit are designed to ensure that the pull-up PMOS (M_{p_mix}) will not conduct the leakage current. To solve the gate-oxide reliability issue without using the additional thick gate-oxide process, the stacked-MOS configuration has been widely used in the mixed-voltage I/O circuits [2–4]. The typical 2.5 V/3.3 V tolerant mixed-voltage I/O circuit is shown in Fig. 1(b) [2]. With a high-voltage input signal at the pad (e.g. 3.3 V in a 2.5 V/3.3 V mixed-voltage I/O interface), the common node between the M_{n_top} and M_{n_bot} in the stacked-NMOS structure has approximately a voltage level of $V_{DD} - V_{th}$ (~1.9 V), where V_{th} (~0.6 V) is the threshold voltage of NMOS device. Therefore, the independent control on the top and bottom gates

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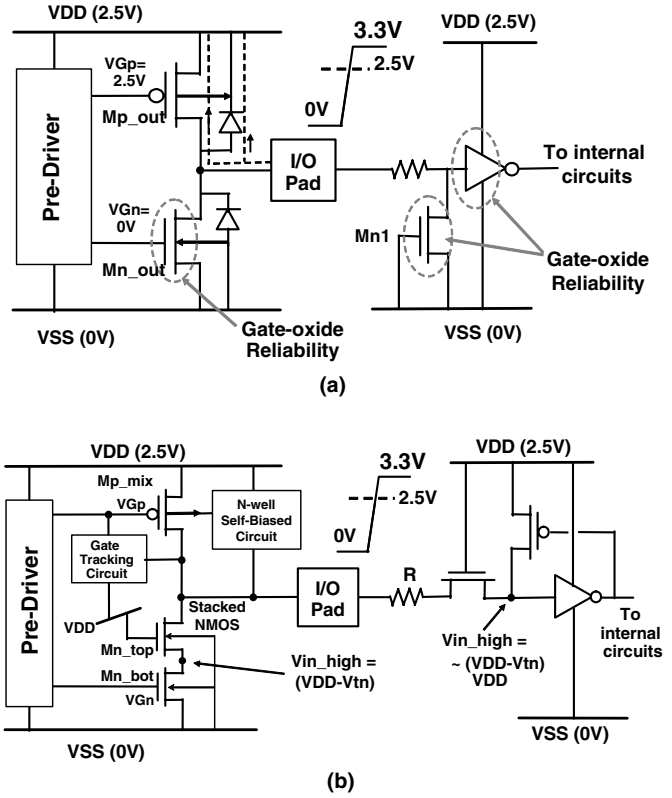

Fig. 1. Typical circuit diagrams for (a) the traditional CMOS I/O buffer, and (b) the mixed-voltage I/O circuits with the stacked-NMOS and the n-well self-biased PMOS.

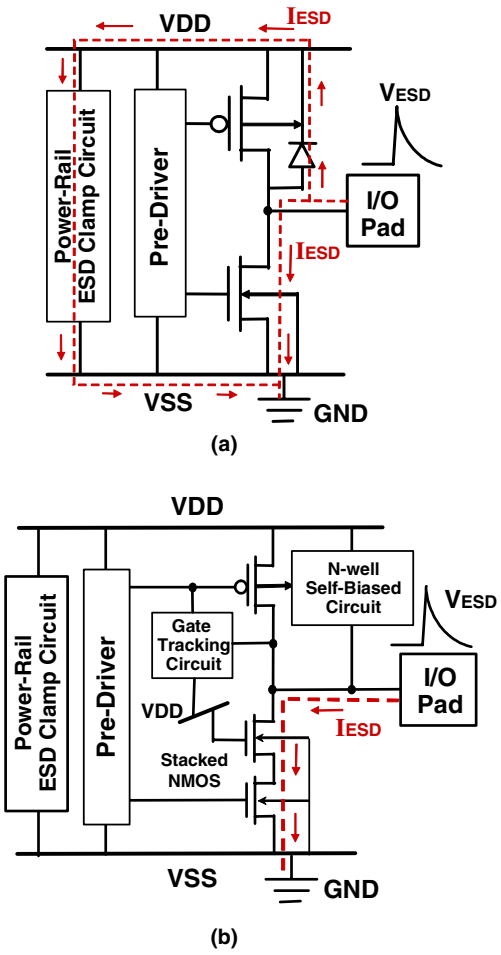

Fig. 2. The ESD current paths of (a) the traditional I/O pad with power-rail ESD clamp circuit, and (b) the mixed-voltage I/O pad with power-rail ESD clamp circuit, under the PS-mode ESD stress.

of the stacked-NMOS allows the devices to be operated within the safe range for both dielectric and hot-carrier reliability limitations during normal circuit operation. In such mixed-voltage I/O circuits, the on-chip ESD protection circuits will meet more design constraints and difficulty.

In this paper, an overview on ESD protection designs for mixed-voltage I/O interface circuits without using the additional thick gate-oxide process is presented. The content covers the ESD design constraints in mixed-voltage I/O circuits, the classification, and analysis of the ESD protection designs for mixed-voltage I/O circuits. Especially, the ESD protection designs for mixed-voltage I/O interfaces with ESD bus and high-voltage-tolerant power-rail ESD clamp circuits are presented and discussed.

2. ESD design constraints in mixed-voltage I/O circuits

ESD stresses on an I/O pad have four pin-combination modes: positive-to-V_{SS} (PS-mode), negative-to-V_{SS} (NS-mode), positive-to-V_{DD} (PD-mode), and negative-to-V_{DD} (ND-mode) stresses. The ESD protection design of I/O pad cooperating with power-rail ESD clamp circuit is shown in Fig. 2(a), where a PS-mode ESD pulse is applied to the I/O pad. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of PMOS from I/O pad to V_{DD}, and then through the V_{DD}-to-V_{SS} ESD clamp circuit to ground. The traditional I/O circuits cooperating with the V_{DD}-to-V_{SS} ESD clamp circuit can achieve a much higher ESD level [5]. But, due to the leakage current issue in the mixed-voltage I/O circuits, there is no diode connected from the I/O pad to V_{DD} power line. The ESD current at mixed-voltage I/O pad under PS-mode ESD stress cannot be discharged from the I/O pad to V_{DD} power line, and cannot be discharged through the additional V_{DD}-to-V_{SS} ESD clamp circuit. Therefore, the power-rail ESD clamp circuit did not help to pull up ESD level of the mixed-voltage I/O pad under the PS-mode ESD stress. Such ESD current at the mixed-voltage I/O pad is mainly discharged through the stacked-NMOS by snapback breakdown, as illustrated in Fig. 2(b). However, the NMOS in stacked configuration has a higher trigger voltage and a higher snapback holding voltage, but a lower secondary breakdown current (I_{t2}), as compared to that of the single NMOS [6,7]. Therefore, such mixed-voltage I/O circuits with stacked-NMOS often have a lower ESD level under PS-mode ESD stress, as compared to the traditional I/O circuits with a single NMOS [6]. In addition, without the diode connected from the I/O pad to V_{DD}, the mixed-voltage I/O circuit also has

a lower ESD level for I/O pad under PD-mode ESD stress.

Although the ESD robustness of stacked-NMOS device can be somewhat improved by layout optimization, the stacked-NMOS device by snapback breakdown still cannot provide efficient ESD protection in the mixed-voltage I/O circuits. By using extra process modification such as ESD implantation [8], the ESD robustness of stacked-NMOS device can be further improved [9], but the process complexity and fabrication cost are increased. Therefore, effective ESD protection design without increasing process complexity is strongly requested by the mixed-voltage I/O circuits in the scaled-down CMOS processes.

3. ESD protection designs for mixed-voltage I/O circuits

3.1. Substrate-triggered stacked-NMOS device

The snapback operation of the parasitic n–p–n BJT in the stacked-NMOS structure can be controlled by its substrate potential. The substrate-triggered technique [10] can be used to generate the substrate current (I_{sub}) in ESD protection circuits. With the substrate-triggered current (I_{trig}), the trigger voltage of the stacked-NMOS device in mixed-voltage I/O circuits can be reduced for more effective ESD protection.

The finger-type layout pattern and the corresponding cross-sectional view of the substrate-triggered stacked-NMOS device are shown in Fig. 3(a) and (b), respectively. As shown in the layout top view, an additional p+ diffusion is inserted into the center drain region of stacked-NMOS device as the substrate-triggered node. The trigger current is provided by the substrate-triggered circuit. An n-well structure is further diffused under the source region, which is also surrounding the whole device, to form a higher equivalent substrate resistance (R_{sub}) for improving turn-on efficiency of the parasitic lateral BJT in the stacked-NMOS device. The substrate-triggered circuit should be designed to avoid electrical overstress on the gate oxide and to prevent the undesired leakage current paths during normal circuit operating condition. During ESD stress condition, the substrate-triggered circuit should generate large enough trigger current to effectively improve the turn-on efficiency of parasitic n–p–n BJT in stacked-NMOS device.

The substrate-triggered circuit I for stacked-NMOS device in the mixed-voltage I/O circuits is shown in Fig. 4 [11]. The substrate-triggered circuit I is composed of the diode string, a PMOS M_{p1}, and an NMOS M_{n1}, to provide the substrate current for triggering on the parasitic n–p–n BJT in the stacked-NMOS device during ESD stress. Under normal circuit operating condition, the turn-on voltage of the substrate-triggered circuit roughly equals to $V_{pad} \geqq V_{string}(I) + |V_{tp}| + V_{DD}$, where $V_{string}(I)$ is the total voltage drop across the diodes and V_{tp} is the threshold voltage of the PMOS. To satisfy the requirement in the 2.5 V/3.3 V mixed-voltage application, the number of the diodes in the diode string should be adjusted to make

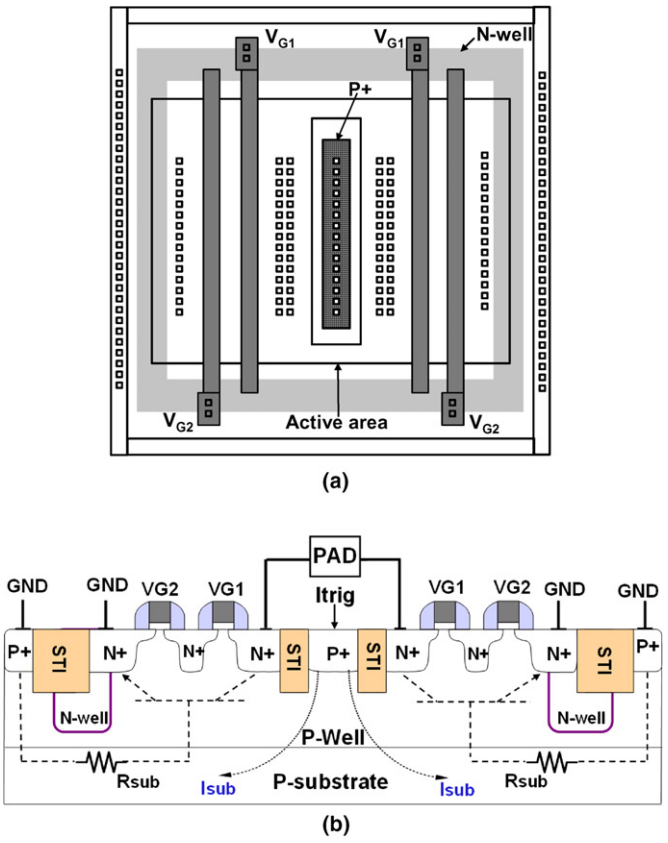

Fig. 3. (a) Finger-type layout pattern, and (b) the corresponding cross-sectional view, of the substrate-triggered stacked-NMOS device for mixed-voltage I/O circuits.

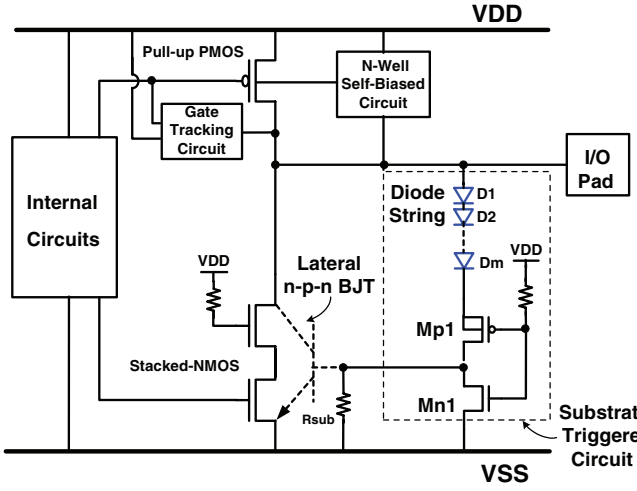

Fig. 4. Schematic circuit diagram of the substrate-triggered stacked-NMOS device with substrate-triggered circuit I for the mixed-voltage I/O circuits.

the turn-on voltage greater than 3.3 V. When a 3.3 V input voltage is applied at I/O pad, M_{p1} is kept off, and the local substrate of the stacked NMOS is biased at V_{SS} by the turned-on M_{n1}. With the diode string to block the 3.3 V input voltage at the I/O pad, the M_{p1} with thin gate oxide

has no gate-oxide reliability issue under normal circuit operating condition. The M_{p1} in conjunction with the diode string is used to reduce the leakage current through the substrate-triggered circuit in normal operating condition. If a lower input leakage is desired, the numbers of the diodes in the diode string should be increased. Under PS-mode ESD stress condition, the gate of the M_{p1} has an initial voltage level of $\sim$0 V, while the V_{SS} pin is grounded but the V_{DD} pin is floating. The substrate-triggered circuit will provide the trigger current flowing through the diode string and the M_{p1} into the p-substrate, when $V_{pad} \geqq V_{string}(I) + |V_{tp}|$. The trigger current provided by the substrate-triggered circuit is determined by the diode string and the size of M_{p1}. Once the parasitic n–p–n BJT in the stacked-NMOS device is triggered on, the ESD current will be discharged from the I/O pad to V_{SS}.

Another substrate-triggered circuit II for stacked-NMOS device in the mixed-voltage I/O circuits is shown in Fig. 5 [12]. The substrate-triggered circuit II is composed of the PMOS M_{p1}, PMOS M_{p2}, NMOS M_{n1}, and NMOS M_{n2}, to provide the substrate current for triggering on the parasitic n–p–n BJT in the stacked-NMOS device during ESD stress. In the 2.5 V/3.3 V mixed-voltage IC application, the gates of M_{p1} and M_{p2} are biased at 2.5 V V_{DD} supply through a resistor R_d under normal circuit operating condition. When the input voltage transfers from 0 V to 3.3 V at the I/O pad, the gate voltage of M_{n1} could be increased through the coupling capacitor C. However, the M_{n2} and M_{p2} can clamp the gate voltage of M_{n1} between $V_{DD} - V_{tn}$ and $V_{DD} + |V_{tp}|$, where V_{tn} is the threshold voltage of NMOS. Once the gate voltage of M_{n1} is over $V_{DD} + |V_{tp}|$, the M_{p2} will turn on to discharge the over-coupled voltage and to keep the gate voltage within $V_{DD} + |V_{tp}|$. Since the upper boundary on the gate voltage of M_{n1} is within $V_{DD} + |V_{tp}|$, the source voltage of M_{p1} is clamping below V_{DD}, which keeps the M_{p1} always off under normal circuit operation condition. The M_{n2} and M_{p2} can further clamp the gate voltage of M_{n1} to avoid gate-oxide reliability issue in the substrate-triggered circuit, even if the I/O pad has a high input voltage level. Under PS-mode ESD-stress condition, the gates of M_{p1} and M_{p2} have an initial voltage level of $\sim$0 V, while the V_{SS} pin is grounded but the V_{DD} pin is floating. The positive ESD transient voltage on the I/O pad is coupled through the capacitor C to the gate of M_{n1}. In this situation, both of the M_{n1} and M_{p1} are operated in the turned-on state. Therefore, the substrate-triggered circuit II will conduct some ESD current flowing from I/O pad through M_{n1} and M_{p1} into the p-substrate. The trigger current provided by the substrate-triggered circuit II is determined by the size of M_{n1}, M_{p1}, and the capacitor C. Once the parasitic n–p–n BJT in the stacked-NMOS device is triggered on, the ESD current can be mainly discharged from the I/O pad to V_{SS}.

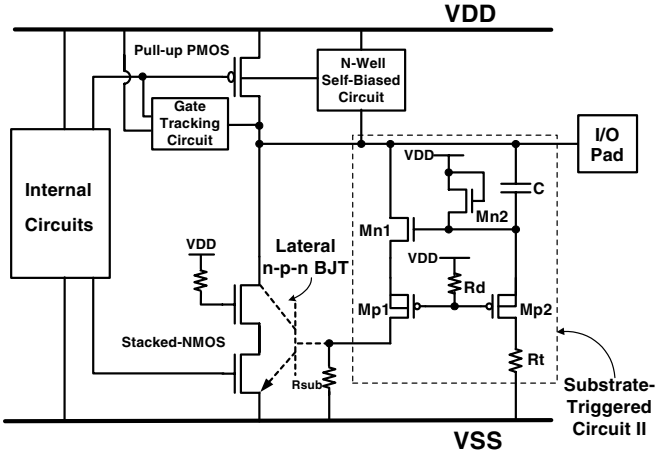

Fig. 5. Schematic circuit diagram of the substrate-triggered stacked-NMOS device with substrate-triggered circuit II for the mixed-voltage I/O circuits.

Both two substrate-triggered designs can significantly reduce the trigger voltage and ensure effective ESD protection for the mixed-voltage I/O circuits. By using such substrate-triggered designs, the gates of stacked-NMOS in the mixed-voltage I/O circuits can be fully controlled by the pre-driver of I/O circuits without conflict to the ESD protection circuits. The main ESD discharge device is the parasitic n–p–n BJT in the stacked-NMOS device. Therefore, the ESD robustness of mixed-voltage I/O circuits can be effectively improved without occupying extra silicon area to realize the additional stand-alone ESD protection device into the mixed-voltage I/O cells.

3.2. Extra ESD device between I/O pad and V_{SS}

To improve ESD level of the mixed-voltage I/O circuits, the extra ESD device was added between I/O pad and V_{SS} power line. The ESD protection design, by using the additional stacked-NMOS triggered silicon controlled rectifier (SNTSCR) [13], has been reported to protect the mixed-voltage I/O circuits. The ESD protection design with the additional SNTSCR device for protecting the mixed-voltage I/O circuits is shown in Fig. 6(a). The device structure of SNTSCR and the corresponding ESD detection circuit are shown in Fig. 6(b). The ESD detection circuit, designed by using the gate-coupled technique with consideration of the gate-oxide reliability issue, is used to provide suitable gate bias to trigger on the SNTSCR device under ESD stress condition. On the contrary, this ESD detection circuit must keep the SNTSCR off when the IC is under normal circuit operating condition. During normal circuit operating condition, the M_{n3} in Fig. 6(b) acts as a resistor to bias the gate voltage (V_{g1}) of M_{n1} at V_{DD}. But, the gate of M_{n2} is grounded through the resistor $R2$ and M_{n4}. So, all the devices in the ESD protection circuit can meet the electrical-field constraint of gate-oxide reliability under normal circuit operating condition. Under PS-mode ESD stress condition, the M_{p1} is turned on but M_{n3} is off since the initial voltage level on the floating V_{DD} line is $\sim$0 V. The capacitors $C1$ and $C2$ are designed to couple ESD transient voltage from the I/O pad to the gates of M_{n1} and M_{n2},

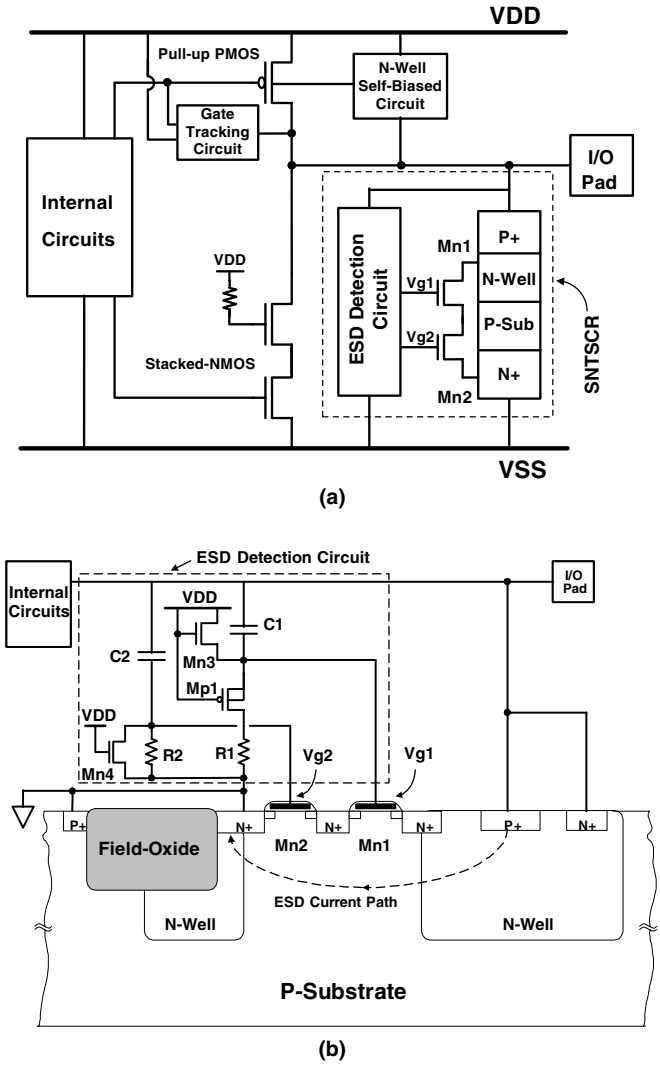

Fig. 6. (a) ESD protection circuit with the SNTSCR device to protect the mixed-voltage I/O circuits. (b) Realizations of the SNTSCR device and the ESD detection circuit with the gate-coupling technique to trigger on the SNTSCR device.

respectively. The coupled voltage should be designed greater than the threshold voltage of NMOS to turn on M_{n1} and M_{n2} for triggering on the SNTSCR device, before the devices in the mixed-voltage I/O circuit are damaged by ESD stress. With the gate-coupled circuit technique, the trigger voltage of SNTSCR can be significantly reduced, so the SNTSCR can be quickly triggered on to discharge ESD current. From the experimental results in a 0.35 μm CMOS process, the HBM ESD level of the mixed-voltage I/O circuits with this ESD protection design has been greatly improved up to 8 kV, as compared with that (~2 kV) of the original mixed-voltage I/O circuits with only stacked NMOS device.

3.3. Extra ESD device between I/O pad and V_{DD}

Because the diode in forward-biased condition can sustain much higher ESD current, the diode string has been used for protecting the mixed-voltage I/O circuits [14]. The ESD protection design with the diode string connected between the I/O pad and V_{DD} power line for the mixed-voltage I/O circuits is shown in Fig. 7. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through the diode string to V_{DD} power line, and then through the power-rail ESD clamp circuit to the grounded V_{SS}. The ESD current at the I/O pad under the PD-mode ESD stress can be directly discharged through the diode string to the grounded V_{DD}.

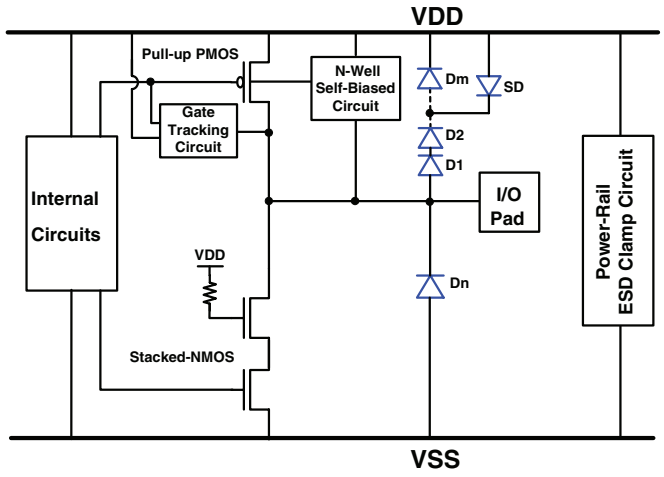

Fig. 7. ESD protection design with the diode string connected between the I/O pad and V_{DD} power line to protect the mixed-voltage I/O circuits.

The number of diodes in the diode string is determined by the voltage difference between the maximum input voltage at I/O pad and the V_{DD} supply voltage. To reduce the turn-on resistance from I/O pad to V_{DD} during ESD stress, the area of such diodes has to be scaled up by the number of the diodes in stacked configuration. The major concern of using the diode string for ESD protection in mixed-voltage I/O circuits is the leakage current. While the mixed-voltage I/O circuit is operating at a high-temperature environment with a high-voltage input signal, the forward-biased leakage current from the I/O pad to V_{DD} through the stacked diodes could trigger on the parasitic vertical p–n–p BJT devices in the diode string. The Darlington bipolar amplification of these parasitic p–n–p BJT devices in the diode string will induce a large leakage current into the substrate. In Fig. 7, an additional snubber diode (SD) was used to reduce the leakage current due to the Darlington bipolar amplification in the diode string [14].

4. ESD protection designs with ESD bus and high-voltage-tolerant power-rail ESD clamp circuits

The ESD protection scheme by using the additional ESD bus for the IC with power-down-mode application has been reported in [15]. Such design concept with ESD bus can be used to form the ESD protection network for the mixed-voltage I/O circuits, as shown in Fig. 8. The additional ESD bus line is realized by a wide metal line

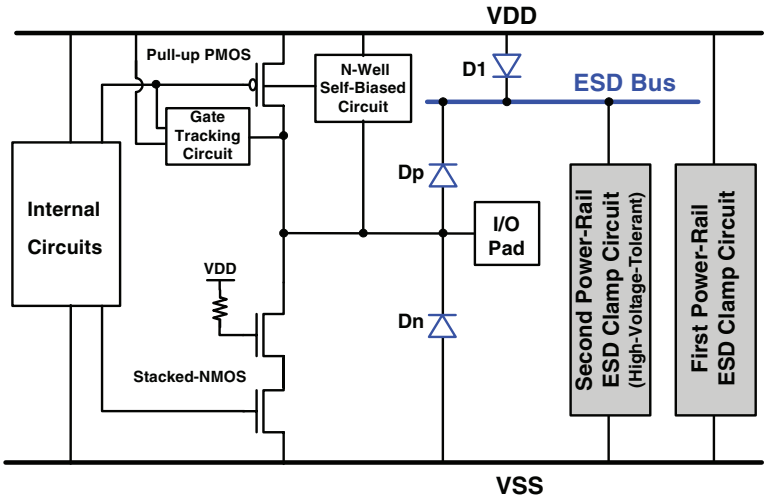

Fig. 8. The ESD protection network with the additional ESD bus line for the mixed-voltage I/O circuits.

in CMOS IC [15,16]. To save layout area, the ESD bus can be realized by the different metal layer, which overlaps the V_{DD} power line. The ESD bus is not directly connected to an external power pin, but initially biased to V_{DD} through the diode D1 in Fig. 8. The diode D1 connected between the V_{DD} power line and ESD bus is also used to block the leakage current path from the I/O pad to V_{DD} during normal circuit operating condition with a high-voltage input signal. The diode D_p is connected between I/O pad and ESD bus, whereas the diode D_n is connected between V_{SS} power line and I/O pad. One (the first) power-rail ESD clamp circuit is connected between V_{DD} power line and V_{SS} power line. Another (the second) power-rail ESD clamp circuit is connected between the ESD bus and V_{SS} power line. The second power-rail ESD clamp circuit connected between ESD bus and V_{SS} power line should be designed with high-voltage-tolerant constraints without suffering the gate-oxide reliability issue. The ESD current at the I/O pad under PS-mode ESD stress can be discharged through the diode D_p to the ESD bus, and then through the second power-rail ESD clamp circuit to the grounded V_{SS}. The ESD current at the I/O pad under the PD-mode ESD stress can be discharged through the diode D_p to the ESD bus, the second power-rail ESD clamp circuit to V_{SS} power line, and then through the parasitic diode of the first power-rail ESD clamp circuit to the grounded V_{DD}. With the turn-on-efficient power-rail ESD clamp circuits, high ESD level for the mixed-voltage I/O circuits can be achieved by this ESD protection scheme with ESD bus. Here, the design key point is how to design such a high-voltage-tolerant power-rail ESD clamp circuit with only low-voltage thin-oxide CMOS devices.

4.1. High-voltage-tolerant power-rail ESD clamp circuit for ESD bus with $2 \times V_{DD}$

Fig. 9 shows the high-voltage-tolerant power-rail ESD clamp circuit realized with only 1.2 V devices for 2.5 V

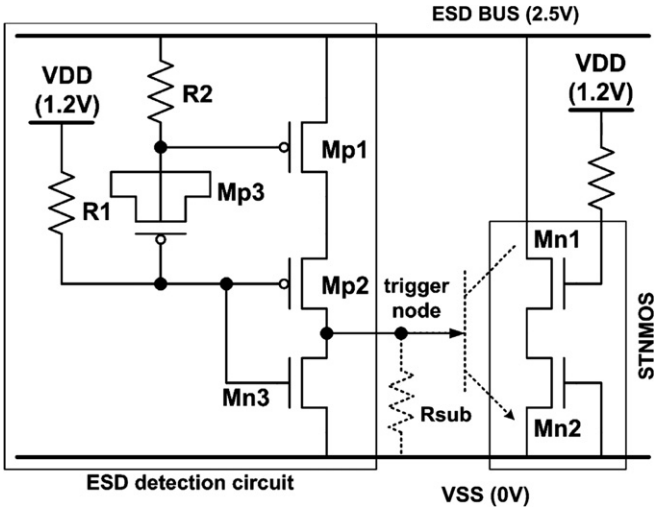

Fig. 9. The high-voltage-tolerant power-rail ESD clamp circuit designed with only 1.2 V devices for operating with ESD bus of 2.5 V.

mixed-voltage I/O applications [17], which contains the ESD clamp device and an ESD detection circuit. The ESD clamp device (M_{n1} and M_{n2}) is realized by the stacked-NMOS (STNMOS) with the substrate-triggered technique [10]. The STNMOS is kept off without gate-oxide reliability during normal operation conditions. The ESD detection circuit is kept inactive during normal operation conditions, but it becomes active to provide substrate-triggered current to quickly trigger STNMOS on under ESD stress conditions. Here, the time constant of $R2$ and C (realized by M_{p3}) should be designed to distinguish the power-on transition from the ESD transition.

In normal operation conditions with V_{DD} power supply of 1.2 V, the ESD bus line could be charged up to maximum 2.5 V by the 2.5 V input signal at I/O pad. With a maximum voltage level of 2.5 V on the ESD bus, M_{p1} and M_{p2} are kept off but M_{n3} is turned on to bias the substrate of STNMOS at V_{SS}, such that STNMOS is

guaranteed to be kept off. The voltages across the gate-drain, gate-source, and gate-bulk terminals of every device in Fig. 9 do not exceed the process limitation (~1.32 V in a given 1.2 V CMOS process). When ESD transient voltage is conducted to ESD bus from I/O pad with V_{SS} relatively grounded, but V_{DD} floating with an initial voltage level of 0 V, M_{p1} and M_{p2} (whose initial gate voltages are at a low voltage level of ~0 V) can be quickly turned on by ESD energy to generate the substrate-triggered current to trigger the STNMOS into its snapback region to discharge ESD current from ESD bus to V_{SS}.

The turn-on speed of STNMOS with or without ESD detection circuit is measured and shown in Fig. 10, where a 0–20 V voltage pulse with a rise time of 10 ns is applied to ESD bus with grounded V_{SS} and floating V_{DD}. The overshooting peak voltage of STNMOS without ESD detection circuit is about 10 V, which could damage the gate oxide of the low-voltage devices. On the contrary, the 20 V voltage pulse can be quickly clamped by STNMOS with ESD detection circuit to a low voltage level without suffering the high overshooting voltage. Transmission line pulsing (TLP) generator [18] is used to verify the secondary breakdown current (I_{t2}) of STNMOS with or without ESD detection circuit. The measured TLP I–V curves of STNMOS with device dimension (W/L) of 240 μm/0.2 μm are shown in Fig. 11. The STNMOS with ESD detection circuit can be triggered on at a lower voltage level than that without ESD detection circuit. In addition, the turn-on uniformity among the multiple fingers of STNMOS can be improved to enhance its ESD robustness by the substrate-triggered effect [10], such that the I_{t2} of STNMOS with ESD detection circuit can be increased from 1.4 A to 2.4 A.

Another high-voltage-tolerant power-rail ESD clamp circuit realized with the stacked-PMOS device has been reported [19,20], as shown in Fig. 12. In this power-rail ESD clamp circuit, the stacked-PMOS device (M_{p1} and M_{p2}) with large device width is designed to discharge ESD current between the ESD bus line and V_{SS} under

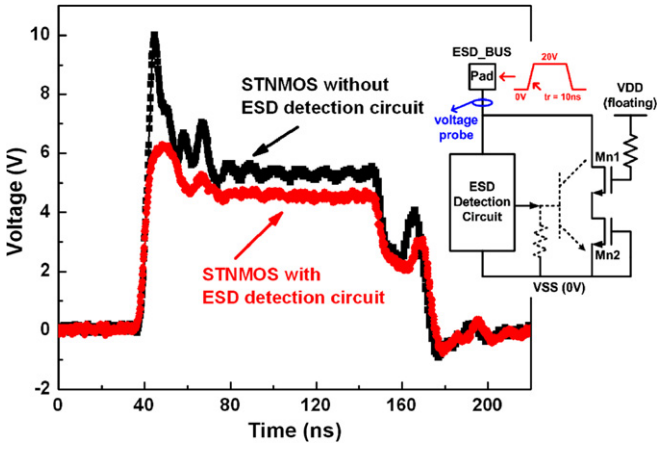

Fig. 10. Measured voltage waveforms to verify the turn-on efficiency of the high-voltage-tolerant power-rail ESD clamp circuit with STNMOS.

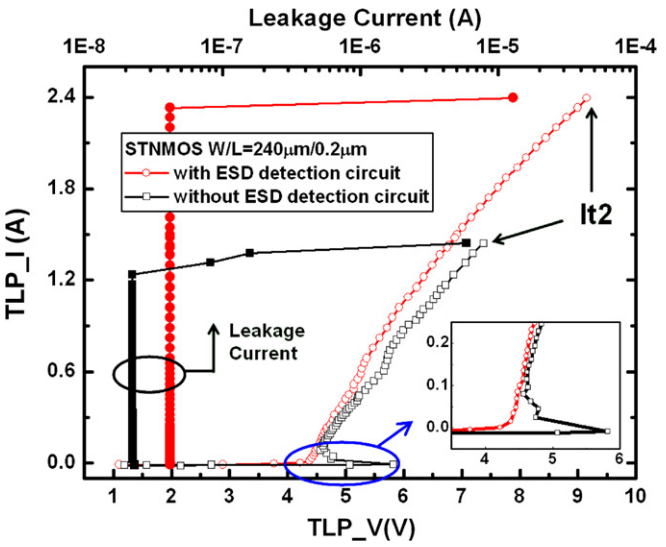

Fig. 11. TLP-measured I–V curves of STNMOS with or without ESD detection circuit.

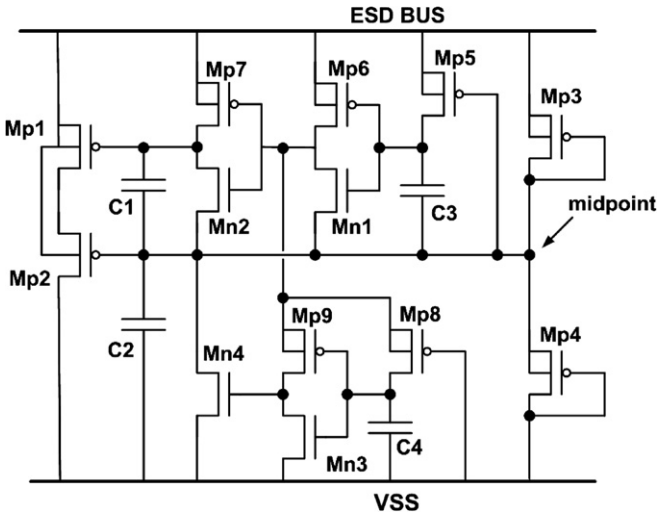

Fig. 12. High-voltage-tolerant power-rail ESD clamp circuit realized with stacked-PMOS structure for ESD bus of twice the ordinary V_{DD}.

ESD stress. The M_{p3} and M_{p4} are the long-channel devices which divide the voltage of ESD bus by two for the mid-point with consideration of minimal leakage current. The gates of M_{p1} and M_{p2} are individually controlled by the RC-based ESD detection circuits. During normal circuit operating condition, the gate of top PMOS M_{p1} is biased at ESD bus, and the gate of bottom PMOS M_{p2} is biased at half of ESD bus. Therefore, the M_{p1} and M_{p2} are kept off without the gate-oxide reliability issue. Under ESD stress condition, both gates of M_{p1} and M_{p2} are initially biased at ~0 V by the ESD detection circuits, therefore the ESD current is discharged through the turned-on stacked-PMOS device. The design concept of stacked-PMOS configuration can be further applied to implement the power-rail ESD clamp circuit for ESD bus with $3 \times V_{DD}$ [20]. The standby leakage current through the

voltage divider in the ESD detection circuit should be further reduced for low-power applications.

4.2. High-voltage-tolerant power-rail ESD clamp circuit for ESD bus with $3 \times V_{DD}$

To meet the applications with $3 \times V_{DD}$ input signals, the power-rail ESD clamp circuit is realized by using both 1 V and 2.5 V devices for the ESD bus of 3.3 V [21], as shown in Fig. 13. The internal power supply voltage of V_{DD} is only 1 V. The stacked-NMOS structure is formed by two NMOS transistors (M_{n1} and M_{n2}) with 2.5 V gate oxide.

During normal circuit operating condition, the gate of top NMOS M_{n1} is biased at V_{DD}, and the gate of bottom NMOS M_{n2} is biased at V_{SS}. Therefore, the stacked-NMOS structure has no gate-oxide reliability problem under the bias (3.3 V) of ESD bus. The ESD detection circuit is composed of the two PMOS devices (M_{p1} and M_{p2}) with 2.5 V gate oxide, to provide the substrate current for triggering on the parasitic n–p–n BJT in the stacked NMOS structure during ESD stress. The gates of M_{p1} and M_{p2} are individually controlled by the RC-based detection circuit. During normal circuit operating condition, the ESD detection circuit can meet the gate-oxide reliability constraints and the local substrate of the stacked NMOS is biased at V_{SS} by the turned-on M_{n3}.

Under ESD stress condition, both the gates of M_{p1} and M_{p2} have the initial voltage level of ~0 V, while the V_{SS} pin is grounded but the V_{DD} pin floating. The ESD detection circuit will provide the trigger current flowing through the M_{p1} and M_{p2} into the p-substrate. The M_{n4} is added in the ESD detection circuit to keep the M_{n3} off and M_{p2} in a conductive state under ESD stress condition. Once the parasitic n–p–n BJT in the stacked-NMOS structure is triggered on, the ESD current is discharged from the ESD bus to the grounded V_{SS}. By this design, the turn-on-efficient high-voltage-tolerant power-rail ESD clamp circuit can be realized with an extremely low leakage current for the mixed-voltage I/O applications with $3 \times V_{DD}$ input signals.

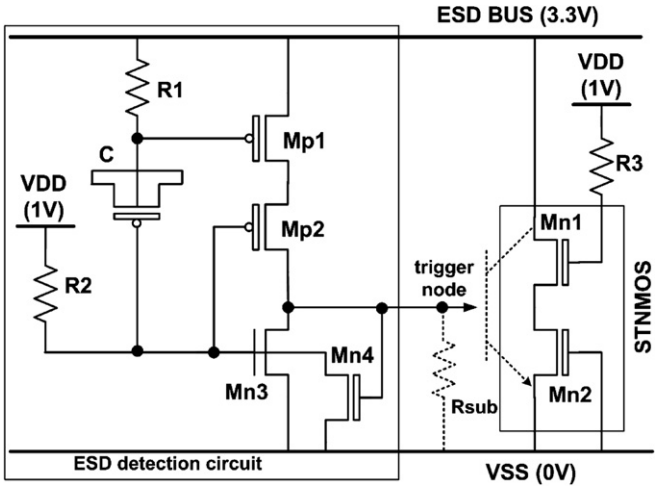

Fig. 13. High-voltage-tolerant power-rail ESD clamp circuit realized with the substrate-triggered stacked-NMOS device. The power-rail ESD clamp circuit is realized by only 1 V and 2.5 V devices for ESD bus biased at 3.3 V without suffering the gate-oxide reliability.

5. Conclusion

This paper presents an overview on ESD protection designs for the mixed-voltage I/O circuits without suffering the gate-oxide reliability issue. To improve ESD level of the mixed-voltage I/O circuits, the ESD protection design without increasing the process complexity is strongly requested by the mixed-voltage I/O circuits in consumer IC products. The ESD protection scheme (circuit solution) with ESD bus and high-voltage-tolerant power-rail ESD clamp circuit is highly recommended to protect the mixed-voltage I/O interfaces. Such ESD protection design in the mixed-voltage I/O circuits still meets the gate-oxide reliability constraints, and can prevent the undesired leakage current paths during normal circuit operating condition. Under ESD stress condition, the ESD protection circuit should be quickly triggered on to discharge ESD current. The effective ESD protection solution for the mixed-voltage I/O circuits with low parasitic capacitance for high-speed I/O applications and low standby leakage current for low-power applications will continually be an important task to SOC implementation in nanoscale CMOS technology.

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