A Novel Four-Mask-Step Low-Temperature Polysilicon Thin-Film Transistor With Self-Aligned Raised Source/Drain (SARSD)

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***Abstract*—In this letter, a novel structure of polycrystalline-silicon thin-film transistors (TFTs) with self-aligned raised source/drain (SARSD) and a thin channel has been developed and investigated. In the proposed structure, a thick SD and a thin active region could be achieved with only four mask steps, which are less than that in conventional raised SD TFTs. The proposed SARSD TFT has a higher ON-state current and a lower OFF-state leakage current. Moreover, the ON/OFF current ratio of the proposed SARSD TFT is also higher than that of a conventional coplanar TFT.**

***Index Terms*—Four masks, ON/OFF current ratio, polycrystalline-silicon thin-film transistor (poly-Si TFT), self-aligned raised source/drain (SARSD), thin channel.**

I. Introduction

LOW-TEMPERATURE polycrystalline-silicon (LTPS) thin-film transistors (TFTs) appear to be one of the most promising technologies for the ultimate goal of building large-area electronic systems on glass substrate [1]. In flat-panel liquid crystal, electroluminescent, and plasma displays, as well as in other applications such as high-speed printers and page-width optical scanners, polycrystalline-silicon (poly-Si) TFTs can be used to integrate peripheral driver circuits on glass for system integration [2]. In order to integrate peripheral driving circuits on the same glass substrate, both a large current drive and a high drain breakdown voltage (BV) are necessary for poly-Si TFT device characteristics. It has been previously reported that the use of a thinner active channel film is beneficial for obtaining a higher current drive [3], [4]. The use of a thin active channel layer, however, inevitably results in poor SD contact and large parasitic series resistance. An ideal TFT device structure, therefore, should consist of a thin active channel region, while maintaining a thick SD region. The thick SD region serves not only to reduce the lateral electric field, thus maintaining the BV [5], [6], but also to reduce the SD series resistance. Previous methods used to fabricate such ideal structures with thin active channel and thick SD regions, however, are not self-aligned in nature and require additional masks [5], [6] when compared to conventional coplanar TFTs.

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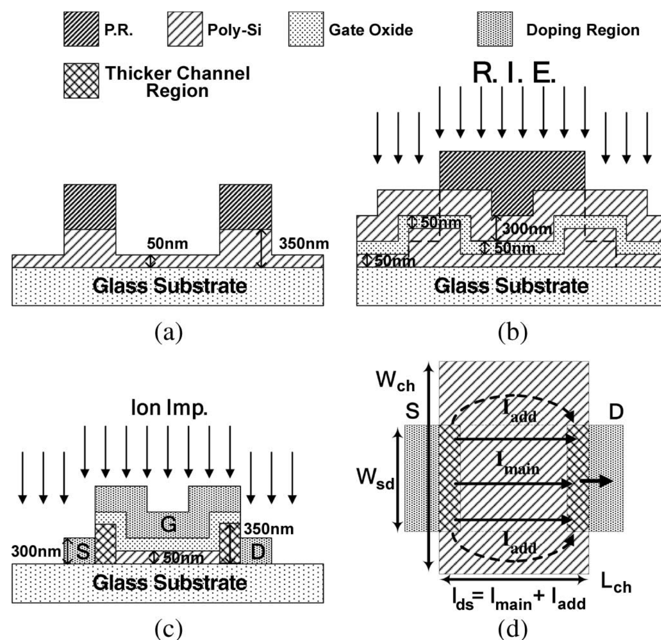

Fig. 1. (a)–(c) Schematic cross section of the major fabrication steps of the proposed n-channel SARSD TFT. (d) Schematic diagram of the proposed SARSD structure current flow.

In this letter, a novel TFT with a self-aligned raised source/drain (SARSD) structure is proposed. The new device features a thin wider active channel region and a thick SD region. The raised SD (RSD) regions are self-aligned, and no additional mask is needed.

II. Device Fabrication

The fabrication processes of the novel n-channel poly-Si SARSD TFT were given as follows: A 350-nm-thick α-Si layer for the active region was deposited by a low-pressure chemical vapor deposition (LPCVD) system using SiH_4 at 550 °C on 500-nm thermal oxidized silicon wafers. After patterning, the thin α-Si (50 nm) regions and the thick α-Si (350 nm) regions were formed using reactive ion etching (RIE) at this mask step, as shown in Fig. 1(a). The widths of the thick α-Si (350 nm) regions were 5 μm. Then, the deposited α-Si film was annealed in nitrogen ambient at 600 °C for 24 h to become the poly-Si film. After recrystallization, the etching damages of the channel surface were recovered, and the surface

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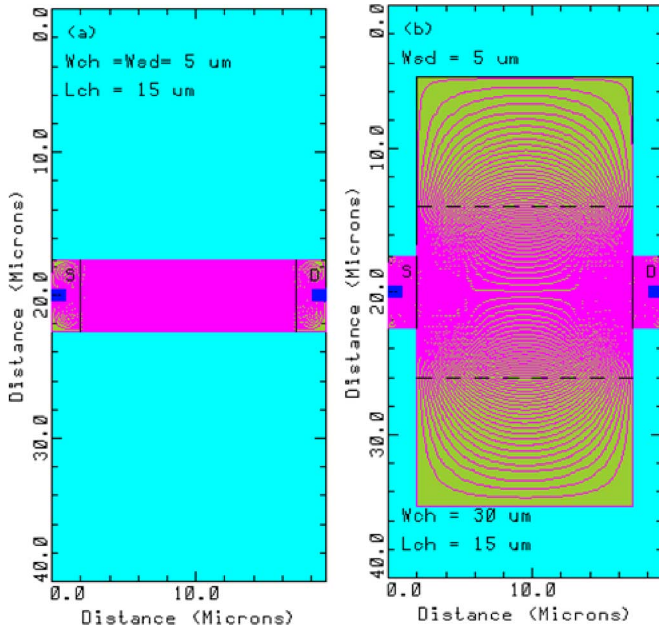

Fig. 2. Current flow lines simulated by MEDICI in (a) the conventional coplanar structure with $L_{\mathrm{ch}} = 15\ \mu$m and $W_{\mathrm{ch}} = W_{\mathrm{sd}} = 5\ \mu$m, and (b) the SARSD structure with $L_{\mathrm{ch}} = 15\ \mu$m, $W_{\mathrm{sd}} = 5\ \mu$m, and $W_{\mathrm{ch}} = 30\ \mu$m.

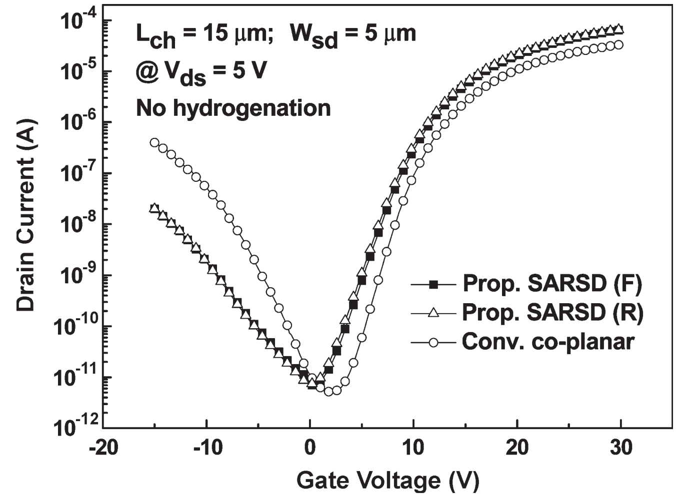

Fig. 3. $I_{\mathrm{ds}}-V_{\mathrm{gs}}$ output characteristics of the proposed SARSD TFT in both forward mode (F) and reverse mode (R), and the conventional coplanar TFT, in which the reverse mode has the source and drain electrodes exchanged.

roughness is approximately 3 nm. A 50-nm plasma-enhanced chemical vapor deposition (PECVD) gate oxide layer was deposited at 350 °C, and then, a 300-nm LPCVD poly-Si gate was deposited. After defining the undoped gate region [gate mask area $= L_{\mathrm{ch}} \times W_{\mathrm{ch}}$, as shown in Fig. 1(d)], the remnant 50-nm oxide film and 50-nm poly-Si film would be further removed using the RIE system to form an isolated active region, as shown in Fig. 1(b) and (c). After the photoresist was removed, the gate, source, and drain regions were formed by ion implantation of phosphorous (dose $= 5 \times 10^{15}$ cm^{-2} at 50 keV) and then activated in nitrogen ambient at 600 °C for 24 h, as shown in Fig. 1(c). It is worth pointing out that the gate region width W_{ch} is larger than that of the SD region W_{sd}. Therefore, a thin and wider active region would be formed below the whole of the gate region, as shown in Fig. 1(d). After the source, drain, and gate activation, the 500-nm passivation oxide was deposited by PECVD. Contact holes were opened using wet etching of the passivation oxide layer. A layer of aluminum was then deposited by thermal coater system with a thickness of 600 nm. After metal patterning, a forming gas anneal is performed at 400 °C for 30 min. The total masks of our fabrication processes are four masks, which are less than those of conventional processes in an RSD poly-Si TFT [5], [6]. For comparison, the conventional coplanar poly-Si TFTs with 50-nm channel thickness were also fabricated in the same run.

III. Results and Discussion

Fig. 1(d) shows the possible current flow paths of the proposed SARSD structure. To ensure that the current flow of the proposed SARSD structure would be as shown in Fig. 1(d), the two-dimensional numerical simulator MEDICI was used. Fig. 2 shows the simulated current flow lines of the conventional coplanar and proposed SARSD poly-Si TFT structures in ON-state. The channel length and width of the simulated conventional coplanar structure are 15 and 5 μm, respectively. From the simulation results in Fig. 2(a), the simulated current flow lines of the conventional structure are uniformly distributed in the channel region and the SD regions. However, for the proposed SARSD structure, as shown in Fig. 2(b), the current flow paths are different from the conventional sample in ON-state. It is because the channel width is wider than the SD width, and a wider channel width would obtain a higher drain current. Therefore, it can be convinced that the proposed RSD structure would obtain a higher drain current than the conventional coplanar one.

As shown in Fig. 3, the proposed SARSD TFT has higher ON-state current ($V_{\mathrm{gs}} = 30$ V) and lower OFF-state leakage current ($V_{\mathrm{gs}} = -15$ V) than the conventional TFT. In ON-state, the main reasons for a higher ON-state current are wider channel width ($W_{\mathrm{ch}} = 30\ \mu$m) and smaller SD parasitic resistances [6]. On the contrary, in OFF-state, the minimum OFF-state leakage current of the proposed SARSD TFT is only slightly larger than that of the conventional TFT. It is because the leakage current is determined by the electron–hole pair generation rate in the depletion region at the drain edge. The pair generation rate is strongly dependent on the number of trap states in the forbidden gap, the lateral electric field, and the generation volume of the depletion region [7]–[9]. Although a thicker drain region causes the generation volume of the SARSD TFT (must be approximately W_{sd} multiplied by the thickness of the depletion region) to increase, the maximum lateral electric field near the drain region of the proposed SARSD TFT largely dropped from 2.13 to 1.57 MV/cm due to the thick SD region [10]. At higher drain and reverse gate bias ($V_{\mathrm{ds}} = 5$ V and $V_{\mathrm{gs}} = -15$ V), the leakage current would be due to the thermionic field emission via grain boundary defects [11]. Therefore, the proposed SARSD TFT has lower OFF-state leakage current than the conventional TFT because the maximum lateral electric field near the drain region largely dropped, even though the generation volume increased. Table I lists some of the parameters of the two devices (forward-mode SARSD TFT and coplanar

TABLE I
SOME PARAMETERS OF SARSD IN FORWARD-MODE AND CONVENTIONAL COPLANAR n-CHANNEL poly-Si TFTs MEASURED AT $V_{ds} = 5$ V

	I_{max} (µA)	I_{min} (pA)	I_{off} (nA) (V_{gs}= -15V)	On/Off Current ratio	Maximum Lateral E. Field (MV/cm)
Conventional co-planar TFT	33.3	5.15	398	6.4×10^6	2.13
Proposed SARSD TFT	64.8	6.57	19.9	9.8×10^6	1.51

TFT). The ON/OFF current ratio of the proposed SARSD TFT is also slightly higher than that of the conventional one.

IV. CONCLUSION

In this letter, a novel four-mask-step n-channel LTPS TFT with an SARSD region and a thin channel was proposed and investigated. The gate mask was used to form a large-area thin-channel region below the gate region, and the SARSD region can be formed without the additional mask step. A lower OFF-state leakage current and a higher ON/OFF current ratio can be obtained for the proposed SARSD TFT. The TFT fabrication processes are fully compatible with the conventional four-mask ones. This new TFT structure may be an attractive device structure for future high-performance large-area device applications.

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