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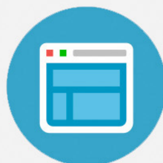
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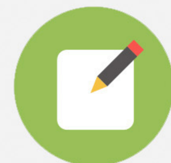

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Advance static random access memory soft fail analysis using nanoprobing and junction delineation transmission electron microscopy

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Nanoprobing was used to analyze the soft cell failure of submicron static random access memory (SRAM) at cell level by means of a Zyvex S100 nanomanipulator system inside a scanning electron microscopy and a multiprobe atomic force probe system, respectively. For the 256 Kbyte dual-port SRAM block, the failure areas exhibit very weak positive-channel field effect transistor drain currents of several magnitudes below the target values, while the drain currents of negative-channel field effect transistor cell transistors are in the expected range. A junction delineation or junction stain was applied to transmission electron microscopy samples to delineate areas with different doping levels so as to make the fail sites visible. Due to the difference in etching behavior of the fail and a reference area, missing lightly doped drain extensions and a partially blocked source/drain implantation were identified as the failure mechanisms. © *2007 American Vacuum Society.*
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I. INTRODUCTION

The soft cell failure (single cell failure sensitive to voltage) of an advance static random access memory (SRAM) cell is one of the failure analysis group.[1,2] The bitmaps of affected memory regions show single cell failure at supply voltage below 1.0 V, and the number of cell failure increased with the decrease of supply voltage. The ever-shrinking device dimensions in state-of-the-art technologies lead to an increased demand to measure the changes in dopant concentration on a smaller scale. One-dimensional techniques such as secondary ion mass spectroscopy possess excellent sensitivity to dosage concentration but do not provide the required spatial resolution. The reliable two-dimensional (2D) techniques are hence required to analyze the implantation profiles at a specific failure area of the deep submicron chips. Most of these techniques, such as scanning capacitance microscopy[3,4] (SCM) and scanning spreading resistance microscopy,[5] start with a mechanical cross section through the failure site and then apply a scanning method by registering the local carrier concentration of the sample surface. However, the devices and implant profiles for sub-100-nm technologies quickly approach the typical interaction areas of the probe tip with the sample surface and a sufficient signal to noise ratio becomes difficult to maintain as the probe volume decreases. In this study, the specific failed cell specimens were approached by focused ion beam (FIB) fabrication so that the sample surface implemented ion damage and was made amorphous by Ga ion resulting in no SCM signal measurement. Moreover, for the commercial SCM with a gold-coated silicon tip radius of approximately 25 nm, the spatial resolution (10–20 nm) is insufficient when applied for sub-100-nm device doped profile analysis.[6,7]

Another solution for 2D dopant characterization, that has been used for decades, is the method of junction etch or dopant-selective etching.[8–14] This method is done by first staining the sample cross section with an appropriate chemical solution to transfer the dopant profile into a topography profile then imaging it in an electron microscope. Nevertheless, the etch process is rather complex and the result depends on a variety of parameters, such as specimen thickness, etching recipe, etching time, and etching temperature, which usually leads to poor sample reproducibility. In order to approach reproducible results cross section thin lamella were fabricated with FIB for consistent specimen processing. Etching solution were evaluated with 0.5% HF/95.5% HNO_3 (reported by Kawamura *et al.*, Marcus and Sheng, and Yoo *et al.*) and HF (49%):HNO_3 (69%):CH_3COOH (99.7%)=1:3:8 (reported by Neogi *et al.*, Y. Liao *et al.*, and Marons and Sheng) for negative-channel field effect transistor (NFET) and positive-channel field effect transistor (PFET), respectively, at room temperature and low temperature. The appropriate etching solution for PFET dopant profile is carried out by etching at low temperature (5 °C) with 1:3:8 mixtures resulting in the reproduction and better control of the etching process.

On the other hand, the imaging and etching steps, which require high lateral resolution and sensitivity to dopant concentration, can be optimized independently. The possibility of applying transmission electron microscopy (TEM) in etch-

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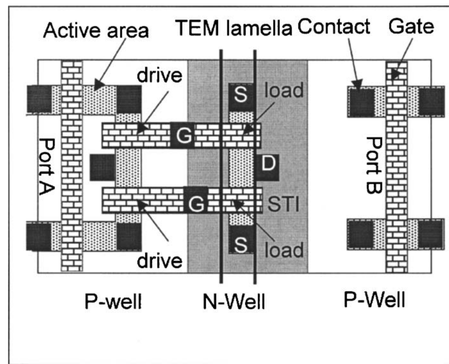

FIG. 1. Schematic layout of the eight transistor dual-port SRAM cell (not to scale). Access and drive transistors are NMOS, load transistors are PMOS devices. The two black lines indicate the physical location of the TEM lamellas.

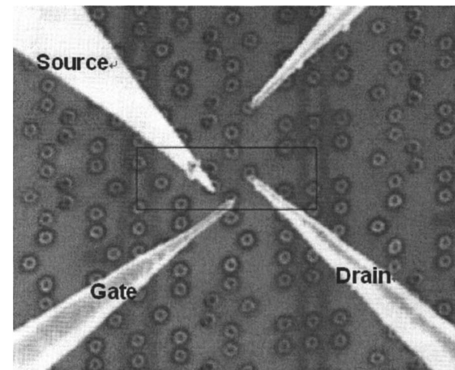

FIG. 2. SEM image at contact level with the probe tips placed on the source, drain, and gate of a *p*-load transistor. The rectangle shows the failed single cell.

ing the surfaces of a FIB fabricated TEM lamella[14] opens a plausible option for qualitative studies of the differences in local implant doses, especially for the sub-100-nm devices.

This article is divided into three parts: A description of devices under investigation, failure analysis equipments, and the test methods are presented in the section of experimental methods. The outcome of bitmap studies and electrical localization of failure sites using the nanoprobing technique are described in the session of experimental results. The results of TEM characterizations are also discussed in the failure localization section. Finally, a model for the cause of failure is proposed.

II. EXPERIMENTAL METHODS

The samples under investigation were 256 Kbyte dual-port SRAM manufactured using a deep submicron complementary metal oxide semiconductor process on *p*-type substrate. The memory cell consisted of eight transistors as shown in Fig. 1. Gate lengths and widths were fine tuned for optimum cell performance and low leakage functionality. A narrow stripe of the cell area was *n*-well implanted (gray area shown in Fig. 1) to yield the two positive-channel metal oxide semiconductor (PMOS) load transistors, while the access transistors of ports *A* and *B* and the drive transistors were negative-channel metal oxide semiconductor (NMOS) devices. After self-aligning source/drain (S/D), halo and light doped drain (LDD) implantations complete the device fabrication. Several rapid annealing steps were applied after implantation for recrystallization and dopant activation purposes. Tungsten (W) contacts connect S/D areas and gates with the five layer Cu metallization. The detailed device fabrication process is described elsewhere.[15]

Bitmaps of failure memories were acquired at wafer level test for 1.2 V and at reduced voltages using a Teradyne J750 device tester. Failure signatures were inspected with a BVIEWNG bitmap viewing software.[16] Nanoprobing used either a Zyvex nanoprober or an atomic force probe (AFP) multiprobe system was employed for data acquisition at single transistor level. Both methods required top-down sample polishing into the contact level to allow direct access to the transistor nodes.

The Zyvex S100 system with four tungsten (W) probes mounted onto an accurate nanomanipulator was attached to the stage of a Philips XL 30 scanning electron microscopy (SEM). The SEM chamber, with typical pressure of about 6×10^{-6} mbar, was equipped with the Evactron plasma cleaner to minimize the sample contamination. SEM imaging was used for sample and needle navigation to approach the contacts. An *in situ* cleaning procedure was applied to the probe tips before every measurement to guarantee low contact resistances. The sample surface was cleaned with an oxide etch dip, which also increased the topography to the W contacts for better probe tip contact. A good grounding of the sample was essential for reliable measurements.

Figure 2 shows a SEM image of a failure sample at contact level with the Zyvex probe needles placed on the source, drain, and gate of a *p*-load transistor. The needles could easily be moved to neighboring contacts. However, a difficulty might arise when the contacts are spaced by more than 10–15 μm, because the SEM magnification had to be lowered and might be insufficient for exact needle positioning.

Alternatively, a multiprobe AFP nanoprobing system was employed. The principle of the AFP is based on the conventional atomic force microscope technique. The system is equipped with four tips, which could be operated to acquire their individual topography images for exact tip placement. A short oxide etching step is applied to the sample surface at contact level to provide the necessary topography for locating the target contacts. Because the AFP provides just a limited scan range of about 15 μm, it is advisable to place a shallow FIB mark near the target cell for identification, especially for regular patterns such as SRAM arrays. Large and abrupt height differences of the sample surface can easily lead to tip damage during scanning, therefore FIB marking and surface etching need to be carefully performed to minimize the topographical change to a range of several nanometers. After connecting to the target contacts, the measurements were accomplished by means of a parameter analyzer. Mechanical, electrical, and thermal stabilities are essential operating parameters in avoiding sample drift and noise.

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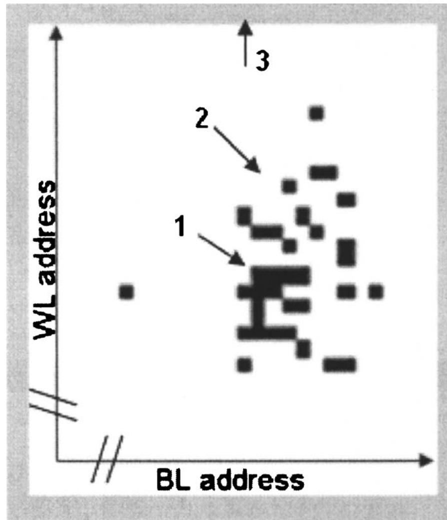

FIG. 3. Failure bitmap at low voltage shows a typical single cell cluster failure (black squares signify failed single cells). The numbers 1, 2, and 3 correspond to cell locations where the *I-V* characteristics of Fig. 5 were acquired.

After the failed transistor was identified, a TEM lamella with about 100 nm thickness was prepared for the target area using standard FIB polishing procedures. Both sides of the TEM lamella were then stained with a wet chemical junction etching.[8] A mixture of oxidizing and HF-containing species with $HF:HNO_3:CH_3COOH=1:3:8$ solution chemically etching for several seconds at 5 °C ice water, specially adopted for highly *p*-type doped Si, was applied to yield a delineation of Si areas with different doping levels. The specimen was finally imaged using a TEM (Philips CM200-FEG) operated at 200 keV.

III. EXPERIMENTAL RESULTS

The results of wafer tests at various supply voltages showed that the functional yield decreases with the decrease of supply voltage when the supply voltage is below 1.2 V. The fallout was due to an increased failure rate of the 256 Kbyte dual-port memories especially at the wafer edge. Figure 3 shows the bitmaps for single cell cluster failures, which typically cover an area of 10–50 μm in diameter.

The number of cell failures as well as the affected area increased with the decrease of supply voltage, signifying a soft failure signature. Most memories were affected by only one single cluster failure. A stacked bitmap analysis revealed that the cluster failures are not randomly distributed over the memory area but always affect characteristic regions near the corner of the cell array.

Figure 4 shows a stacked bitmap of a 256 Kbyte memory at low voltage. The memory consists of two 128 K blocks leading to an interruption of the cell layout in the middle of the word line (WL) direction. It is obvious that the cluster failures frequently occur near the three corners of the lower memory block. Furthermore, the failure rate strongly depends on the orientation of the memory on the wafer. Memories with a layout rotated by 90° are less affected.

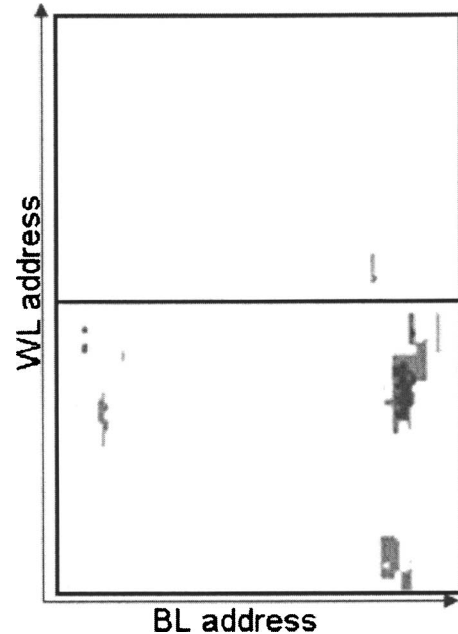

FIG. 4. Stacked failure bitmap of a dual-port memory at low voltage. The gray area indicates failure addresses which occurred only for one chip. The black area indicates identical failure addresses for multiple bits.

Further electrical localization relied on the comparison of the cell transistor characteristics between failed and reference cells using nanoprobing to access the transistor contact nodes. The measurements are in good agreement for both nanoprobing techniques, the Zyvex system and the multiprobe AFP. Table I summarizes the *I-V* characteristics from single failed cell nanoprobed data where it can be seen that the six NFET devices fulfil the specifications, while the two PFET transistors exhibit very weak drain currents about two orders of magnitude below the target value in the cluster failure area.

Figure 5 shows the normalized PFET current-voltage (*I-V*) curves for a failed cell (curve 1), a randomly chosen pass cell near the edge of the cluster failure area (curve 2), and a reference device picked from an unaffected area of the same memory array (curve 3). The approximate cell positions can be referenced to Fig. 3. While the reference device is in good agreement with the simulated target curve (curve 4 in Fig. 5), both pass and failed cell PFET transistors in the cluster failure area show drain currents several orders of magnitude lower than the target. The fact that the cell is functional with *I-V* characteristics of curve 2 is evidenced by the robustness of cell design. However, if the voltage were further lowered, this cell would also certainly fail.

The location of the TEM lamellas, which were prepared from the *p*-load transistor region, is schematically shown in Fig. 1. The cross-sectional specimen covers both *p*-load transistors and two of the three contacts. The center contact between the gates is off the plane of cross section and is not part of the TEM lamella. Figures 6(a) and 6(b) show bright-field TEM images of failed and passed cells, respectively. Both images were acquired from the same TEM lamella after junction stain etching, prepared from the center of the cluster

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TABLE I. SEM nanoprobed *I-V* characteristics of failed cell (SG=select gate, PG=pass gate, PD=pull down, and PL=pull load).

Transistor name and *I-V* characteristics			Top side: Drain sweep (μA)	Top side: Drain sweep (μA)	Bottom side: Drain sweep (μA)	Bottom side: Drain sweep (μA)
SG	V_g=1.2 V, V_d=1.2 V,	I_d	20.3	−20.9	16.4	−18.8
(NFET)	V_s=V_b=0 V	I_s	−20.3	20.9	−16.4	18.8
PG		I_d	20.3	−20.9	16.4	−18.8
(NFET)		I_s	−20.3	20.9	−16.4	18.8
PD		I_d	20.3	−20.9	16.4	−18.8
(NFET)		I_s	−20.3	20.9	−16.4	18.8
PL	V_g=−1.2 V, V_d=−1.2 V,	I_d	−0.17	0.38	−0.17	0.24
(PFET)	V_s=V_b=0 V	I_s	0.17	−0.38	0.17	−0.24

failure area. Another lamella was prepared under identical junction etching conditions for a pass region far outside the cluster fail area and the corresponding TEM image is shown in Fig. 6(c).

Areas with different shades of gray could be distinguished, representing either different materials or different local sample thicknesses. The etching rate of Si was high for areas with high carrier concentration, such as polygates, S/D and LDD implants, and the polysalicide. The areas became light gray or even white when they are thinner or completely etched through. The Si areas with lower implant dosage (e.g., the substrate) were etched at a lower rate and appeared with darker contrast. The thicknesses of insulators, such as oxide, nitride layers, and metals, remained almost unchanged.

Distinct differences were observed via a comparison of Figs. 6(a)–6(c). First, the reference sample shown in Fig. 6(c) reveals the expected S/D implant profile. This allows us to resolve the LDD extensions under the gate spacers, while the LDD extensions are not visible in any of the images in the cluster failure area shown in Figs. 6(a) and 6(b). Second, the central S/D implant region between the two transistors is darker in the cluster failure area, especially for the failed cell [indicated by an arrow in Fig. 6(a)] while the neighboring contact S/D areas are not affected. Sample preparation artifacts were not responsible for this observation, because Figs. 6(a) and 6(b) are taken from the same TEM lamella and in all cases only the central S/D area was affected.

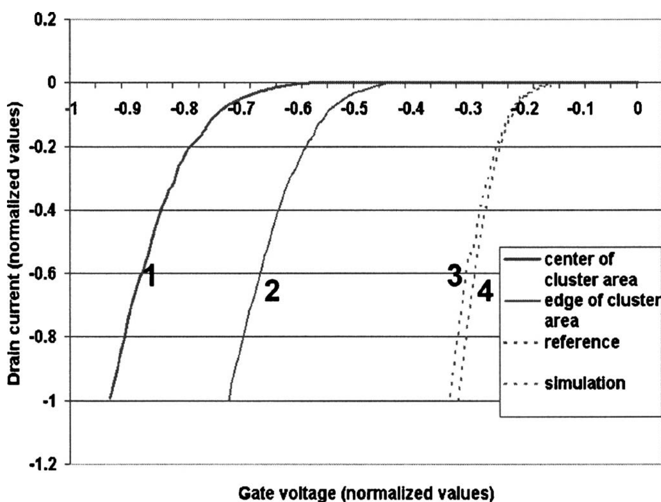

FIG. 5. Normalized PFET current-voltage (*I-V*) curves for a failed cell (curve 1), a randomly chosen pass cell near the edge of the cluster failure area (curve 2), a reference device picked from an unaffected area of the same memory array (curve 3), and a reference device with the simulated curve (curve 4).

IV. DISCUSSION

From the results presented above, we concluded that the cluster area is generally affected by poor LDD formation, leading to a high resistive electrical connection between S/D implant and the channel region under the gate oxide. This implied an additional voltage drop, affecting the device functionality and causing the measured shifts in the *I-V* characteristic of PFET devices (see Fig. 5). The bitmap signature shown in Fig. 3 suggests that the cell design is robust enough to tolerate this misprocessing for the majority of cells at least for the applied voltage range. The other characteristic signature in the failure region is the darker S/D area between the gates caused by a locally reduced doping level. This further increased the resistance between channel and contact and more likely induced the cell failures.

Locally reduced implant dosage could be explained by a mechanism that partially blocks the implantation. Typical failure causes are random particles, incomplete resist removal, or too thick oxide screening layers. The failure signature in this study is rather systematic, affecting only particular areas of the wafer (edge was worse), layout (dual-port SRAMs in a specific orientation), memory (only areas near the memory corners were affected) and transistors (only the PFET devices were affected). Random defects hence were not responsible of the failures.

The failures could, however, be explained by assuming a systematic problem with resist removal, such as scumming. Figure 7 schematically shows how resist scumming results in the soft failure signatures. The drawing represents the situation during LDD and S/D implantations of PFET, respec-

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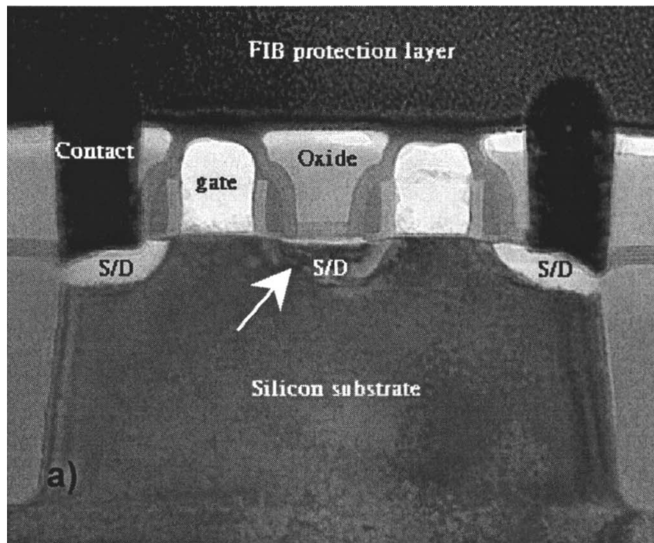

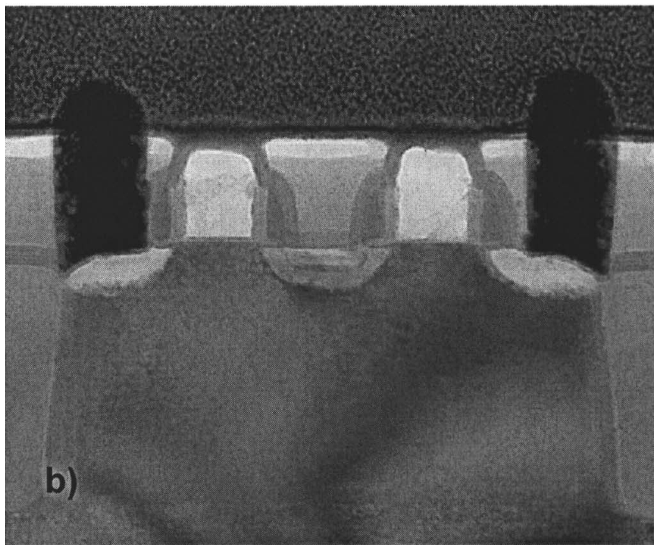

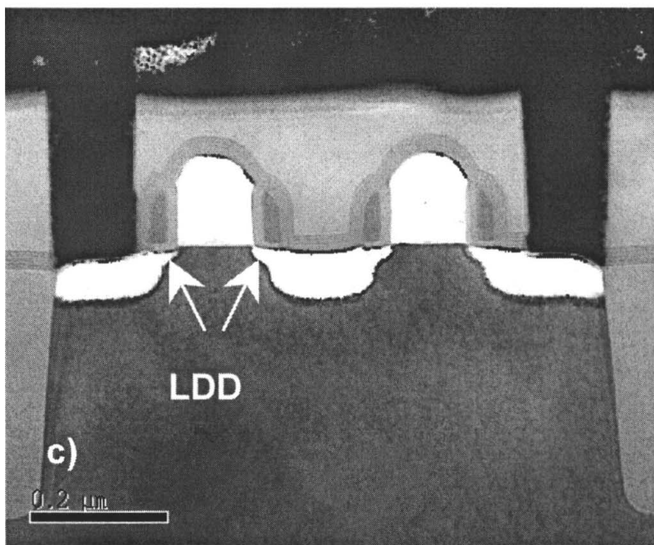

FIG. 6. TEM micrographs of a (a) failed and (b) passed cell from the cluster failure area and from (c) an unaffected region. The failed cell shows a weakly etched S/D region between the gates [indicated by the arrow shown in (a)]. LDD extensions are only visible in (c).

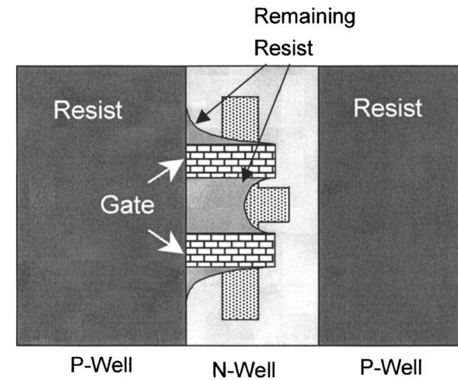

FIG. 7. Schematic plot of a single cell before LDD and S/D implantations in the case of resist scumming, leading to residual resist in the trench corner near and between the gates (not to scale).

tively. At these stages the polygates are already structured, but the contacts are still missing. The polygates are covered with a thin oxide spacer during LDD implantation and with an additional thicker nitride spacer during S/D implantation to yield the desired lateral implant dose profile. The p-well areas must be completely covered with resist for both implantations, because only a narrower resist area needs to be opened for the PFET device implant process. The removal of resist remainders in the trench corners is more difficult compared to the NFET devices where the situation is inverted. The NFET areas marked "resist" in Fig. 7 are opened, and the N well is blocked for LDD and S/D of NFET implantation. In particular, the trench corners near and between the gates will be affected, because the gates act as even smaller trenches in the direction perpendicular to the n-well stripe.

When resist remains on top of the active area, it would affect the device functionality because Si receives a reduced implant dose. The hypothetical resist profile (gray areas in Fig. 7) then blocks the LDD implants on both sides of the gates and the S/D implant between the gates, in accordance with the TEM results. Such a model can also explain why the cluster failure affects only the dual-port but not the single-port SRAM layout. For the single-port SRAM, the areas of p well and n well are equally distributed because only four instead of six NFET transistors are required. This improves the etch robustness against loading effects. The etching process is in fact sensitive to loading effects, so that the cluster failures affect only a few distinct areas of the dual-port SRAM, especially near the corner of the memory. Finally, resist thickness and etching behaviors might differ slightly at the wafer edge in comparison with the wafer center and hence the wafer edge is more sensitive to the cluster fail signature.

V. CONCLUSIONS

A junction stain TEM analysis on 90 nm technology SRAM single cell soft failures revealed the missing LDD extensions and partially blocked S/D implantation for PFET devices in the failed area. The failed transistors were located by fail bitmaps and nanoprobing on all transistor nodes of

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the failed cell. The electrical measurements, performed individually by using a Zyvex nanoprober and a multiprobe AFP system, showed similar *I-V* characteristics with reduced drain currents for PFET devices by several orders of magnitude, while the NFET transistors exhibited expected values. A failure model was proposed to explain these characterizations on the basis of resist scumming during LDD and S/D implantations that partially blocks the implantations.

A comparison of the two nanoprobing techniques found that the SEM-based system possesses the advantages that the status of the tips is directly visible at all times and measurements at higher topography are possible. For the AFP system, the benefits are the easiness to place and lower the tips to the contacts and the independent positioning of the tips at any distance to each other.

ACKNOWLEDGMENTS

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