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# Study of Thermal Stability of $HfO_xN_y$/Ge Capacitors Using Postdeposition Annealing and $NH_3$ Plasma Pretreatment

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We studied the thermal stability of the as-deposited $HfO_xN_y$ thin films on the Ge substrate by employing rapid thermal annealing. After undergoing high-temperature processing, we observed several interesting physical and electrical features presented in the $HfO_xN_y$/Ge system, including a large Ge out-diffusion (>15 atom %) into high-*k* films, positive shift of the flatband voltage, severe charge trapping, and increased leakage current. These phenomena are closely related to the existence of $GeO_x$ defective layer and the degree of resultant GeO volatilization. We abated these undesirable effects, especially for reducing the amount of Ge incorporation (<5 atom %) and the substoichiometric oxide at dielectric-substrate interface, through performing $NH_3$ plasma pretreatment on the Ge surface. These improvements can be interpreted in terms of a surface nitridation process that enhanced the thermal stability of the high-*k*/Ge interface. In addition, we measured that the conductance loss in inversion was still high and it revealed independence with respect to gate bias, reflecting the fact that the minority carriers in Ge can rapidly respond either through a diffusion mechanism or through midgap trap states residing in Ge bulk substrates.
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Recently, Ge-channel devices, including bulk Ge,[1,2] strained Ge,[3] and Ge-on-insulator (GOI)[4] systems, integrated with high-*k* gate dielectrics have attracted considerable research interest. Although transistors were originally fabricated on Ge substrates, the lack of a stable Ge native oxide has been an obstacle in complementary-metal-oxide-semiconductor (CMOS) device realization with Ge. Therefore, silicon has been used in CMOS technology for many decades because of the better qualities of its native oxide, such as a low leakage current, low interface state density, and good thermal stability. With the further scaling of device and gate oxide dimensions down to the nanometer range, however, the leakage current density in $SiO_2$ has become much higher than 2 $mA/cm^2$, which is the maximum concession for low-power applications.[5] Consequently, higher dielectric constant materials with a thicker physical thickness are being introduced to suppress the concern of excessive gate leakage while maintaining the equivalent oxide thickness (EOT) of the scaled devices.

Presently, hafnium-based oxides or oxynitrides, e.g., $HfO_2$, HfON, and HfSiON, are the uppermost candidates for application among all of the potential high-*k* dielectrics. Both Si and SiGe metal oxide semiconductor field-effect transistors (MOSFETs) integrated with Hf-based gate dielectrics exhibit admirable properties,[6-8] but they also reveal undesirable surface carrier mobility degradation behavior.[9,10] Changing the substrate from silicon to germanium might be a possible solution to this problem because Ge has a higher carrier mobility relative to that of Si. From recent advances in the deposition of high-*k* materials, Ge MOSFETs incorporating high-*k* gate dielectrics have exhibited some promising performance.[11,12] In this study, we first investigated the physical and electrical characteristics of $HfO_xN_y$ thin films deposited on bulk Ge substrates and then determined the impact of thermal annealing processing on the entire capacitor structure. Recent reports have described that annealing a cleaned Ge substrate in a $NH_3$[13] or $SiH_4$[14] gas ambient, prior to deposition of a high-*k* dielectric, further improves the MOS properties on Ge. In this paper we describe our investigation of the effects on the passivation efficiency when using $NH_3$ plasma on a Ge substrate. We found that the overall MOS structures had higher thermal stability and showed improved electrical characteristics. In addition, we provide a scheme outlining the charge trapping mechanism.

## Experimental

Metal–insulator–semiconductor (MIS) capacitors were fabricated on n-type Ge substrates (resistivity ~8–12 Ω cm), which were precleaned through a cyclic rinse involving a diluted HF dip and deionized water. After wet cleaning, the $NH_3$ plasma exposure on the Ge surface of some samples was performed in the plasma-enhanced chemical vapor deposition (PECVD). $HfO_xN_y$ thin films were subsequently deposited through reactive sputtering in a Ar + $N_2$ ambient with a pure Hf target, followed by annealing in a $N_2$ atmosphere containing residual oxygen; various postdeposition annealing temperatures (500 and 600°C) and durations (30 s and 5 min) were employed. Next, a platinum (Pt) dot was deposited using electron beam evaporation through a shadow mask. For evaluating the thermal stability of the Pt/high-*k*/Ge structures, the annealing conditions described above were performed after metallization. The detailed deposited conditions and fabrication procedures have been described previously.[15] Transmission electron microscopy (TEM) and secondary-ion mass spectroscopy (SIMS) were employed to investigate the entire structure and Ge incorporation behavior, respectively. In addition, we carried out ex situ XPS measurements using an Al Kα source (1486.6 eV) to examine the effects of surface plasma nitridation on the dielectric-substrate interface and evaluate the Ge contamination level within the top high-*k* films. In electrical characterization, the capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) curves were measured using an HP4284 LCR meter, while the current-voltage (*I-V*) characteristics were measured using a Keithley 4200 semiconductor analyzer system. We further extracted the series resistance and external inductance or capacitance in measurements and then applied as a correction to the measured capacitance and conductance.[16,17] The value of the effective trapped charge density ($N_{eff}$) was determined quantitatively by measuring the hysteresis width at flatband voltage ($V_{FB}$) in the bidirectional (*C-V*) sweeps.[18] The interface state density ($D_{it}$) was estimated from both high-low frequency capacitance method[19] and the (*G-V*) characteristics using Hill's method.[20]

## Results and Discussion

*TEM image and SIMS depth profiles.*— Figure 1 shows cross-sectional TEM image of as-deposited Pt/$HfO_xN_y$/Ge structure. We characterized that the thicknesses of the $HfO_xN_y$ bulk film and the interfacial layer (IL) were ca. 73 and 19 Å, respectively. When $HfO_xN_y$/Ge system undergoes high-temperature process, of primary interest is the resultant germanium diffusion in the overlying $HfO_xN_y$ films. As the SIMS depth profiles illustrated in Fig. 2, we observed a large Hf tail, a known SIMS artifact, at the end of the $HfO_xN_y$ layer, and ion yield enhancements of both Ge and Hf at the beginning of the Ge substrate. Discarding these artificial phenomena, a U-shaped distribution of Ge did exist inside the overlying

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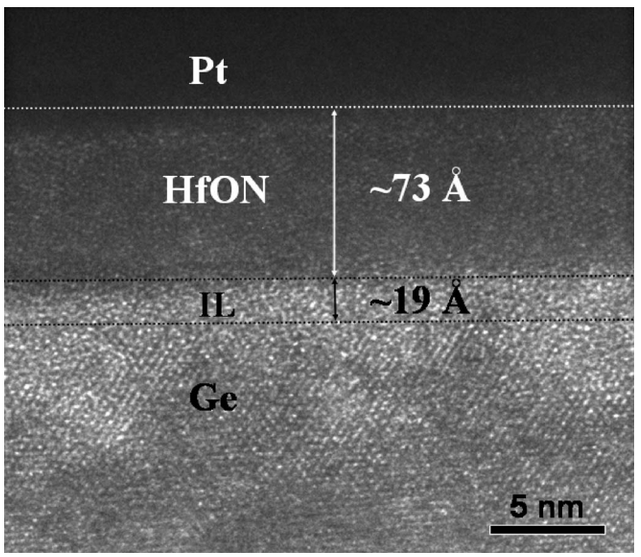


**Figure 1.** Cross-sectional TEM image of as-deposited Pt/$HfO_xN_y$/Ge gate stack.

$HfO_xN_y$ layer. From the concentration levels, we suggest that the higher thermal annealing indeed enhanced the incorporation of Ge, relative to the concentration in low-temperature processed sample. Assuming that the composition is the mixture of $HfO_xN_y$ and $GeO_xN_y$, we evaluated the amount of incorporated Ge quantitatively through X-ray photoelectron spectroscopy (XPS) measurements because of the lack of sputtering yield information for Ge in the $HfO_xN_y$ layer. Considering the respective atomic sensitivity factors of the Ge 2p3, Hf 4f, O 1s, and N 1s core levels, we estimated an average Ge concentration of ca. 12(±1.4) atom % in their overlying high-*k* layers for the 400°C processed sample, with the values increasing to ca. 19.3(±2) atom % after 500°C PDA for 5 min. Such a low-temperature annealing has led to severe Ge incorporation into the $HfO_xN_y$ dielectric film. Note that the maximum sampling depth is ca. 45 Å in Ge 2p3 spectrum, and it exactly involves in a U-shaped distribution of Ge within the high-*k* films, therefore, we use an average value for evaluating the Ge contamination. These Ge

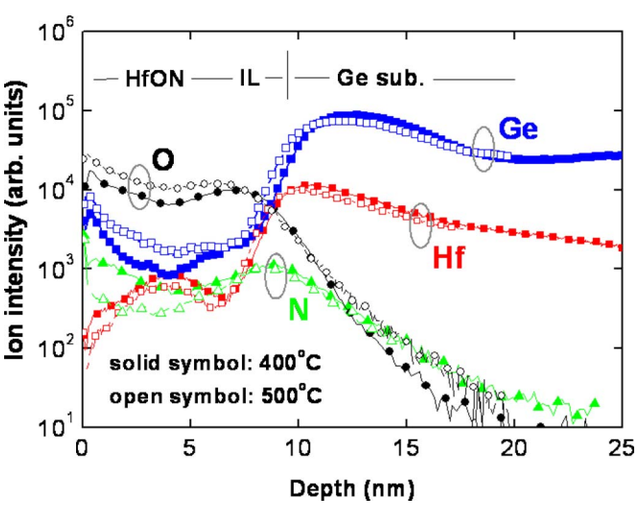


**Figure 2.** (Color online) SIMS profiles of as-deposited $HfO_xN_y$/Ge gate stack after two different annealing conditions: (a) 400°C, 30 s and (b) 500°C, 5 min

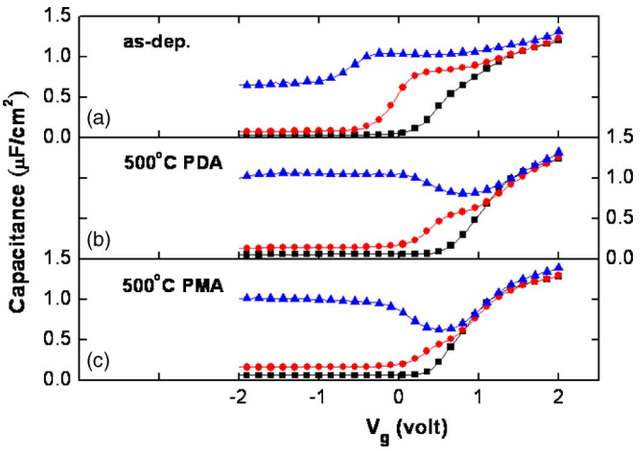


**Figure 3.** (Color online) Multifrequency C-V curves of Pt/$HfO_xN_y$/n–Ge capacitors measured at (▲) 10 kHz, (•) 100 kHz, and (■) 1 MHz: (a) as-deposited, (b) 500°C PDA, 30 s, and (c) 500°C PMA, 30 s.

atoms are incorporated in the form of $GeO_x$ through both external and internal contamination mechanisms. A higher surface concentration of Ge oxide in the SIMS analyses has been identified as arising from gaseous GeO species diffusing out from the substrate and downward into the high-*k* layer via airborne transportation; the contamination depth has been estimated to be ca. 20 Å, at least for high-*k* thin films deposited on Ge substrates.[21] This kind of surface contamination, however, can be further suppressed by capping a thick $SiO_2$ layer onto the back side of the Ge substrate prior to performing the annealing process. In addition, bulk contamination of $GeO_x$ may result from the desorption of a defective $GeO_x$-containing IL and/or the oxidation of the Ge substrate due to residual oxygen existing in a $N_2$ ambient.[15]

*Capacitance and conductance characteristics of high-k/Ge MIS capacitor.*— Figure 3 displays multifrequency *C-V* characteristics of Pt/$HfO_xN_y$/Ge capacitors before and after performing the postdeposition annealing (PDA) and postmetallization annealing (PMA), respectively. Note that the sweep direction in all of the curves presented here is from strong accumulation to strong inversion and they seem not to reach full saturation in the accumulation regimes. This phenomenon can be reasonably understood in term of fast detrapping of the trapped charges during the *C-V* sweep; on the contrary, when the voltage is swept from inversion to accumulation, the normal saturation behavior in *C-V* curves can be seen. Here, we extracted the capacitance-equivalent-thickness (CET) at a value of $V_g$ of +2 V in the *C-V* curves was ca. 28 Å for as-deposited sample; it decreased to ca. 27 and 26 Å after PDA and PMA, respectively. Extending the annealing duration to 5 min leads to further CET reduction of ca. 23 Å (not shown here), and it partly arises from the shrinkage of the IL[15] due to the fact that Ge does not prefer to form the germinate $HfGeO_4$,[22,23] unlike Si, which readily forms $HfSiO_4$, through reaction with Hf. In addition, we observed that the *C-V* stretch-out behavior with the hump emerged in depletion for all samples, indicating the existence of a large density of interface states at the dielectric interface. Considering the frequency dependence of the interface properties, the deviation of the 10 kHz curve with respect to the 1 MHz curve was obviously abated by performing subsequent annealing processes. In particular, the PMA-processed sample revealed a deeper "dip" in depletion, indicative of its improved interface quality. The quantitative analyses of the $D_{it}$ showed that the as-deposited $HfO_xN_y$/Ge gate stack revealed a large value of $D_{it}$ of ca. $8 \times 10^{12}$ $cm^{2\cdot}$ $eV^{-1}$ and it reduced to the value of $D_{it}$ of ca. $3.5 \times 10^{12}$ and ca. $1.4 \times 10^{12}$ $cm^{2\cdot}$ $eV^{-1}$ for the PDA and PMA samples, respectively. Interface traps and dangling-bond defects existing in near-interfacial Ge oxide or Ge oxynitride have

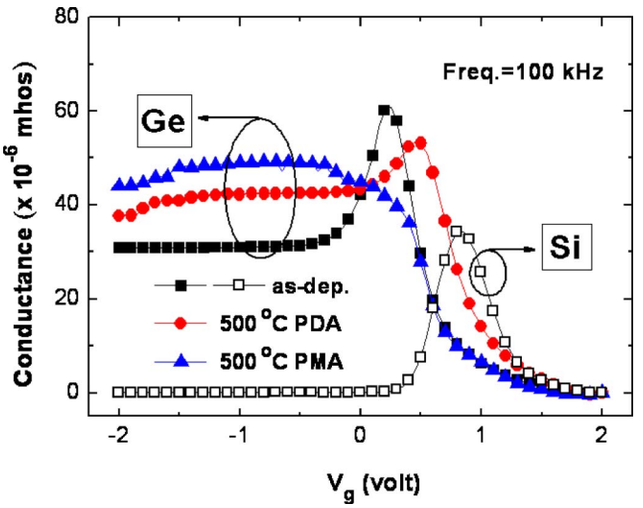


**Figure 4.** (Color online) Typical 100 kHz *G-V* curves of as-deposited and annealed Pt/$HfO_xN_y$/n–Ge capacitors (solid symbols); the annealing duration is 30 s for these two thermal processes. Note that the *G-V* curve of as-deposited Pt/$HfO_xN_y$/n–Si capacitor (open squares) is added for comparison.

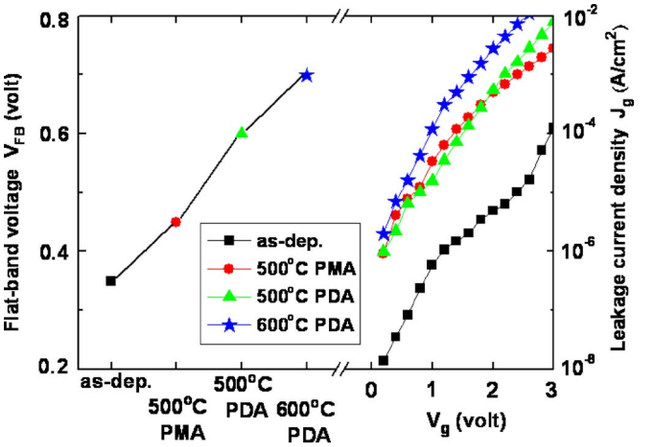


**Figure 5.** (Color online) The $V_{FB}$ shift (the left *y*-axis) and *I-V* characteristics (the right *y*-axis) of Pt/$HfO_xN_y$/n–Ge capacitors subjected to different thermal processing.

been characterized in the $HfO_2$/Ge system.[24] Recently, Chui et al. also examined that the level of $D_{it}$ was quite high and still on the order of $10^{12}$ $cm^{2\cdot}$ $eV^{-1}$ for $GeO_xN_y$/Ge gate stack even though receiving forming-gas anneal (FGA).[25] As a result, we believe that a higher value of $D_{it}$ presented at the $HfO_xN_y$/Ge interface should be associated with poor quality of the defective $GeO_x$ IL.

Figure 4 presents the corresponding *G-V* curves of Pt/$HfO_xN_y$/Ge gate stacks measured at 100 kHz; the result of Pt/$HfO_xN_y$/Si control sample is also shown for comparison. The *G-V* traces obviously exhibit an interface loss peak, corresponding to the hump observed in *C-V* depletion. The PMA process reduced the conductance peak that emerged in the *G-V* curve of the as-deposited sample to a greater extent than did the PDA process, which is consistent with the examination of $D_{it}$. Another noteworthy feature is that we measured a high value of conductance in inversion and it displayed gate-bias independence; this finding is rare for traditional Si MOS capacitors.[26] Generally, the equivalent parallel conductance passes through a peak in weak inversion and drops immediately to a very low value in strong inversion; in other words, an exponential decline of the conductance values should occur, like Si case shown here. In contrast, we observed gate-bias-independent conductance in inversion in our case, suggesting that the minority carriers in the Ge substrate, formed either through the generation/recombination via midgap trap levels or through a diffusion mechanism, do indeed contribute an energy loss in inversion and compete with interface-state loss in depletion.[27] Fukuda et al. have investigated the $GeO_xN_y$/Ge interface properties through the conductance method[28] and they also simultaneously explored the identical inversion conductance.[29] We have observed the anomalous *G-V* characteristics on low-doped (ca. $10^{14}$ $cm^{-3}$) Ge substrate for both types; this behavior can be minimized by increasing dopant concentration. Chui et al. characterized the gate-bias-independent conductance in inversion for MOS capacitors with $GeO_xN_y$ dielectric thin film on n-type (ca. $10^{16}$ $cm^{-3}$) Ge substrate, but not on p-type (ca. 5 $\times$ $10^{17}$ $cm^{-3}$) Ge substrate.[25] We suggest that the onset of this strange behavior in Ge capacitor is strongly dependent on the substrate doping level because this in turn determines the amount of minority carrier and corresponding response time. Moreover, we noticed that the measured capacitance and conductance rose after different thermal processes, which are a typical characteristic of the increased number of bulk traps, presumably caused by impurity atoms introduced during high-temperature annealing. These induced bulky defects in Ge, with energy levels near the midgap, not only contribute to greater bulk trap loss but also enhance the supply of minority carriers to the inversion layer, incurring the low-frequency-like behavior in the 10 kHz *C-V* curves. We suggest that both thermal mechanisms are significant in Ge because of a large intrinsic carrier concentration (ca. 2 $\times$ $10^{13}$ $cm^{-3}$) because they obviously affect the room-temperature *C-V* characteristics measured at high frequencies, even as high as 1 MHz.[30]

*Flatband voltage shift and gate leakage characteristics*.— As indicated in Fig. 5, we examine the variation of the $V_{FB}$ shift (the left-hand axis) and the gate leakage current $J_g$ (the right-hand axis) with respect to the annealing temperature. It can be seen that the value of $V_{FB}$ for the as-deposited sample (ca. 0.35 V) is lower than the value of the ideal work-function difference (ca. 0.9 eV) between a Pt gate and n-Ge substrate, implying that a substantial number of positive charges have been introduced into the gate dielectric/IL bi-layer. High temperature annealing caused the positive shift of the $V_{FB}$ and increased the $J_g$ considerably to 1 $\times$ $10^{-3}$ $A/cm^2$ at ($V_{FB}$ + 1) V after 600°C PDA; these behaviors are possibly correlated with the degree of GeO volatilization. As far as the positive $V_{FB}$ shift after thermal annealing is concerned, the desorption process of GeO is believed to generate additional negative charges and leads to charge neutralization. Bai et al. have examined that an increase of PMA temperature made the value of $V_{FB}$ shift positively and they interpreted this phenomenon in terms of the out-diffusion of $GeO_x$ from Ge substrate.[31] Another result demonstrated further by Wu et al. was that the thicker the Si layer capping onto Ge substrate is, the smaller the amount of Ge out-diffusion is. Accordingly, a less positive $V_{FB}$ shift was found owing to the reduction of these negative charges.[32] Furthermore, more severe out-diffusion of GeO was seen upon increasing annealing temperature; this in turn caused the high-*k*/Ge interface degradation.[22] This tendency is obviously different from that observed in the Pt/$HfO_xN_y$/Si capacitors which depict the reduction in $J_g$ upon increasing PDA temperature. We thus suggest that the $GeO_x$ incorporation into the overlying $HfO_xN_y$ bulk film may form the leakage path and contribute to gate leakage current, especially after annealing at 600°C.

*Influence of $NH_3$ plasma passivation on high-k/Ge MIS properties*.— Most studies have demonstrated that the gate leakage current in high-*k*/Ge systems decreases significantly after receiving surface thermal-annealing in a $NH_3$ ambient, especially prior to the deposition of $HfO_2$ dielectric films.[33] We observed similar effects after $NH_3$ plasma, as presented in the inset of Fig. 6. The gate leakage

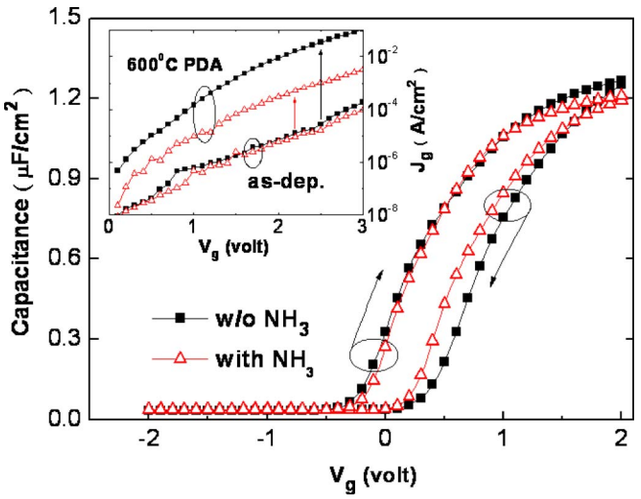


**Figure 6.** (Color online) Bidirectional sweep (1 MHz) *C-V* curves of Pt/$HfO_xN_y$/n–Ge capacitors prepared (■) without and (△) with $NH_3$ nitridation. The inset displays the corresponding plots of $J_g$ vs $V_g$ before and after PDA at 600°C.

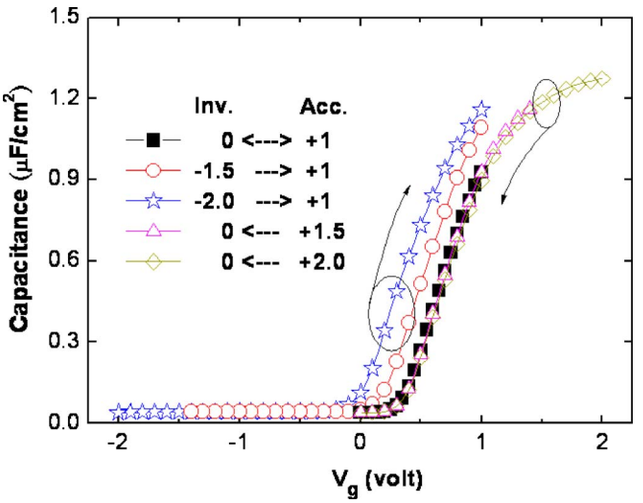


**Figure 7.** (Color online) Dependence of the hysteresis width in *C-V* (1 MHz) sweep on the starting accumulation and inversion gate biases; the absence of the hysteresis behavior in the gate-bias ranged from 0 to 1 V.

was lower after higher-temperature PDA for the $NH_3$-treated sample relative to that of the HF-last sample. Moreover, plasma treatment reduced the hysteresis loop in the bidirectional *C-V* curves measured at 1 MHz (Fig. 6); reduction of the interface state density to the order of $10^{11}$ cm$^{2.}$ eV$^{-1}$ was also achieved. We obtained a corresponding value of $N_{\text{eff}}$ of ca. $4.8 \times 10^{12}$ cm$^{-2}$ for HF-last sample and it decreased to ca. $2.5 \times 10^{12}$ cm$^{-2}$ after surface nitridation. It was believed that substoichiometric oxide may create a high density of charge-trapping sites at the dielectric-substrate and they could induce charge trapping and detrapping. The formation of Ge–N chemical bonds and the inhibited growth of $GeO_x$ ($x \leqq 2$) may be responsible for the resulting improved electrical performance. The interposed $GeO_xN_y$ IL may behave as a diffusion barrier and suppress the volatilization of GeO out-diffusion from Ge substrate; therefore, causing a less significant increase in $J_g$ after $NH_3$ plasma pretreatment.

On the other hand, to obtain a deeper insight into the origin of the hysteresis behavior, we separately extended the inversion and accumulation biases in the *C-V* sweeps and found that the increased inversion bias did lead to an increased hysteresis width, but the increased accumulation bias did not, as is evident in Fig. 7. This fact implies that hole trapping is the dominant mechanism; the scheme of a charge trapping model for a Pt/$HfO_xN_y$/$GeO_x$/Ge gate stack has been proposed in other studies.[34] We conclude that the minority carriers (in this case, holes for n-type Ge) tunnel from the Ge substrate and become trapped at the inner-interface and/or inside the deficient $GeO_x$ interlayer. This process causes the *C-V* curve to shift negatively with the deviation of the $V_{\text{FB}}$ when the sweeping bias is started further from the negative side, i.e, more inversion charges are trapped. In contrast, the *C-V* curve exhibits its own value of $V_{\text{FB}}$ without being trapped when the voltage is swept from accumulation to inversion.

*XPS analysis of Ge interface chemistry through $NH_3$ plasma nitridation.*— In Fig. 8 and 9 we investigate the distribution of GeO species in entire structures through analyses of the Ge 2p3 and Ge 3p core levels, a broad band consisting of Ge dioxides and suboxides and elemental Ge. We compared the spectra of these two Ge photoemissions because they allow sampling at significantly different depths. We employed mixed Gaussian-Lorentzian line shapes to reproduce these two Ge core levels from three components, Ge, GeO, and $GeO_2$. From the high-surface-sensitivity Ge 2p3 spectrum (Fig. 8), a quite high intensity ratio of the $GeO_2$ and GeO to the Ge substrate was found for both samples; this feature arose primarily from the surface contamination of $GeO_x$ ($x \leqq 2$). The average Ge concentration estimated within the top of high-*k* bulk layer is ca. 12(±1.4) atom % for HF-last sample; with the value can be reduced to ca. 4.8 atom % providing that the Ge substrate receives surface pretreatment of $NH_3$ plasma. Subsequently annealing the $NH_3$ sample at 600°C for 30 s causes the Ge concentration increasing to the value of ca. 14 atom %. From the concentration levels, we found that $NH_3$ pretreatment did assist to minimize Ge incorporation behavior during annealing with respect to the result obtained in HF-last sample that the Ge contamination was up to ca. 19.3(±2) atom % after annealing at 500°C for 5 min. However, we suggest that the finite improvements in characteristics of $NH_3$-treatment samples as compared to the literatures[14,32] using another passivation technique, the Si interlayer on Ge, can be attributed to the incomplete passivation of the dangling bonds on the Ge surface; such a surface would not fully diminish the formation of $GeO_x$. Lower dissociated tem-

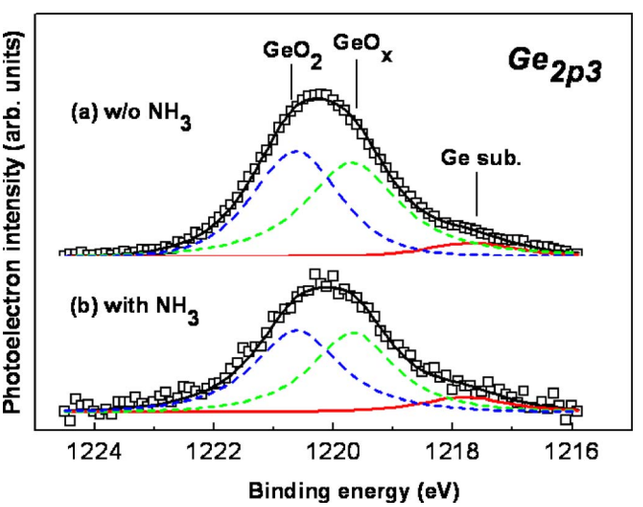


**Figure 8.** (Color online) Ge 2p3 XPS spectra of Pt/$HfO_xN_y$/n–Ge capacitors prepared without and with $NH_3$ nitridation. Three components were extracted: Ge, $GeO_x$, and $GeO_2$.

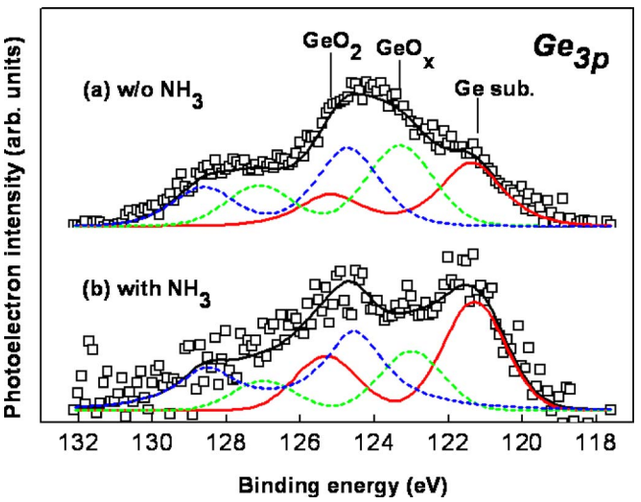


**Figure 9.** (Color online) Ge 3p XPS spectra of Pt/$HfO_xN_y$/n–Ge capacitors prepared without and with $NH_3$ nitridation. Three components were extracted: Ge, $GeO_x$, and $GeO_2$.

perature (ca. 500°C) of Ge–N bonds[35] is a major cause to result in a still higher concentration of Ge observed after high-temperature processing.

In contrast, the Ge 3p spectrum (Fig. 9) clearly demonstrated that the intensity from the $GeO_x$ ($x \leqq 2$) was lower than that from the substrate after $NH_3$ plasma nitridation, especially for inhibiting a large amount of Ge suboxides; these phenomena are the opposite of that observed for the non-nitrided high-*k*/Ge sample. Our explanation for this experimental finding is that the Ge 3p core level is capable of examining the amount of Ge oxide existing at the high-*k*/Ge interface because it possesses a higher sampling depth (ca. 80 Å) relative to that (ca. 34 Å) of the Ge 2p3 spectrum.[36] Accordingly, such a low oxide/substrate emission ratio after performing the nitridation process is a direct result of $NH_3$ plasma pretreatment diminishing the number of $GeO_x$ ($x \leqq 2$) defects at the interface; in other words, the reduced charge trapping centers is achieved. These results also imply that surface nitridation does indeed assist in enhancing the thermal stabilities of Pt/$HfO_xN_y$/Ge MOS structures.

## Conclusions

In this study, we performed the physical and electrical analyses to systematically examine the $HfO_xN_y$ thin films sputtered on Ge substrates and the admittance properties of their MIS capacitors. We observed a U-shaped distribution of Ge atoms into the overlying $HfO_xN_y$ dielectric and an increased Ge incorporation (>17 atom %) after higher thermal processing. Although high-temperature annealing did improve the interface qualities, they also caused a positive shift of the $V_{FB}$, severe charge trapping, and increased $J_g$ considerably; which are closely related to the existence of $GeO_x$ defective layer and the degree of resultant GeO desorption. These problems could be relieved after performing $NH_3$ plasma pretreatment on the Ge surface; in particular, suppressing the amount of Ge incorporation (<5 atom %) and the substoichiometric oxide at dielectric–substrate interface. We suggested that the surface nitridation process indeed diminished the volatilization of gaseous GeO and enhanced the thermal stability of the high-*k*/Ge interface. Additionally, we measured a high loss in the parallel conductance in the inversion region and it revealed gate-bias independence, implying the fast generation rate of minority carriers in Ge through either a diffusion mechanism or bulk traps within the substrates.

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## References

1. R. Li, S. J. Lee, H. B. Yao, D. Z. Chi, M. B. Yu, and D. L. Kwong, *IEEE Electron Device Lett.*, **27**, 476 (2006).
2. Y.-L. Chao and J. C. S. Woo, Abstract 1052. Extended Abstrects of the International Conference Solid State Devices and Materials (2006).
3. A. Ritenour, S. Yu, M. L. Lee, N. Lu, W. Bai, A. Pitera, E. A. Fitzgerald, D. L. Kwong, and D. A. Antoniadis, *Tech. Dig. - Int. Electron Devices Meet.*, **2003**, 433.
4. C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho , M.-F. Li, and D. L. Kwong, in *Technical Digest of the Symposium. VLSI*, p. 119 (2003).
5. http://public.itrs.net
6. O. Weber, F. Andrieu, M. Cass, T. Ernst, J. Mitard, F. Ducroquet, J.-F. Damlencourt, J.-M. Harmann, D. Lafond, A.-M. Papon, L. Militaru, L. Thevenod, K. Romanjek, C. Leroux, F. Martin, B. Guillaumot, G. Ghibaudo, and S. Deleonibus, *Tech. Dig. - Int. Electron Devices Meet.*, **2004**, 867.
7. C. S. Kang, H.-J. Cho, K. Onishi, R. Choi, R. Nieh, S. Gopalan, S. Krishnan, and J. C. Lee, in *Technical Digest of the Symposium, VLSI*, p. 146 (2002).
8. H. C.-H. Wang, C.-W. Tsai, S.-J. Chen, C.-T. Chan, H.-J. Lin, Y. Lin, H.-J. Tao, S.-C. Chen, C. H. Diaz, T. Ong, A. S. Oates, M.-S. Liang, and M.-H. Chi, in *Technical Digest of the Symposium, VLSI*, p. 170 (2005).
9. A. L. P. Rotondaro, M. R. Visokay, J. J. Chambers, A. Shanware, R. Khamankar, H. Bu, R. T. Laaksonen, L. Tsung, M. Douglas, R. Kuan, M. J. Bevan, T. Grider, J. Mcpherson, and L. Colombo, in *Technical Digest of the Symposium, VLSI*, p. 148 (2002).
10. T. Yamaguchi, R. Iijima, T. Ino, A. Nishitama, H. Satake, and N. Fukushima, *Tech. Dig. - Int. Electron Devices Meet.*, **2002**, 621.
11. M. Houssa, T. Conard, F. Bellenger, G. Mavrou, Y. Panayiotatos, A. Sotiropoulos, A. Dimoulas, M. Meuris, M. Caymax, and M. M. Heynsa, *J. Electrochem. Soc.*, **153**, G1112 (2006).
12. S. Zhu, R. Li, S. J. Lee, M. F. Li, A. Du, J. Singh, C. Zhu, A. Chin, and D. L. Kwong, *IEEE Electron Device Lett.*, **26**, 81 (2005).
13. N. Lu, W. Bai, A. Ramirez, C. Mouli, A. Ritenour, M. L. Lee, D. Antoniadis, and D. L. Kwong, *Appl. Phys. Lett.*, **87**, 051922 (2005).
14. N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, A. Du, N. Balasubramanian, M. F. Li, A. Chin, and J. K. O. Sin, *IEEE Electron Device Lett.*, **25**, 631 (2004).
15. C.-C. Cheng, C.-H. Chien, C.-W. Chen, S.-L. Hsu, C.-H. Yang, and C.-Y. Chang, *J. Electrochem. Soc.*, **153**, F160 (2006).
16. W. H. Wu, B. Y. Tsui, Y. P. Huang, F. C. Hsieh, M. C. Chen, Y. T. Hou, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang, *IEEE Electron Device Lett.*, **27**, 399 (2006).
17. H.-T. Lue, C.-Y. Liu, and T.-Y. Tseng, *IEEE Electron Device Lett.*, **23**, 553 (2002).
18. M.-K. Lee, C.-F. Yen, J.-J. Huang, and S.-H. Lin, *J. Electrochem. Soc.*, **153**, F266 (2006).
19. D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed., 368, John Wiley & Sons, Inc., New York (1998).
20. W. A. Hill and C. C. Coleman, *Solid-State Electron.*, **23**, 987 (1980).
21. Q. Zhang, N. Wu, D. M. Y. Lai, Y. Nikolai, L. K. Bera, and C. Zhu, *J. Electrochem. Soc.*, **153**, G207 (2006).
22. C.-C. Cheng, C.-H. Chien, J.-H. Lin, C.-Y. Chang, G.-L. Luo, C.-H. Yang, and S.-L. Hsu, *Appl. Phys. Lett.*, **89**, 012905 (2006).
23. P. M. Lambert, *Inorg. Chem.*, **37**, 1352 (1998).
24. V. V. Afanas'ev, Y. G. Fedorenko, and A. Stesmans, *Appl. Phys. Lett.*, **87**, 032107 (2005).
25. C. O. Chui, F. Ito, and K. C. Saraswat, *IEEE Trans. Electron Devices*, **53**, 1501 (2006).
26. D. Flandre, F. Campabadal, J. Esteve, E. Lora-Tamayo, and F. V. D. Wiele, *J. Appl. Phys.*, **70**, 5111 (1991).
27. E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*, John Wiley & Sons, Inc., New York (1982).
28. Y. Fukuda, T. Ueno, and S. Hirono, *Jpn. J. Appl. Phys., Part 1*, **44**, 7928 (2005).
29. Y. Fukuda, T. Ueno, S. Hirono, and S. Hashimoto, *Jpn. J. Appl. Phys., Part 1*, **44**, 6981 (2005).
30. A. Dimoulas, G. Vellianities, G. Mavrou, E. K. Evangelou, and A. Sotiropoulos, *Appl. Phys. Lett.*, **86**, 223507 (2005).
31. W. P. Bai, N. Lu, and D.-L. Kwong, *IEEE Electron Device Lett.*, **26**, 378 (2005).
32. N. Wu, Q. Zhang, D. S. H. Chan, N. Balasubramanian, and C. Zhu, *IEEE Electron Device Lett.*, **27**, 479 (2006).
33. N. Wu, Q. Zhang, C. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D.-L. Kwong, A. Y. Du, C. H. Tung, and N. Balasubramanian, *Appl. Phys. Lett.*, **84**, 3741 (2004).
34. C.-C. Cheng, C.-H. Chien, G.-L. Luo, C.-H. Yang, M.-L. Kuo, J.-H. Lin, and C.-Y. Chang, *Appl. Phys. Lett.*, **90**, 012905 (2007).
35. K. Prabhakaran and T. Ogino, *Surf. Sci.*, **387**, L1068 (1997).
36. NIST Electron Inelastic-Mean-Free-Path Database 71 (Version 1.1), National Institute of Standards and Technology (2000).