



Performance Improvement of CoTiO₃ High-*k* Dielectrics with Nitrogen Incorporation

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In this paper, three approaches to incorporating nitrogen in CoTiO₃ high-*k* dielectric films, ion implantation of N₂⁺, ion implantation of N⁺, and N₂O plasma treatment have been investigated for the new CoTiO₃ high-*k* dielectrics. All three methods reduced the leakage currents and improved the breakdown characteristics but the N₂O-plasma treatment produced the best-behaved C-V curves, when compared to the untreated control samples.

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The thickness of the conventional silicon dioxide (SiO₂) gate dielectrics has been scaled down to around 1.5 nm to meet the high drive requirements of high-performance (CMOS).¹ The most serious problem we face today for this ultrathin gate dielectric is the huge gate leakage due to the direct tunneling of carriers from the channel of metal oxide semiconductor field-effect transistors (MOSFETs),² which reduces the transconductance of devices, and increases the standby power. This is not adequate for low-power applications in portable equipment. For a long time, high dielectric constant (high-*k*) gate materials such as Si₃N₄,^{3,4} Al₂O₃,⁵⁻⁷ HfO₂,⁸⁻¹⁰ and ZrO₂¹¹⁻¹³ have been proposed to replace the conventional ultrathin SiO₂ to solve this problem. For the same equivalent-oxide-thickness (EOT), the thickness of high-*k* gate dielectrics can be increased many times. Hence, the direct tunneling current can be significantly reduced. The choice of high-*k* material is based on the following requirements:

1. The *k*-value should be in the range 20-50, as high as possible but low enough to avoid the fringing-induced barrier lowering effect in sub-100 nm nMOSFETs.¹⁴
2. The bandgap energy should be larger than 4.5 eV and barrier height larger than 1 eV to avoid increased leakage current at elevated temperature.^{15,16}
3. The interface state density should be less than 10¹¹ cm⁻² eV⁻¹ to maintain a well-behaved subthreshold characteristic.
4. Low trap densities are required in the film to avoid Frankel-Poole tunneling.
5. The dielectric should have good thermal stability during the high-temperature processing.
6. It should have high breakdown voltage, low-leakage, and low hysteresis. In our previous paper, a new high-*k* dielectric CoTiO₃ has been proposed for application in MOSFETs and dynamic random access memories (DRAMs).¹⁷ The dielectric constant for this CoTiO₃ with the bottom oxide layer can be as high as 50, which makes this high-*k* dielectric become very promising after the current medium *k* value (15-25) materials, such as HfO₂ and ZrO₂, have reached their useful limit. However, some issues still remain when high-*k* materials are used. The most important issues are:

1. The interfacial layer of SiO₂ or silicate remaining after deposition of high-*k* materials.
2. The high fixed charge in the bulk of high-*k* dielectrics which results in flabband voltage (*V*_{FB}) shifts.
3. The degradation of mobility.

4. A low crystallization temperature.

5. Boron penetration for pMOSFETs. According to recent reports,¹⁸⁻³² optimized treatments which incorporate nitrogen have resulted in a significant improvement in the high-*k* dielectric properties. Nitridation of the silicon surface can reduce the growth of an interfacial layer. Plasma nitridation after deposition of the high-*k* dielectric can recover the degradation of mobility. The advantages of nitrogen incorporation are the increase of the *k*-value, the increase of the temperature of crystallization, the reduction of the leakage, reasonable *V*_{FB}, and reduced boron penetration.¹⁸⁻³¹ Because we have investigated the material and electrical properties in Ref. 33 and 34, in this paper, nitrogen incorporation using N₂⁺/N⁺ ion implantation or N₂O plasma treatment to improve this CoTiO₃ films investigated. We found that the nitrogen incorporation by either ion implantation or plasma treatment can be used to significantly improve the electrical performance of CoTiO₃ high-*k* dielectrics.

Experimental

Capacitors were fabricated on n-type 150 mm Si(100) wafers with a resistivity of 2-7 Ω cm. After the growth of a 550 nm thick field oxide, the active region of capacitors were defined and etched by buffered oxide etch (BOE, NH₄F: HF = 6:1). Wafers underwent a RCA standard cleaning process and were put into the low-pressure chemical vapor deposition (LPCVD) tube in a pure NH₃ ambient to grow an ultrathin nitride ~1.0 nm thick on the Si surface. The thickness of the nitride was measured by ellipsometry. The purpose of this NH₃-grown ultrathin nitride film is to prevent the reaction of the following sputtered Ti and then Co (Co/Ti) metal films, and also to retard the oxidation of silicon during the oxidation of Co/Ti layer. The Ti (5 nm) and Co (5 nm) films were deposited by sputtering at a power of 500 W, and a sputtering rate was of 0.9 nm/s. Then wafers underwent the N₂⁺ or N⁺ ion implantation. To avoid the nitrogen penetration through the metal films and to reduce damage of the metal films, a low ion energy of 10 keV was used with nitrogen doses of 2 × 10¹⁴ and 2 × 10¹⁵ atom/cm². Wafers were then oxidized in the furnace using flows of 5000 sccm each of O₂ and N₂. Splits were done for oxidation temperatures of 800, 850, and 900°C, and the oxidation time was 10 min. Some wafers without nitrogen implantation underwent N₂O plasma treatment in a plasma enhanced chemical vapor deposition (PECVD) system. The flow rate of N₂O was 60 sccm, the temperature was 350°C, the power was set at 10, 15, or 20 W, and the processing time was 5 min. The purpose of this N₂O plasma treatment is to passivate the oxygen vacancies in the bulk film, and also to incorporate nitrogen in the dielectrics. The top electrode for electrical measurements was a 500 nm Al film which was deposited by physical vapor deposition (PVD). The capacitance voltage (C-V) curves of the capacitors were measured

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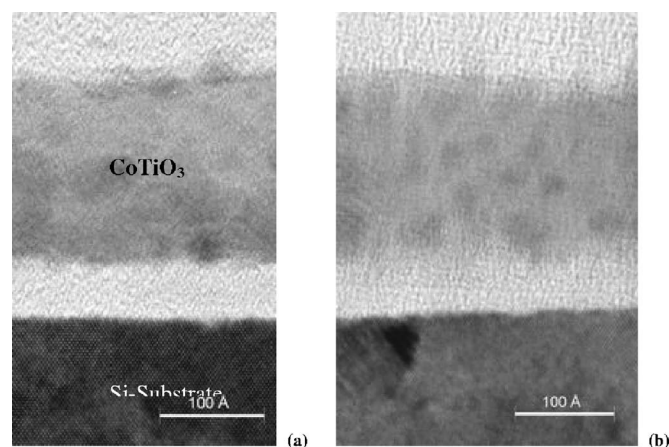


Figure 1. TEM pictures for samples of CoTiO₃ oxidized at 800°C for 10 min (a) without and (b) with nitrogen ion implantation.

with a HP 4284 impedance meter at 100 kHz. The areas of the capacitors were $2.5 \times 10^{-5} \text{ cm}^2$ ($50 \times 50 \text{ }\mu\text{m}$) and $1 \times 10^{-4} \text{ cm}^2$ ($100 \times 100 \text{ }\mu\text{m}$). The current-voltage (I - V) curves were measured using a HP 4156 parameter analyser. The properties of high- k dielectrics with and without nitrogen incorporation were analyzed by transmission electron microscopy (TEM), secondary-ion mass spectrometry (SIMS), and X-ray diffraction (XRD).

Results and Discussion

The thickness of all CoTiO₃ samples was first measured by TEM. Figure 1a and b show one set of the TEM pictures for samples of CoTiO₃ oxidized at 800°C for 10 min without and with nitrogen ion implantation, respectively. The physical thickness of both samples was in the range 24–25 nm. It was observed that the oxidation of the Ti/Co films increases the thickness of the interfacial layer. This indicates that the ultrathin nitride film was not thick enough to retard the diffusion of oxygen. Compared with the sample without nitrogen implantation, smaller grains and a less diffuse boundary profile between high- k and interfacial layers were found for the N₂⁺-implanted sample. C- V curves at a high frequency of 100 kHz are shown in Fig. 2. The C- V curves for samples oxidized at 800°C for 10 min without nitrogen implantation were not obtained due to a large leakage current during measurement. This may be due to the nonfully oxidized Co/Ti in the bulk of dielectrics at

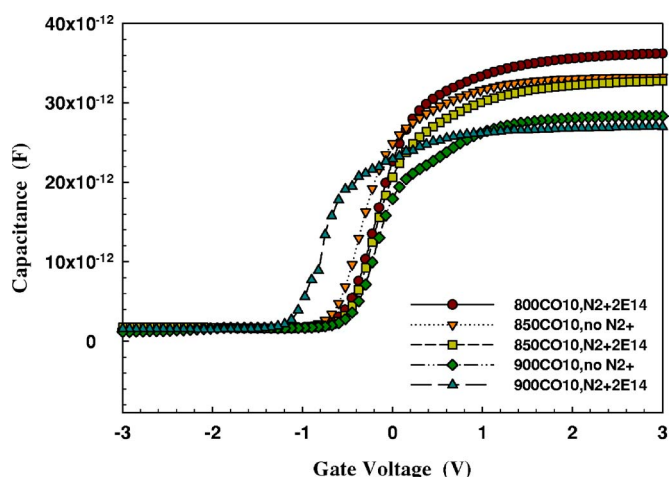


Figure 2. (Color online) High-frequency C- V curves measured at 100 kHz for all samples oxidized at 800, 850, and 900°C with or without nitrogen implantation.

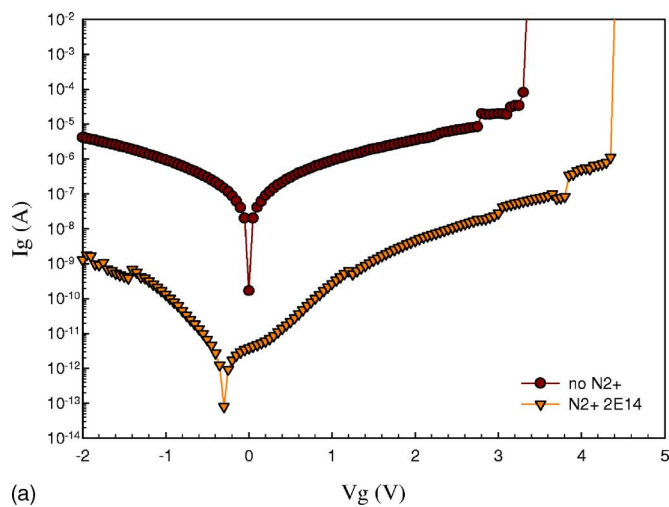
Table I. The resultant equivalent-oxide-thickness (EOT), interface layer, CoTiO₃ dielectric thickness, total thickness, effective k -value, and flatband voltage for all samples.

	EOT (Å)	Interface layer (Å)	Dielectric film (Å)	Total film (Å)	Effective k -value	Flatband voltage (V)
800 N2+	21.9	58.8	188.2	247.0	43.9	0.3
850 no	25.4	85.7	128.6	214.3	32.9	0.15
850 N2+	27.2	66.7	176.2	242.9	34.8	0.38
900 no	30.3	82.4	155.9	238.2	30.6	0.45
900 N2+	29.4	90.0	153.3	243.3	32.2	-0.23

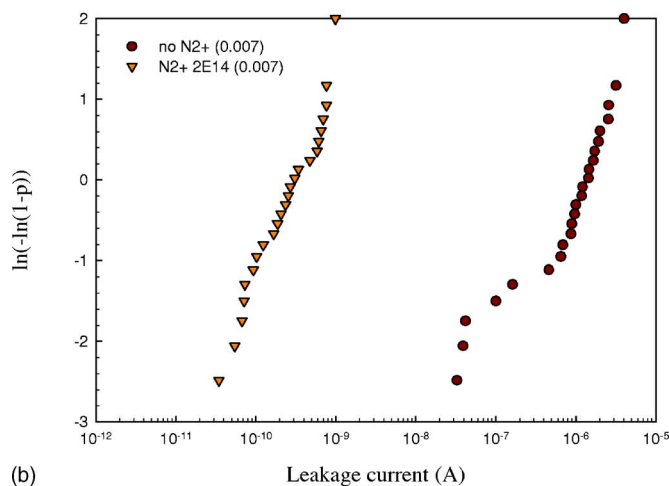
lower temperature for a short oxidation time of 10 min. It was found that the accumulation of $C_{ox}C_{ox}$ decreases as the oxidation temperature was increased due to abundant oxygen incorporation during the oxidation step. The extract equivalent-oxide-thickness (EOT), interfacial silicate thickness, high- k dielectric thickness, total thickness, effective k -value and flatband voltage are compiled and shown in Table I. The existing interfacial layer degrades the effective k -value. However, in Ref. 17 we have estimated the intrinsic bulk dielectrics constant for CoTiO₃ under the same processes. The intrinsic bulk dielectric constant was estimated as high as 50, excluding the interfacial layer. It was found that the EOT increases as the oxidation temperature increased. As a result, the effect k -value deduced from the result of C- V and TEM measurements decreases as the temperature is increased. The flatband voltage shifts to a negative value for the sample oxidized at 900°C with nitrogen implantation. This may be due to nitrogen diffusion into the interfacial layer which creates positive charges in the film. Figure 3 shows the electrical properties for samples oxidized at 900°C for 10 min. Figure 3a shows that capacitors with nitrogen ion implantation exhibit a lower leakage current and high breakdown voltage. This phenomenon is the same for samples with 800° and 850°C oxidation. Figure 3b shows the Weibull distribution of gate leakage current at $V_g = 1 \text{ V}$. Capacitors with nitrogen implantation have a tighter distribution and smaller leakage than those without. Figure 3c shows the Weibull distribution of breakdown voltage for two samples. Once again, the capacitors with nitrogen implantation have higher breakdown voltage than the ones without. The two samples were also subjected to constant voltage ($V_g = 2 \text{ V}$) stress and the results are shown in Fig. 4a and b. For the capacitors without nitrogen implantation, a significant increase of gate leakage was found when the stress time was increased to 100 s compared with the implanted samples. On the other hand, the samples with nitrogen implantation exhibited no significant increased gate leakage when compared to the capacitor without nitrogen implantation. The X-ray diffraction spectrum is shown in Fig. 5 for a CoTiO₃ film oxidized at 850°C with and without nitrogen implantation. For the sample without nitrogen implantation, a clear peak intensity was found around 34° for CoTiO₃ (311) but the peak is not so clear for the sample with nitrogen implantation. This implies that the nitrogen implantation of the Ti/Co films can retard the crystallization of CoTiO₃.

To reduce the damage from the nitrogen ion implantation, two approaches were adopted. The first approach was to reduce the mass of implanted species by using N⁺ instead of N₂⁺. Figure 6a shows the result. The oxidation temperature was 850°C with a reduced oxidation time of 5 min. This can reduce the oxygen encroachment during the high temperature oxidation. The leakage current decreased as the nitrogen dose increased. The Weibull distributions of gate leakage current and breakdown voltage are shown in Fig. 6b and c, respectively. It can be seen that high nitrogen doses improve the electrical properties of the capacitors.

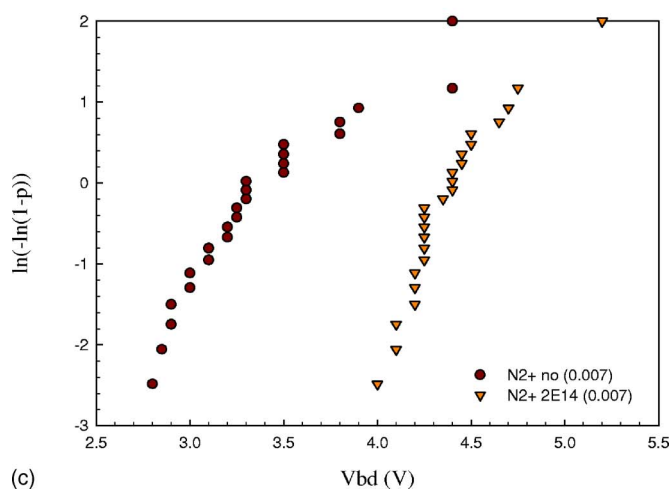
The second approach to avoid the damage from ion implantation was generally to use the N₂ plasma treatments³⁴⁻³⁶ or post-deposition annealing (PDA) in nitrogen ambient, such as N₂, NO, N₂O, or HH₃.^{37,38} In this work, we use N₂O plasma treatment (at



(a)



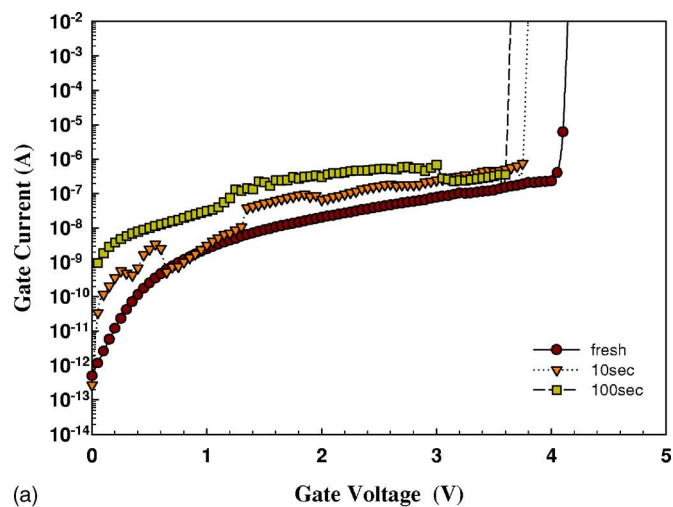
(b)



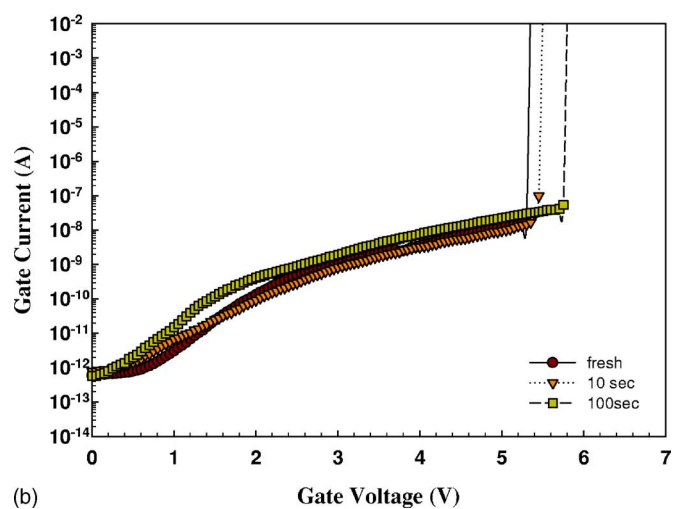
(c)

Figure 3. (Color online) I - V curves of samples oxidized at 900°C for 10 min with and without nitrogen implantation. (a) Gate voltage vs gate leakage current. (b) Weibull distribution of gate leakage current at $V_g = 1$ V. (c) Weibull distribution of breakdown voltage.

powers of 10, 15, and 20 W) after the oxidation step. Some samples without nitrogen ion implantation underwent the N_2O plasma treatment before metal deposition. This treatment can passivate the oxygen vacancies (radical of oxygen in N_2O plasma) in the dielectric



(a)



(b)

Figure 4. (Color online) The I - V curves for samples oxidized at 850°C for 10 min (a) without and (b) with nitrogen implantation after constant voltage stress at $V_g = 2$ V for 100 s.

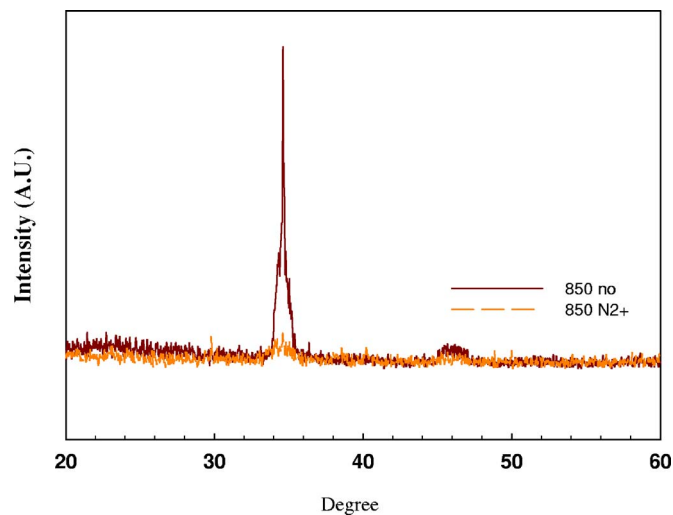
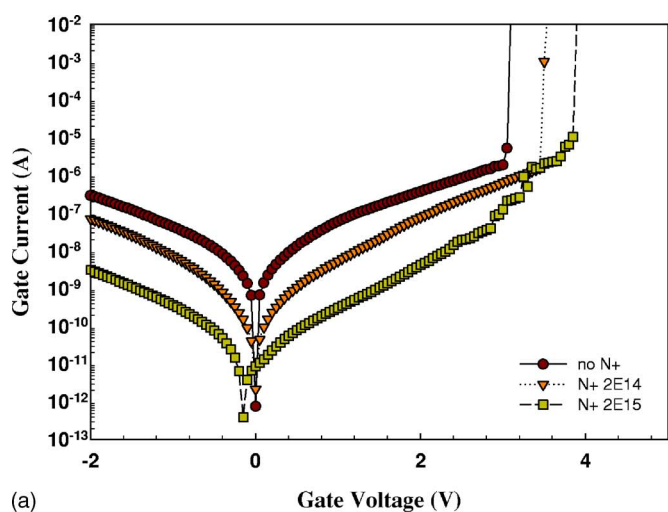
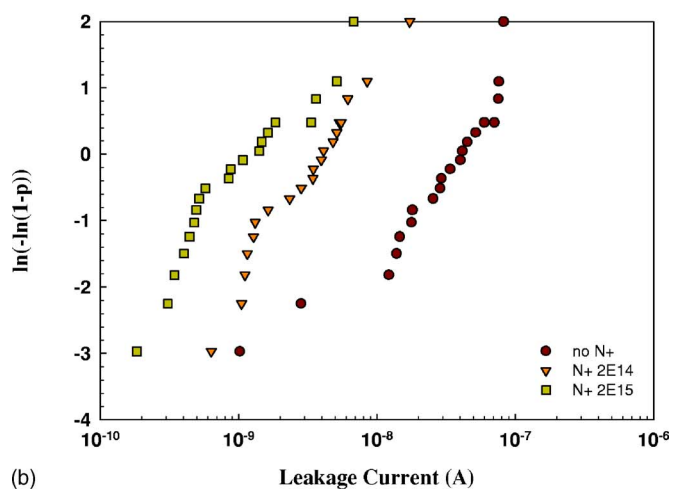


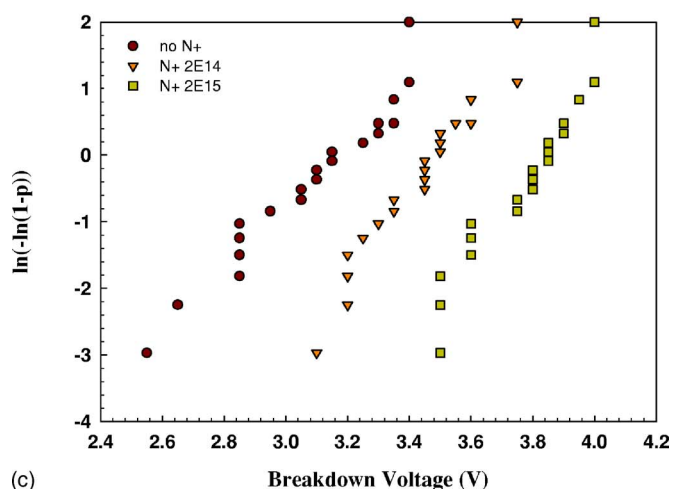
Figure 5. (Color online) XRD spectrum for a $CoTiO_3$ film oxidized at 850°C with and without nitrogen implantation.



(a)



(b)



(c)

Figure 6. (Color online) Electrical measurements for samples oxidized at 850°C for 5 min with and without N⁺ ion implantation. (a) Gate current vs gate voltage. (b) Weibull distribution of gate leakage at $V_g = 1$ V. (c) Weibull distribution of breakdown voltage.

bulk and also introduce nitrogen (radical of nitrogen in N₂O plasma) in the bulk. Figure 7 shows the SIMS profile for samples with N₂O plasma treatment (20 W). We found that nitrogens pile up at the high-*k*/Si interface using N₂O plasma. This profile is different from

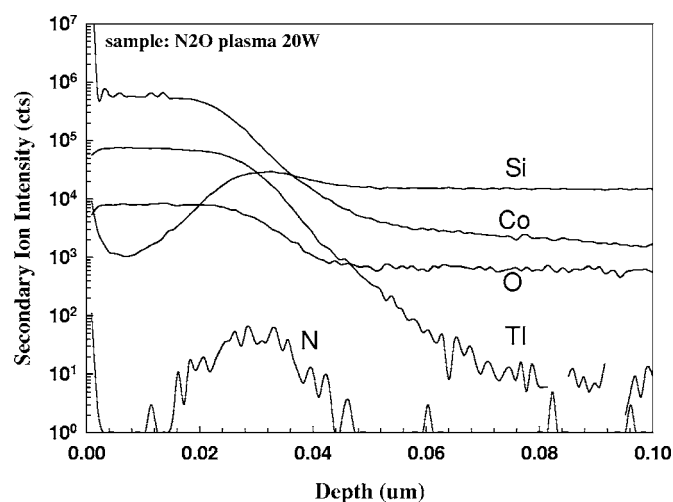


Figure 7. SIMS profiles for samples with 20 W N₂O plasma treatment.

the report using N₂ plasma in which the nitrogen was diffused uniformly into the bulk after annealing at 700°C.³⁶ However, this result is similar to the resultant nitrogen profile in ultrathin gate oxide (or oxy-nitride) formed by N₂O oxidation or annealing.³⁹ Another advantage using N₂O plasma instead of N₂ plasma is the oxygen radical introduced in the bulk high-*k* film. The oxygen profiles for all samples were measured and shown in Fig. 8. It is clear that the sample with N₂O plasma treatment exhibited an increased oxygen concentration compared to that the without one. From the previous report,²⁹ leakage current of high-*k* dielectrics with nitrogen incorporation can be significantly reduced by 3-4 orders of magnitude. Recently, it has been widely accepted that the reason for leakage current reduction by nitrogen incorporation is due to that nitrogen anneals oxygen vacancies.^{37,38} As a result, the increase of oxygen by the N₂O plasma treatment is also helpful to reduce the oxygen vacancy in high-*k* dielectrics.^{34-38,40} The electrical results for all samples with or without N₂O plasma treatment are shown in Fig. 9. Figure 9a shows the C-V curves for all samples. All capacitors with the N₂O plasma treatment have better-behaved C-V curves than that those without. This implies that the interfacial property has been improved by this N₂O plasma treatment.⁴¹ The accumulation capacitance C_{ox} of all N₂O plasma treatment capacitors is higher than on the C_{ox} of those

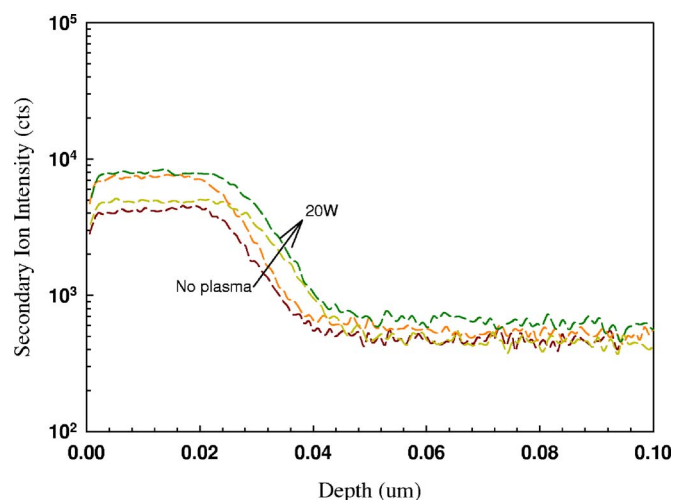


Figure 8. (Color online) The oxygen profiles for samples without N₂O plasma or with N₂O plasma treatment using powers of 10, 15, and 20 W.

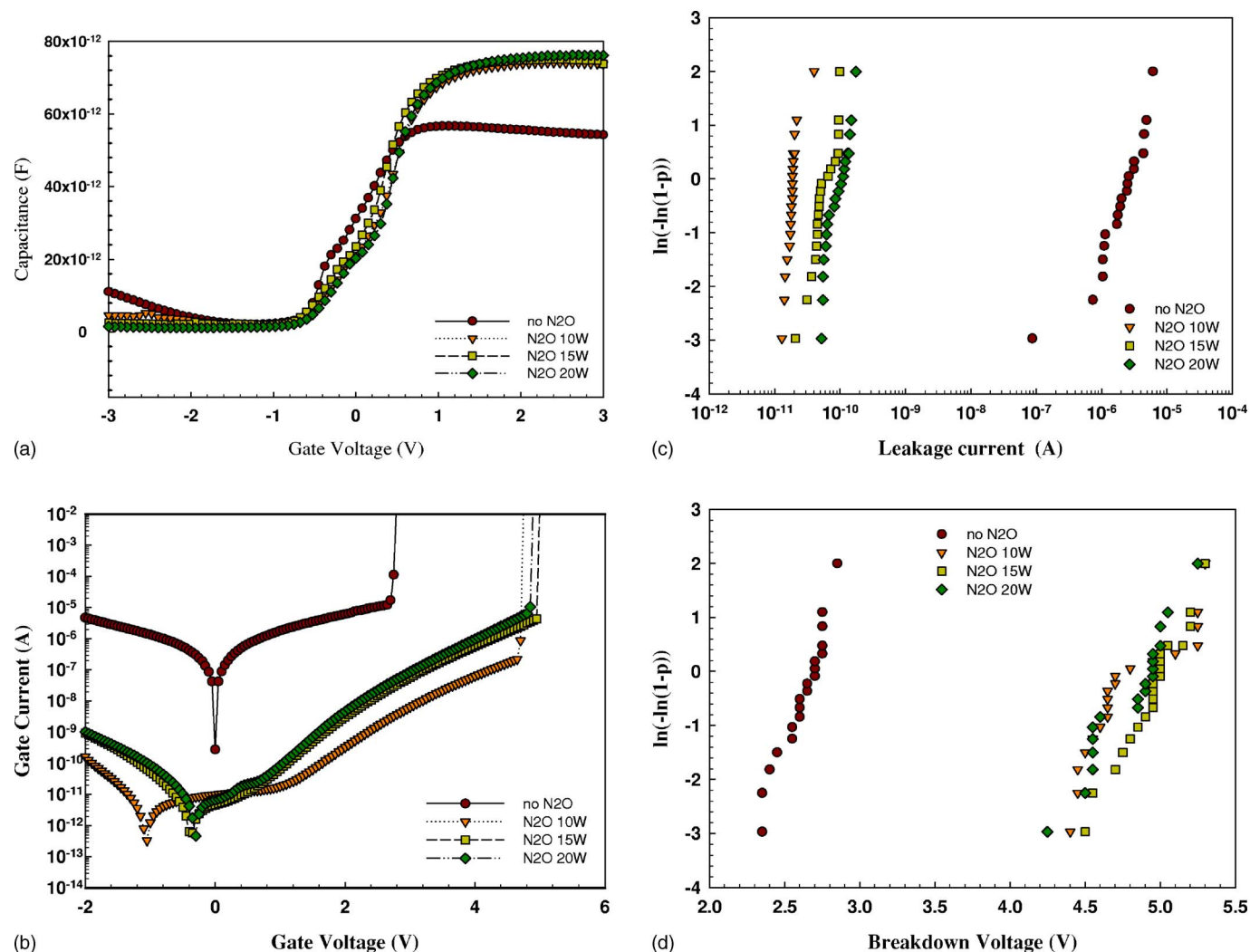


Figure 9. (Color online) (a) C-V curves for all samples with and without N₂O plasma treatment. (b) Gate leakage current vs gate voltage. (c) The Weibull distribution of gate leakage current at V_g = 1 V. (d) The Weibull distribution of breakdown voltage.

without. This is due to the passivation of oxygen and nitrogen, resulting in a good interface of the dielectrics with the silicon substrate. Figure 9b shows the gate leakage. The N₂O plasma-treated sample shows a great improvement compared with the untreated sample. The Weibull distribution of gate leakage and breakdown voltage are shown in Fig. 9c and d, respectively. Capacitors with N₂O plasma treatment demonstrate much lower gate leakage currents and higher breakdown voltages.

Conclusions

We have investigated three approaches to nitrogen incorporation for the new CoTiO₃ high-*k* dielectrics. Nitrogen (N₂⁺) incorporation by ion implantation can improve the electrical properties in terms of gate leakage, breakdown voltage, and T_{BD}. To reduce the mass of ion implanting species, N⁺ ion implantation has been used. The same trends can be found as those produced using N₂⁺. Higher doses of N⁺ can improve the performance further. An alternative N₂O plasma treatment was also an excellent method to improve the electrical properties, exhibiting better-behaved C-V curves, lower gate leakage currents, and higher breakdown voltages compared with the untreated samples.

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References

1. Y. Taur, *IBM J. Res. Dev.*, **46** 213 (2002).
2. S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, *IEEE Electron Device Lett.*, **18**, 209 (1997).
3. K. Sekine, Y. Saito, M. Hirayama, and T. Ohmi, *IEEE Trans. Electron Devices*, **47**, 1370 (2000).
4. M. Khare, G. Xin, X. W. Wang, T. P. Ma, G. J. Cui, T. Tamagawa, B. L. Halpern, and J. J. Schmitt, *VLSI Technology*, p. 51 (1997).
5. C. S. Kuo, J. F. Hsu, S. W. Huang, L. S. Lee, M. J. Tsai, and J. G. Hwu, *IEEE Trans. Electron Devices*, **51**, 854 (2004).
6. D. S. Yu, C. H. Huang, A. Chin, Z. Chunxiang, M. F. Li, B. J. Cho, and D. L. Kwong, *IEEE Electron Device Lett.*, **25**, 138 (2004).
7. L. Manchanda, W. H. Lee, J. E. Bower, F. H. Baumann, W. L. Brown, C. J. Case, R. C. Keller, Y. O. Kim, E. J. Laskowski, M. D. Morris, R. L. Opila, P. J. Silverman, T. W. Sorsch, and G. R. Weber, *Tech. Dig. - Int. Electron Devices Meet.*, **1998**, 605.
8. H. Y. Yu, M. F. Li, and D. L. Kwong, *IEEE Trans. Electron Devices*, **51**, 609 (2004).
9. J. Lu, Y. Kuo, and J. Y. Tewg, *J. Electrochem. Soc.*, **153**, G410 (2006).
10. W. J. Zhu, T. P. Ma, S. Zafar, and T. Tamagawa, *IEEE Electron Device Lett.*, **23**, 597 (2002).
11. Y. Y. Fan, R. E. Nieh, J. C. Lee, G. Lucovsky, G. A. Brown, L. F. Register, and S. K. Banerjee, *IEEE Trans. Electron Devices*, **49**, 1969 (2002).
12. I. Kim, J. Koo, J. Lee, and H. Jeon, *Jpn. J. Appl. Phys., Part 1*, **45**, 919 (2006).
13. C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and

- D. L. Kwong, *Tech. Dig. - Int. Electron Devices Meet.*, **2000**, 27.
14. G. C. F. Yeap, S. Krishnan, and M. R. Lin, *Electron. Lett.*, **34**, 1150 (1998).
 15. F. C. Chiu, J. J. Wang, J. Y. M. Lee, and S. C. Wu, *J. Appl. Phys.*, **81**, 6911 (1997).
 16. A. Paskaleva, E. Atanassova, and T. Dimitrova, *Vacuum*, **58**, 470 (2000).
 17. T. S. Chao, W. M. Ku, H. C. Lin, D. Landheer, Y. Y. Wang, and Y. Mori, *IEEE Trans. Electron Devices*, **51**, 2200 (2004).
 18. S. Inumiya, K. Sekine, S. Niwa, A. Kaneko, M. Sato, T. Watanabe, H. Fukui, Y. Kamata, M. Koyama, A. Nishiyama, M. Takayanagi, K. Eguchi, and Y. Tsunashima, in *IEEE Symposium on VLSI Technology*, IEEE, p. 17 (2003).
 19. K. Sekine, S. Inumiya, M. Sato, A. Kaneko, K. Eguchi, and Y. Tsunashima, *Tech. Dig. - Int. Electron Devices Meet.*, **2003**, 103.
 20. T. Watanabe, M. Takayanagi, R. Iijima, K. Ishimaru, H. Ishiuchi, and Y. Tsunashima, in *IEEE Symposium on VLSI Technology*, IEEE, p. 17 (2003).
 21. A. Kaneko, Y. Kamata, M. Ono, M. Koyama, A. Nishiyama, Y. Kamimuta, C. Hongo, A. Takashima, D. Gao, S. Inumiya, K. Eguchi, and M. Takayanagi, in *SSDM*, p. 742, (2002).
 22. A. L. P. Rotondaro, M. R. Visokay, J. J. Chambers, A. Shanware, R. Khamankar, H. Bu, R. T. Laaksonen, L. Tsung, M. Douglas, R. Kuan, M. J. Bevan, T. Grider, J. McPherson, and L. Colombo, in *IEEE Symposium on VLSI Technology*, IEEE, p. 148 (2002).
 23. A. Shanware, J. McPherson, M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, H. Bu, M. J. Bevan, R. Khamankar, and L. Colombo, *Tech. Dig. - Int. Electron Devices Meet.*, **2001**, 137.
 24. J. C. Wang, D. C. Shie, T. F. Lei, and C. L. Lee, *Electrochem. Solid-State Lett.*, **6**, F34 (2003).
 25. M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, A. Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi, and A. Nishiyama, *Tech. Dig. - Int. Electron Devices Meet.*, **2002**, 849.
 26. C. S. Kang, H. J. Cho, K. Onishi, R. Choi, Y. H. Kim, R. Nieh, J. Han, S. Krishnan, A. Shahriar, and J. C. Lee, *Tech. Dig. - Int. Electron Devices Meet.*, **2002**, 865.
 27. H. S. Jung, Y. S. Kim, J. P. Kim, J. H. Lee, J. H. Lee, N. I. Lee, H. K. Kang, K. P. Suh, H. J. Ryu, C. B. Oh, Y. W. Kim, K. H. Cho, H. S. Baik, Y. S. Chung, H. S. Chang, and D. W. Moon, *Tech. Dig. - Int. Electron Devices Meet.*, **2002**, 853.
 28. Y. Morisaki, T. Aoyama, Y. Sugita, K. Irino, T. Sugii, and T. Nakamura, *Tech. Dig. - Int. Electron Devices Meet.*, **2002**, 861.
 29. C. H. Choi, S. J. Rhee, T. S. Jeon, N. Lu, J. H. Sim, R. Clark, M. Niwa, and D. L. Kwong, *Tech. Dig. - Int. Electron Devices Meet.*, **2002**, 857.
 30. D. Ishikawa, S. Sakai, K. Katsuyama, and A. Hiraiwa, *Tech. Dig. - Int. Electron Devices Meet.*, **2002**, 869.
 31. H. J. Cho, C. S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, S. Krishnan, and J. C. Lee, *IEEE Electron Device Lett.*, **23**, 249 (2002).
 32. N. J. Seong, S. G. Yoon, S. J. Yeom, H. K. Woo, D. S. Kil, J. S. Roh, and H. C. Sohn, *Appl. Phys. Lett.*, **87**, 132903 (2005).
 33. T. M. Pan, T. F. Lei, and T. S. Chao, *J. Appl. Phys.*, **89**, 3447 (2001).
 34. T. M. Pan, T. F. Lei, T. S. Chao, K. L. Chang, and K. C. Hsieh, *Electrochem. Solid-State Lett.*, **3**, 433 (2000).
 35. S. Kamiyama, T. Miura, Y. Nara, and T. Arikado, *J. Electrochem. Soc.*, **152**, G750 (2005).
 36. K. J. Choi, J. H. Kim, and S. G. Yoon, *Electrochem. Solid-State Lett.*, **7**, F59 (2004).
 37. J. L. Gavartin, A. L. Shluger, A. S. Foster, and G. I. Bersuker, *J. Appl. Phys.*, **97**, 053704 (2005).
 38. S. A. Krishnan, M. Quevedo, R. Harris, B. H. Lee, G. Bersuker, and J. C. Lee, *Jpn. J. Appl. Phys., Part 1*, **45**, 2945 (2006).
 39. M. Bhat, D. J. Wristers, L. K. Han, J. Yan, H. J. Fulford, and D. L. Kwong, *IEEE Trans. Electron Devices*, **42**, 907 (1995).
 40. N. Umezawa, K. Shiraiishi, T. Ohno, H. Watanabe, T. Chikyow, K. Torii, K. Yamabe, K. Yamada, H. Kitajima, and T. Arikado, *Appl. Phys. Lett.*, **86**, 143507 (2005).
 41. S. Chakraborty, M. K. Bera, and C. K. Maiti, *J. Appl. Phys.*, **100**, 023706 (2006).