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Fabrication of SONOS-Type Flash Memory with the Binary High-*k* Dielectrics by the Sol-Gel Spin Coating Method

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We fabricated the binary high-*k* ($Hf_xZr_{1-x}O_2$) nanocrystal memory using a very simple sol-gel spin coating method and 900°C 60 s rapid thermal annealing (RTA). From the transmission electron microscopy identification, the nanocrystals were formed as the monolayered charge trapping site after 900°C 60 s RTA and the size was ca. 5 nm. We verified the electrical properties in terms of program-erase speed, charge retention, and endurance. The sol-gel device exhibited the long charge retention time of 10^4 s with only 2.5% charge loss, and good endurance performance for program/erase cycles up to 10^5.
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Conventional flash memory devices use floating gate structure and charge is stored in polysilicon floating gate.[1] But, when tunneling oxide is below 65 nm, floating gate structure faces scaling issues.[2] The storage charge leaks easily due to defects in the tunneling oxide formed by repeated program-erase cycles. So, discrete trap memory devices like polysilicon-oxide-nitride-silicon (SONOS) structure and nanocrystal memory are widely studied to replace floating gate structure for semiconductor memory application.[3-7] The charge trapping layer of traditional SONOS memory is silicon nitride (Si_3N_4). High-*k* materials are considered as charge storage material to get faster programming speed and better charge retention performance. But, SONOS high-*k* memory has the electron migration problem in the charge trapping layer;[5] this will cause charge loss and degrade the charge retention performance. The nanocrystal memory can keep the charge trapped tightly to avoid the charge loss problem of SONOS memory and also achieve the advantages like fast program-erase speed, low programming voltage, and good endurance as SONOS memory.[8,9]

Recently, numerous technologies have been developed for the preparation of various high-*k* films. To prepare insulating thin films, atomic layer deposition (ALD), physical vapor deposition (PVD), and chemical vapor deposition (CVD) methods have all been used to prepare films for new technologies.[10-12] The sol-gel method is a very interesting simple technique for preparing the high-*k* dielectric films[13] or memory charge trapping films.[14]

The sol-gel method can provide colloidal solvents or precursor compounds when metal halides are hydrolyzed under controlled conditions in the beaker. In the sol-gel process, hydrolysis, condensation, and polymerization steps occur to form metal-oxide networks in the solution. The most interesting feature of sol-gel processing in the solution is its ability to synthesize new types of materials that are known as "inorganic-organic hybrids."[15] Film formation with spin coating is a simpler method than ALD, PVD, or CVD to deposit the sol-gel materials due to its cheaper precursor and tool. In addition, the film can be fabricated in the normal pressure system instead of high vacuum system.[16]

In this paper, we used the sol-gel spin coating method to fabricate a SONOS-type flash memory device. We used the sol-gel method to combine two different high-*k* precursors, i.e., $HfCl_4$ and $ZrCl_4$, together to form binary high-*k* ($Hf_xZr_{1-x}O_2$) nanocrystal memory. We performed transmission electron microscope (TEM) and electrical analyses, including I_d-V_g, retention, and program-erase speed measurements, to evaluate the performance of the binary ($Hf_xZr_{1-x}O_2$) nanocrystals memory.

Experimental

The fabrication of sol-gel spin coating nanocrystals memory started with local oxidation of silicon (LOCOS) isolation process on p-type (100) 150 mm silicon substrate. At the beginning, a 4 nm tunneling oxide was thermally grown at 925°C by furnace. The charge trapping layer was prepared using a sol-gel spin coating method. $HfCl_4$ (99.5%, Aldrich, USA) and $ZrCl_4$ (99.5%, Aldrich, USA) were used as the precursors. Initially, we prepared a solution for which the molar ratio of $HfCl_4$:$ZrCl_4$:isopropanol is 1:1:1000. The charge trapping layer was deposited by spin coating at 3000 rpm for 60 s at ambient temperature (25°C). The spin-coater used was TEL Clean Track model MK8 (Japan). After spin coating, the wafer was under rapid thermal annealing (RTA) at 900°C for 60 s in O_2 ambient to form $Hf_xZr_{1-x}O_2$ nanocrystals. The RTA temperature[13] should range from 900–1050°C to meet the below source/drain (S/D) annealing condition. Hence, we chose 900°C due to the lower device damage and thermal budget.[13,14] The blocking oxide 30 nm was deposited by high density plasma chemical vapor deposition (HDPCVD) tetraethyl orthosilicae (TEOS) followed by poly-Si gate 200 nm deposition. Finally, gate patterning, S/D implant, and the rest of the subsequent complementary metal oxide semiconductor (CMOS) processes were used to fabricate this nanocrystal memory. A self-aligned implantation was used to perform the n^+ S/D extension with the As^+ dosage of 5×10^{15} cm^{-2} at the en-

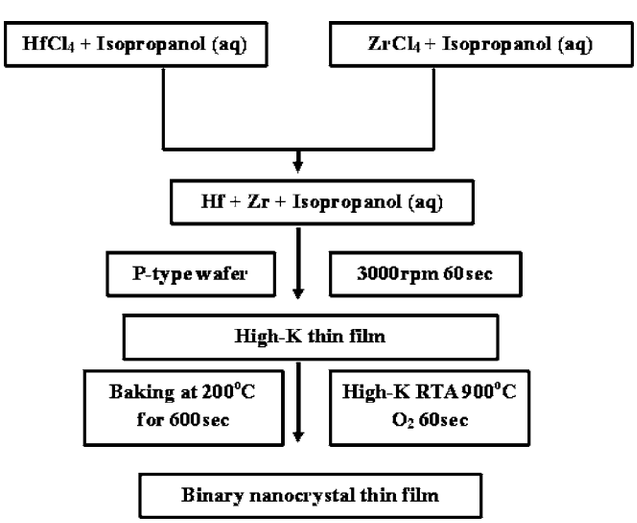

Figure 1. The process flow of the binary high-*k* SONOS-type memory.

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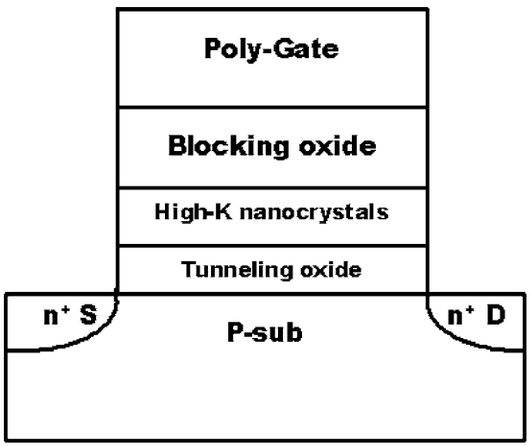

Figure 2. The structure of the binary high-*k* SONOS-type memory.

ergy of 20 keV. The channel length of the memory device was 0.35 μm. The process flow and the structure of the sol-gel SONOS-type memory are depicted in Fig. 1 and 2, respectively.

Results and Discussion

The high-resolution transmission electron microscopy (HRTEM) image in Fig. 3 depicts the nanocrystals on SiO_2 film after annealing at 900°C for 60 s. The average nanocrystal size is around 5 nm. Tang et al.[15] have studied the detailed synthesis of $Hf_xZr_{1-x}O_2$ nanocrystals at various conditions in the solution. They suggest the molar fraction of Hf or Zr in the nanocrystal from ~330°C reaction is quite complex and cannot be determined. Similarly, the binary nanocrystal is formed in our SONOS-type memory after 900°C annealing, and the molar fraction of Hf or Zr is still unknown due to the unavailability of analytical tools.

Figure 4 shows the I_d-V_g curve of the SONOS memory. We use channel hot electron injection to program, and band to band tunneling induced hot hole injection to erase. The program condition is V_g = 15 V, V_d = 10 V for 10 ms. The erase condition is V_g = −10 V, V_d = 10 V for 1 s. We can read the *V*th shift (= "*V*th of program" - "*V*th of erase") about 4 V from Fig. 4. The subthreshold slopes of I_d-V_g curves are different for the fresh cell and erased cell. The degradation of the subthreshold swing of the device with localized charge trapping is attributed to a subsurface conduction underneath the charge trapping region. Figure 5 shows the program speed

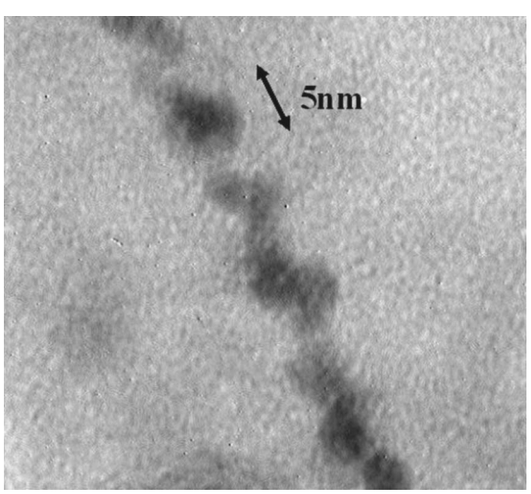

Figure 3. The TEM image of the binary high-*k* nanocrystals.

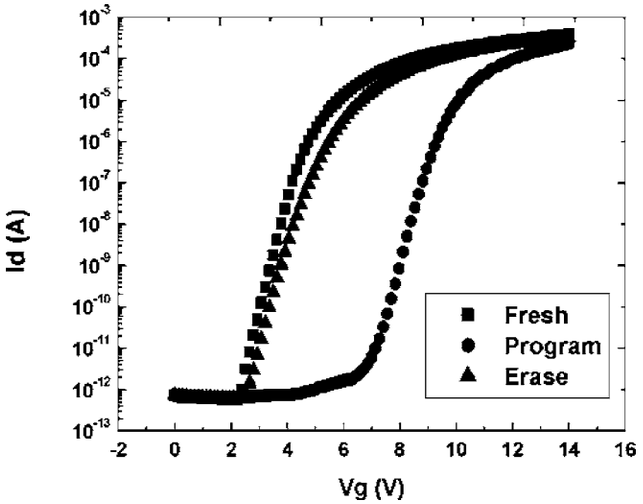

Figure 4. I_d-V_g curve of the binary high-*k* SONOS-type memory.

of the $Hf_xZr_{1-x}O_2$ nanocrystal memory. We used channel hot electron (CHE) to program, and the program conditions were (*i*) V_g = 10 V, V_d = 10 V, (*ii*) V_g = 12 V, V_d = 10 V, (*iii*) V_g = 15 V, V_d = 10 V, respectively. The *V*th shift increases with increasing applied gate voltage, and the program speed can be as fast as 0.1 ms with 2.5 V memory window for program condition V_g = 15 V, V_d = 10 V. We can see from the figure that, as the applied gate voltage increases, the *V*th shift also increases. This is because the larger the gate voltage is applied, the more "hot" electrons are generated. There are more electrons able to cross the barrier height and trapped in the $Hf_xZr_{1-x}O_2$ sites, so the *V*th shift increases. The erase speed of the $Hf_xZr_{1-x}O_2$ nanocrystal memory is also demonstrated in Fig. 6. We use band to band hot hole (BTBHH) to erase, and the erase conditions are (*i*) V_g = −10 V, V_d = 10 V, (*ii*) V_g = −12 V, V_d = 10 V, (*iii*) V_g = −15 V, V_d = 10 V, respectively. The normalized erase speed curve appears in Fig. 6, and the same explanation can be applied on the *V*th shift as gate voltage becomes more negative. Using CHE to program and BTBHH to erase yields high program-erase efficiency. The charge retention characteristic of the sol-gel $Hf_xZr_{1-x}O_2$ nanocrystal memory is demonstrated in Fig. 7. The normalized *V*th shift is defined as the ratio of the *V*th shift at the time of interest and at the beginning. Using this as an indicator, we can see the charge loss for the nanocrystal memory. The curve is obtained in

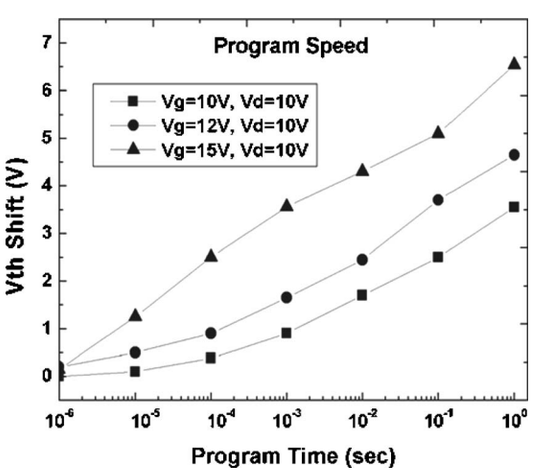

Figure 5. The program speed of the binary high-*k* SONOS-type memory.

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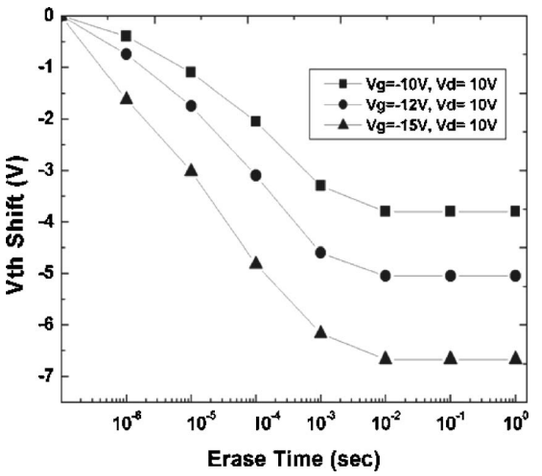

Figure 6. The erase speed of the binary high-*k* SONOS-type memory.

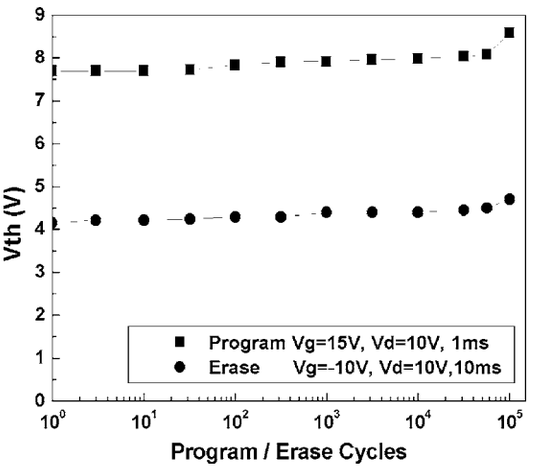

Figure 8. The endurance characteristic of the binary high-*k* SONOS-type memory.

program condition of V_g = 12 V and V_d = 10 V at 10 ms under room temperature and 85°C, respectively. The room temperature retention curve shows only 2.5% charge loss as time is measured up to 10^4 s. The 85°C curve exhibits ~15% charge loss. This result indicates the $Hf_xZr_{1-x}O_2$ nanocrystals in the charge trapping site can tightly catch the tunneling electrons. Hence, the electrons trapped by the sol-gel-derived nanocrystal devices did not easily escape, and the exhibited charge loss percentage is quite low. Figure 8 shows the endurance characteristics of the nanocrystal memory. The measurement condition is programmed under V_g = 15 V and V_d = 10 V for 1 ms, and is erased under V_g = −10 V and V_d = 10 V for 10 ms. As the figure shows, the memory window is about 3.6 V after 10^5 program/erase (*P*/*E*) cycles. No significant window narrowing is observed. This observation verifies the reliability of our sol-gel-derived $Hf_xZr_{1-x}O_2$ nanocrystal memory.

Conclusions

In this paper, we used a sol-gel spin coating method to form nanocrystals as the charge trapping site of SONOS memory. The TEM analysis indicates the formation of ~5 nm $Hf_xZr_{1-x}O_2$ nanocrystals. We have verified the device performance with the *P*/*E* speed, charge retention, and endurance. The quality of the nanocrystals formed by the sol-gel spin coating method and RTA treatment exhibits better properties in terms of fast *P*/*E* speed, long charge retention time, and good endurance with no memory window narrowing.

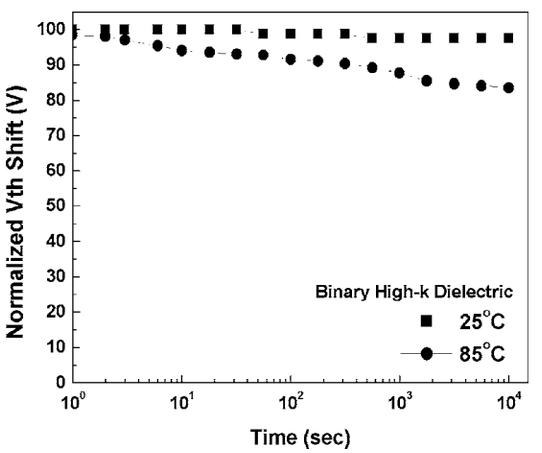

Figure 7. Charge retention curve of the binary high-*k* SONOS-type memory at room temperature and 85°C, respectively.

Acknowledgments

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References

1. R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, *Proc. IEEE*, **91**, 489 (2003).
2. B. D. Salvo, C. Gerardi, R. V. Schaijk, S. A. Lombardo, D. Corso, C. Plantamura, T. Serafino, G. Ammendola, M. V. Duuren, P. Goarin, W. Y. Mei, K. V. D. Jeugd, H. Baron, M. Gély, P. Mur, and S. Deleonibus, *IEEE Trans. Device Mater. Reliab.*, **4**, 377 (2004).
3. Y.-N. Tan, W.-K. Chim, B. J. Cho, and W.-K. Choi, *IEEE Trans. Electron Devices*, **51**, 1143 (2004).
4. Y. N. Tan, W. K. Chim, W. K. Choi, M. S. Joo, T. H. Ng, and B. J. Cho, *Tech. Dig. - Int. Electron Devices Meet.*, **2004**, 889.
5. T. Sugizaki, M. Kohayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, *VLSI Tech. Symposium*, 27 (2003).
6. X. Wang, and D. L. Kwong, *IEEE Trans. Electron Devices*, **53**, 78 (2006).
7. M. H. White, D. A. Adams, and J. Bu, *IEEE Circuits Devices Mag.*, **22**, (2000).
8. M. She and T. J. King, *IEEE Trans. Electron Devices*, **50**, 1934 (2003).
9. M. Takata, S. Kondoh, T. Sakaguchi, H. Choi, J.-C. Shim, H. Kurino, and M. Koyanagi, *Tech. Dig. - Int. Electron Devices Meet.*, 2003, 553.
10. S. Kamiyama, T. Miura, and Y. Nara, *J. Electrochem. Soc.*, **153**, G187 (2006).
11. J. Y. Tewg, Y. Kuo, and J. Lu, *J. Electrochem. Soc.*, **152**, G643 (2005).
12. L. Goux, H. Vander Meeren, and D. J. Wouters, *J. Electrochem. Soc.*, **153**, F132 (2006).
13. H.-C. You, F.-H. Ko, and T.-F. Lei, *J. Electrochem. Soc.*, **153**, F94 (2006).
14. T.-H. Hsu, H.-C. You, F.-H. Ko, and T.-F. Lei, *J. Electrochem. Soc.*, **153**, G934 (2006).
15. J. Tang, J. Fabbri, R. D. Robinson, Y. Zhu, I. P. Herman, M. L. Steigerwald, and L. E. Brus, *Chem. Mater.*, **16**, 1336 (2004).
16. H.-C. You, T.-H. Hsu, F.-H. Ko, J.-W. Huang, W.-L. Yang, and T.-F. Lei, *IEEE Electron Device Lett.*, **27**, 644 (2006).

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