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High-Performance HfO_2 Gate Dielectrics Fluorinated by Postdeposition CF_4 Plasma Treatment

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The superior characteristics of fluorinated HfO_2 gate dielectrics were investigated. Fluorine was incorporated into HfO_2 thin film by postdeposition CF_4 plasma treatment to form fluorinated HfO_2 gate dielectrics. Secondary-ion mass spectroscopy results showed that there was a significant incorporation of fluorine atoms at the TaN/HfO_2 and HfO_2/Si interface. Improvement of the gate leakage current, breakdown voltage, capacitance-voltage hysteresis, and charge trapping characteristics was observed in the fluorinated HfO_2 gate dielectrics, with no increase of interfacial layer thickness. A physical model is presented to explain the improvement of hysteresis and the elimination of charge trapping. These results indicate that the fluorinated HfO_2 gate dielectrics appear to be useful technology for future ultrathin gate dielectrics.
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For anticipated applications of very large scale integration (VLSI) technology, more advanced materials for gate dielectrics will be required. Although a physical gate thickness of <1 nm for a complementary metal oxide semiconductor transistor with nitride/oxynitride gate stacks has been demonstrated,[1] continued scaling for future semiconductor technology requires an equivalent oxide thickness of less than 1.0 nm for sub-65-nm metal oxide semiconductor field-effect transistor (MOSFET) devices.[2] However, development of a dielectric thin film with an effective oxide thickness under 1.0 nm and an acceptable leakage current level will be very difficult, due to the high direct tunneling leakage current of nitride/oxynitride gate dielectrics. As a result, high-dielectric-constant (high-k) oxide thin films are currently attracting great interest as possible alternatives to nitrided-SiO_2 gate dielectrics.[3-5]

Various extrinsic gate dielectrics, including Ta_2O_5, Y_2O_3, ZrO_2, CeO_2, $SrTiO_3$, $BaSrTiO_3$ (BST), and HfO_2 have been extensively investigated. Among these high-k gate materials, HfO_2 gate dielectrics[6-8] are the most popular candidate currently under study, due to their high dielectric constant (25–30), wide energy bandgap ($\sim$5.68 eV), and the high stability of their Si surface. At the moment, capacitance-voltage (C-V) hysteresis and charge trapping when the hafnium dioxide is applied to the MOSFET as the gate dielectrics,[9-11] are critical problems for future ultralarge scale integration (ULSI) technology applications of HfO_2. Therefore, various methods have been used to ameliorate these problems, including cosputtering of silicon and aluminum with hafnium to deposit hafnium silicate and aluminate dielectrics,[12,13] nitridation before HfO_2 deposition,[14]and oxidizing a sputtered metal nitride such as HfN[15] to form hafnium oxynitride (HfON) films.

Recently, fluorinated gate dielectrics have been shown to improve the SiO_2/Si interface.[16-19] Furthermore, fluorine incorporation into the high-k gate dielectrics has been proposed, to improve both the thermal stability,[20] and the negative bias temperature instability (NBTI) reliability.[21,22] However, characterization of key aspects of fluorinated HfO_2 gate dielectrics formed by CF_4 plasma treatment, including the thermal stability of the gate leakage current and C-V characteristics, breakdown voltage, and effective oxide thickness, has not been well developed. In addition, neither charge trapping during electrical measurement nor the temperature dependence of the gate leakage current has been investigated.

In this paper, the characteristics of fluorinated HfO_2 gate dielectrics using CF_4 plasma treatment were demonstrated. Fluorinated HfO_2 gate dielectrics show thinner effective oxide thickness ($\sim$2.2 nm), smaller C-V hysteresis (45 mV), low gate leakage current density ($\sim 5 \times 10^{-9}$ A/cm^2), high breakdown voltage (~ -9 V), better thermal stability, good distribution of electrical performance, and less charge trapping. A physical model is proposed to comprehensively explain the mechanism for electron and hole trapping in fluorinated HfO_2 thin film. Furthermore, the temperature dependence of the leakage current explains why the generated traps are effectively eliminated in fluorinated HfO_2 gate dielectrics.

Experimental

For the purposes of this research, MOS capacitors were fabricated. The silicon wafers used in this study were p-type (100) Czochralski (CZ) with a resistance of 4–7 Ω cm. Standard RCA cleaning was first performed on all samples. HfO_2 thin film was then deposited by reactive radio-frequency (rf) sputter method. Deposition plasma was created by applying 150 W rf power to a 7.5 cm diam target positioned 15 cm away from the substrate. Hafnium dioxide deposition took place for 2.5 min, resulting in the formation of a 5 nm HfO_2 thin film. After HfO_2 thin film deposition, CF_4 plasma was used to treat the HfO_2 thin film to form the fluorinated HfO_2 gate dielectrics. Some samples were treated under CF_4 plasma in the plasma-enhanced chemical vapor deposition (PECVD) system, whose chamber volume is 3.76×10^5 cm^3. The cathode diameter was 40 cm, and the distance between the cathode and the holder was 4 cm. The sample was loaded into the substrate at an elevated temperature (300°C). The reactive pressure and the flow rate of the CF_4 gas were 600 mTorr and 500 sccm, respectively. The rf power was 40 W with CF_4 plasma exposure times of 1 and 5 min (termed P-1 and P-5, respectively). For the normal HfO_2 gate dielectrics samples (denoted as as-deposited), there was no CF_4 plasma treatment after the hafnium dioxide deposition. Postdeposition annealing (PDA) was performed on rapid thermal anneal (RTA) equipment at 700°C for 30 s in N_2 ambient. Samples with PDA treatment were called as-deposited/A, or P-1/A and P-5/A. The PDA process was used to determine the thermal stability of the as-deposited HfO_2 and fluorinated HfO_2 gate dielectrics. In a later phase of the investigation, a 50 nm TaN metal gate was also deposited by the rf sputter method. An aluminum film 300 nm thick was then deposited on the TaN gate for use as the gate electrode. Finally, the 300 nm aluminum film was evaporated from the bottom of the electrode by a thermal evaporator to form the MOS capacitors.

The effective oxide thickness (EOT) was estimated from the accumulation capacitance of the high-frequency (100 kHz) C-V measurement with a gate area of 6.75×10^{-5} cm^2. Quantum effects were not considered. To explore CF_4 plasma etching effects in HfO_2 thin film, atomic force microscopy (AFM) was used to analyze the

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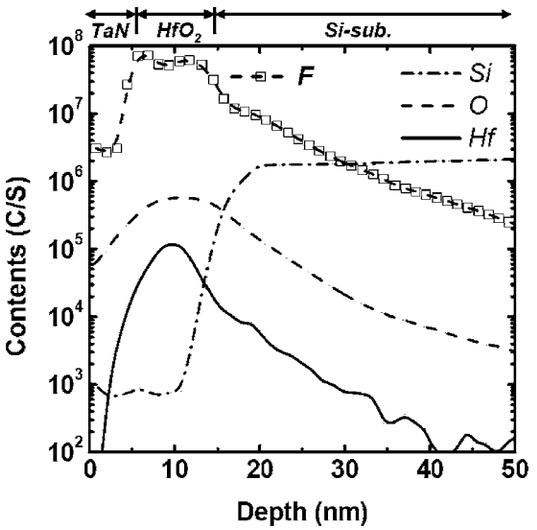

Figure 1. SIMS depth profile of MOS structure for fluorine oxygen, hafnium, and silicon atom distribution. The fluorine atoms were accumulated mainly at the two interfaces of the gate-oxide films.

surface morphology of the HfO_2 thin film after CF_4 plasma treatment. Furthermore, the content and distribution of the fluorine atoms was measured by secondary-ion mass spectroscopy (SIMS). X-ray photoelectron spectroscopy (XPS) was used to analyze the Hf-O and Hf-F bondings of the fluorinated HfO_2 thin films.

Results and Discussion

Figure 1 shows the SIMS depth profiles of HfO_2 film with post-deposition CF_4 plasma treatment. The location of both the top and bottom HfO_2 interfaces was determined from the silicon, oxygen, and hafnium profiles. This experimental result shows that the fluorine atoms are located primarily at the two interfaces of the TaN/HfO_2 and HfO_2/Si-substrates. The accumulation of fluorine atoms the interfaces of the gate dielectrics has been proposed in previous studies.[22,23] However, some fluorine atoms accumulated in the bulk HfO_2 thin film, as shown by the XPS analysis (Fig. 2). Thus, it appears that fluorine atoms are distributed in each of the HfO_2 gate

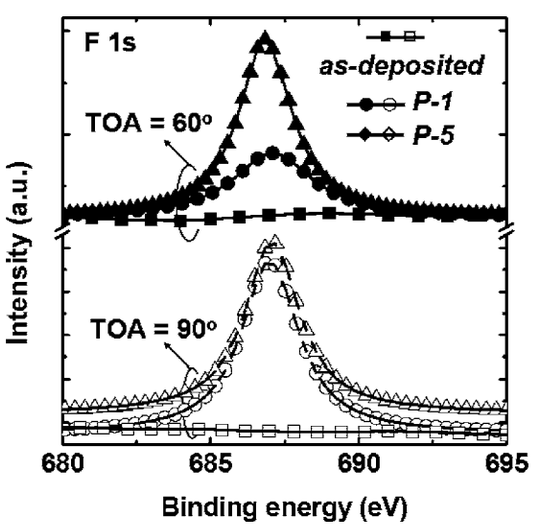

Figure 2. XPS analysis of the F 1s electronic spectra of as-deposited and fluorinated samples, TOAs of 60 and 90°, respectively, where the F 1s peak is at 687 eV.

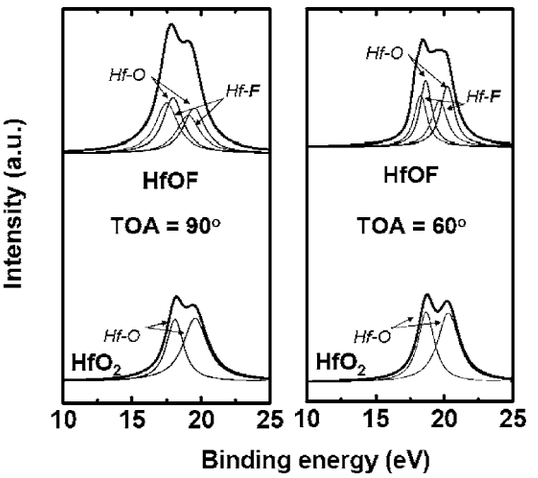

Figure 3. Hf 4f XPS spectra of as-deposited and fluorinated HfO_2 thin films, respectively. Take-off angles of 60 and 90° were used to measure the XPS spectra.

dielectrics after CF_4 plasma treatment. Wright et al. proposed that fluorine atoms react with Si–O bonds, and then the released oxygen atoms oxidize the SiO_2/Si interface.[24] We thus argue that the structural change of the gate-oxide films occurs due to the reaction between the fluorine atoms and the Si–O bonds.

Take-off angles (TOAs) of 60 and 90° were used to measure the XPS spectra of surface and bulk HfO_2 thin films (Fig. 2). In Fig. 2, for all samples except the as-deposited sample, a distinct F 1s peak at 687 eV can be observed. The CF_4 plasma treatment processes are apparently introducing fluorine atoms into the dielectrics, as noted in the prior SIMS analysis. Furthermore, the F 1s peak of the sample with the longer CF_4 plasma treatment (5 min) displays a higher intensity when the TOA is 60°. This implies that the longer CF_4 plasma treatment introduces more fluorine at the surface of the HfO_2 thin films. In addition, the fluorine intensity was nearly identical in the bulk of HfO_2 thin films, regardless of CF_4 plasma treatment conditions (Fig. 2; TOA is 90°). Figure 3 shows the Hf 4f ESCA spectra of HfO_2 and fluorinated HfO_2 thin film. Two distinct peaks of Hf–O bonding, at 18.7 and 20.3 eV, were found in the as-deposited sample. Nevertheless, the as-deposited samples may also have large numbers of other types of bonding defects, which was not observed when the material is prepared. The TOA angles of 60 90° were also used to measure the XPS spectra. Compared to the Hf–O bonds in Hf 4f spectra of the HfO_2 thin film, the Hf 4f spectra of the fluorinated HfO_2 thin film is shifted roughly 0.43 eV (Fig. 3). This also shows the Hf–F bonding formation after CF_4 plasma treatment, as seen in Fig. 1 and 2. To investigate the plasma etching effect in HfO_2 thin film, we used AFM and ellipsometry to analyze the surface roughness and thickness of the HfO_2 thin film with and without CF_4 plasma treatment. Ellipsometry indicated that the thicknesses of as-deposited and fluorinated HfO_2 thin films (P-5) are 5.035 and 4.994 nm, respectively. These results imply that the CF_4 plasma etching effect during the treatment of HfO_2 thin films is negligible. In addition, the root-mean-square (rms) variations of the surfaces of the as-deposited and fluorinated HfO_2 thin film (P-1), extracted from the AFM images, are 1.05 and 1.74 Å, respectively (Fig. 4a and b). Furthermore, the rms of the HfO_2 thin film with 5 min of CF_4 plasma treatment was only 2.03 Å. These results appear to show that the CF_4 plasma treatment did not damage the HfO_2 thin film during fluorinated HfO_2 thin film formation.

Figure 5 shows the current density vs gate voltage (J-V) characteristics of as-deposited and fluorinated HfO_2 gate dielectrics. The gate leakage current of the samples after 700°C annealing increased due to dielectric film crystallization. In addition, the breakdown

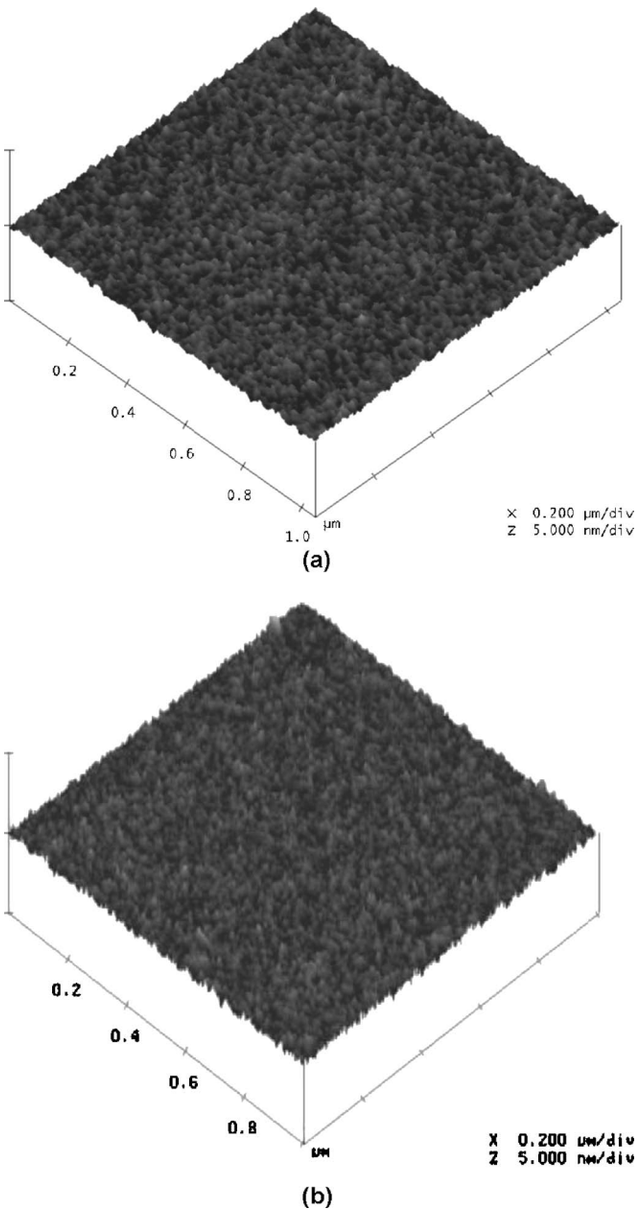

Figure 4. AFM images of the surface of the HfO_2 thin films (a) without CF_4 plasma treatment and (b) with CF_4 plasma treatment for 1 min.

voltage of the fluorinated HfO_2 gate dielectrics was also improved (Fig. 5). The inset in Fig. 5 depicts the close fit of all samples to the Frenkel–Poole model. The linear behavior is a further indication that the carrier transportation in both as-deposited and fluorinated HfO_2 is F–P emission. The effective barrier heights (Φ_B) were much higher for the fluorinated HfO_2 gate dielectrics, with and without PDA treatment (inset, Fig. 5). In addition, the Schottky emission barrier (TaN/HfO barrier) was also calculated. Because the barrier height extracted from Schottky emission was larger than the trap energy extracted from F–P conduction, the F–P conduction mechanism would dominate over the Schottky emission.

Figure 6 shows the effective oxide thickness vs gate leakage current characteristics of HfO_2 gate dielectrics with and without CF_4 plasma treatment and 700°C postdeposition annealing (PDA). The inset shows the C-V characteristics of all the samples. The thinner EOT extracted from C-V curves was obtained for the HfO_2 gate dielectrics with CF_4 plasma treatment and was further improved

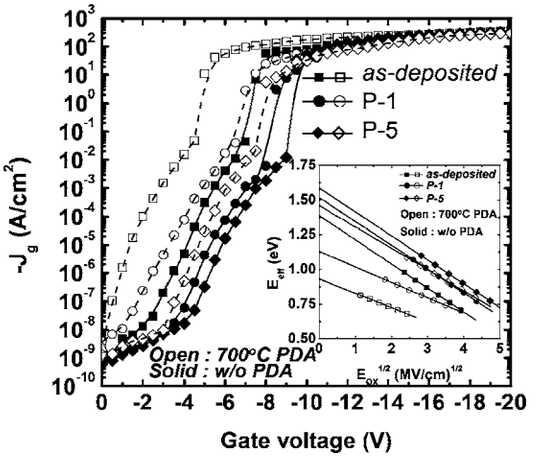

Figure 5. C-V characteristics for the as-deposited and fluorinated HfO_2 gate dielectrics with and without PDA. (Inset) The F–P curve fit for all samples. The fluorinated HfO_2 gate dielectrics have a higher F–P barrier height, which increases as plasma treatment time increases.

after annealing at 700°C. The CF_4 plasma treated HfO_2 films appeared to possess properties superior to those of the as-deposited samples, including thin EOT and low leakage current. However, the HfO_2 films, after 700°C PDA, still presented higher gate leakage current at the same EOT than the as-deposited samples, owing to the film crystallization discussed earlier.

Figure 7 shows the Weibull distribution plots of the gate leakage current density at the gate voltage of −3 V and the breakdown voltage for all samples. Both the performance and uniformity distribution of the fluorinated HfO_2 gate dielectrics were superior to those of the as-deposited samples.

The normalized C-V hysteresis curves of the as-deposited and fluorinated HfO_2 gate dielectrics are shown in Fig. 8a and b, respectively. The C-V hysteresis of the as-deposited HfO_2 gate dielectrics was 1 V, but decreased to roughly 50 mV for the fluorinated HfO_2 gate dielectrics (P-5). According to the inner-interface trapping model,[25] when the capacitor is biased at accumulation (V_G = −3 V), majority carriers (holes for the p-type Si substrate) tunnel from p-Si substrate through the interfacial layer (IL) and are trapped at the inner-interface, as indicated in the inset band diagram in Fig.

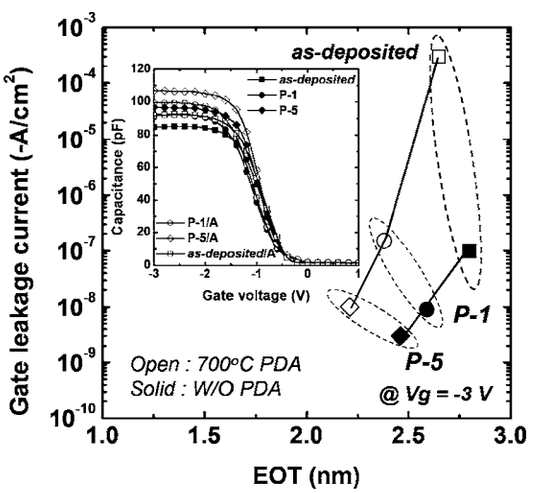

Figure 6. The relationship between gate leakage current and EOT, extracted from the C-V curves (inset figure) for all samples. The fluorinated HfO_2 gate dielectrics have lower leakage current and EOT.

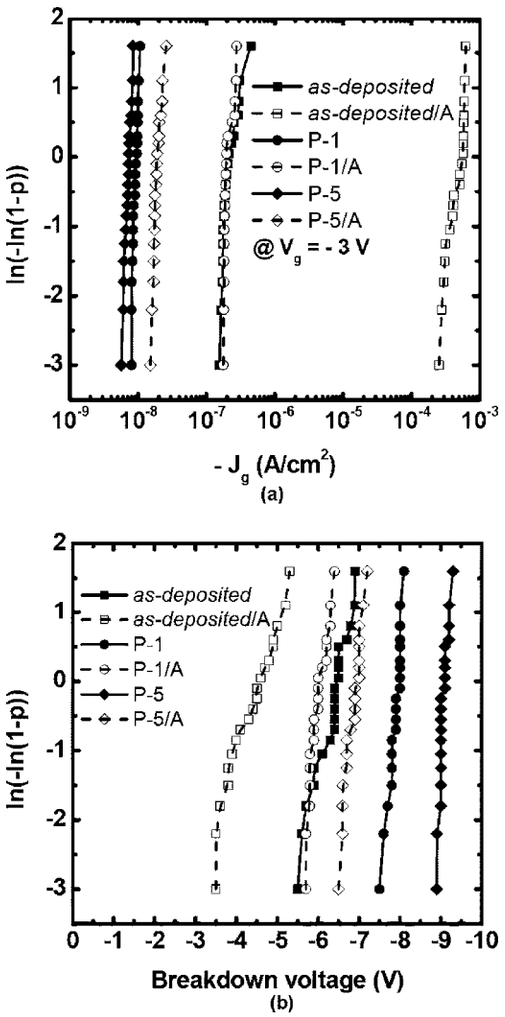

Figure 7. The Weibull distribution of the (a) gate leakage current and (b) breakdown voltage, for the as-deposited and fluorinated HfO_2 gate dielectrics. A good distribution performance of the fluorinated HfO_2 gate dielectrics was observed.

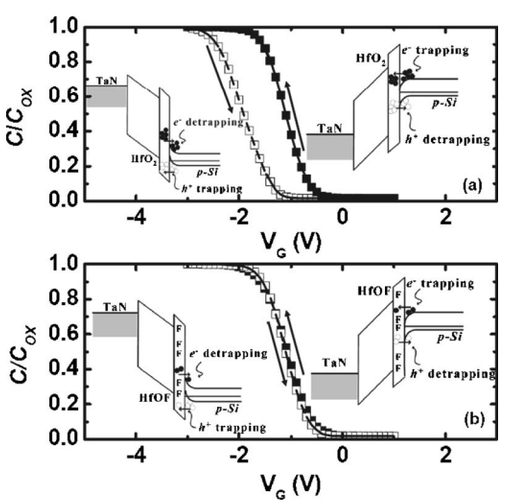

Figure 8. The C-V hysteresis characteristics for the (a) as-deposited and (b) fluorinated HfO_2 gate dielectrics, respectively. The inset band-diagram explains the charge trapping mechanism.

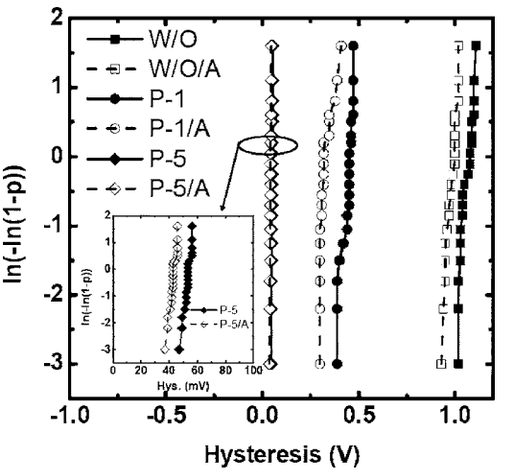

Figure 9. The Weibull distribution of the C-V hysteresis for all samples. Only 50 mV C-V hysteresis was observed for the fluorinated HfO_2 gate dielectrics.

8a. Furthermore, when the voltage is biased at the inversion region (V_G = 1 V), the trapped holes at the inner-interface will be detrapped, while at the same time the minority carriers (electrons) tunnel from the p-Si substrate and are trapped at the inner-interface. On the other hand, the shifted C-V curves are not parallel at intermediate and low voltages. A slight degradation of C-V curves in depletion region can be observed as indicated in Fig. 8a. As a result, the hysteresis phenomenon was contributed by both interface states and bulk trapping. However, for the fluorinated HfO_2 thin film, the number of holes and the number of electrons trapped at the inner-interface and some interface states were reduced, owing to the F atoms incorporated into the HfO_2 thin film (Fig. 8b, inset). This indicates that hole trapping was observed in our HfO_2 thin film, a finding strongly supported by the negative flat band voltage shift during the C-V hysteresis measurement.

Figure 9 displays the Weibull distribution of C-V hysteresis for all samples. The C-V hysteresis was improved by increasing the CF_4 plasma treatment duration. Of all the samples, the HfO_2 films with CF_4 plasma treatment for 5 min, and rapid thermal annealing at 700°C for 30 s (P-5/A) exhibit the smallest C-V hysteresis, about 40 mV.

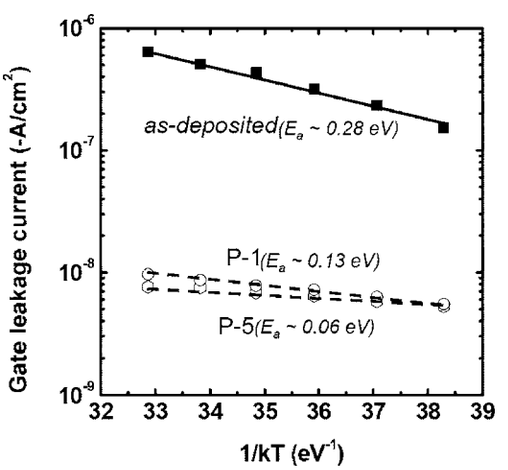

Figure 10. Arrhenius plots of leakage current density for the HfO_2 and fluorinated HfO_2 gate dielectrics. The plots were obtained from the current-voltage characteristics at $Vg = -3$ V measured from 303 to 353 K.

Table I. Summaries of the characteristics for all samples. The fluorinated sample exhibits superior properties in EOT, leakage current, breakdown voltage, hysteresis, and charge trapping.

	EOT (nm)	Jg A/cm^2 @$V_g = -3$ V	F-P Φ_B (eV)	C-V Hys. (V)	E_a (eV)	$-V_{BD}$ (V)	Surface rough. (Å)
As-deposited	2.8	1×10^{-7}	1.38	1.1	0.28	6.5	1.05
As-deposited/A	2.68	5×10^{-4}	0.93	1	0.27	4.8	
P-1	2.62	9×10^{-9}	1.52	0.51	0.13	8	1.74
P-1/A	2.53	1×10^{-7}	1.13	0.31	0.13	5.9	
P-5	2.47	7×10^{-9}	1.58	0.05	0.06	9	2.03
P-5/A	2.21	1×10^{-8}	1.46	0.045	0.06	7	

Figure 10 shows the Arrhenius plots of the temperature dependence leakage current density for the as-deposited and fluorinated HfO_2 gate dielectrics. The plots were obtained from the current voltage characteristics at $V_G = -3$ V, measured at 303–353 K. The data fit to the relationship $J \propto \exp(-E_a/k_B T)$. The calculated values of the activation energies for the as-deposited sample and fluorinated samples are 0.28, 0.13 (P-1), and 0.06 eV (P-5), respectively. This apparently shows that the CF_4 plasma treatment effectively removed the dielectric vacancies, leading to a lower concentration of generated traps.[26] The temperature dependence performance of the gate leakage current for as-deposited HfO_2 gate dielectrics was more obvious, owing to the large concentration of generated traps (hole trapping), as illustrated in C-V hysteresis. The results of the decrease in activation energy (Fig. 10) indicate that the fluorinated HfO_2 gate dielectrics have a lower concentration of generated hole traps.

Table I summarizes the characteristics for all samples. The surface roughness of the HfO_2 thin films was not degraded by CF_4 plasma treatment. Furthermore, the fluorinated sample exhibits superior properties in EOT, leakage current, breakdown voltage, hysteresis, and elimination of deep traps.

Conclusion

An approach to demonstrate the characteristics of fluorinated HfO_2 gate dielectrics formed by CF_4 plasma treatment was proposed and systematically studied. The fluorinated HfO_2 thin film exhibited superior C-V and I-V performance even after high-temperature annealing. Furthermore, charge trapping occurred in C-V hysteresis, while measurement of the fluorinated HfO_2 gate dielectrics was effectively improved. This technology may be applicable to HfO_2 thin films for future ULSI applications.

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