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Degradation of the Capacitance-Voltage Behaviors of the Low-Temperature Polysilicon TFTs under DC Stress

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In this paper, the degradation of n-type low-temperature polycrystalline silicon (poly-Si) thin-film transistors (TFTs) under dc stress is investigated with measurement of the capacitance between the source and the gate (C_{GS}), as well as the capacitance between the drain and the gate (C_{GD}). It is discovered that the degradation in C_{GD} curves of the device after hot carrier stress shows apparent frequency dependence, while that in the C_{GS} curves remains almost the same. A circuit model based on the channel resistance extracted from the current-voltage behavior is proposed to describe the frequency dependence of the capacitance behavior. From this model, it is revealed that the anomalous frequency-dependent capacitance-voltage characteristics may simply reflect the transient behaviors of the channel resistances. Besides, it was found that the C_{GS} curves after self-heating effect exhibit a significant shift in the positive direction and an additional increase for the smaller gate voltage, while the C_{GD} curves show only positive shifts. By employing simulation, it was proved that the self-heating effect creates interface states near the source region and increases the deep states in the poly-Si film near drain. The proposed circuit model further explains the behavior of the C_{GS} and C_{GD} curves for the stressed device at different measuring frequencies.
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Low-temperature poly-Si (LTPS) thin-film transistors (TFTs) have attracted much attention for active matrix liquid crystal display (AMLCD) and active matrix organic light emitting diode (AMOLED) applications due to the high mobility and capability of realizing integrated circuits on the same glass. The degradation behavior of the device is an important issue in the application. It was reported that poly-Si TFTs suffer from several degradation mechanisms, such as hot carrier effect,[1-4] self-heating effects,[5,6] water,[7] and photon-induced leakage current.[8,9] The two main degradation mechanisms of n-type TFTs are the hot carrier effect and the self-heating effect.[10] Hot carrier effect, arising from the carriers under the high electric field around the drain, is reported to cause the degradation of drain current and channel mobility.[11] In poly-Si TFTs, because there are many traps in the poly-Si film, the hot carrier effect is closely related to the crystallization condition and grain boundary locations of the poly-Si film.[12] The degradation of threshold voltage and mobility of devices after self-heating stress is especially a serious problem, because TFTs are fabricated on glass substrates which have the poor thermal conductivity. Most of the previous works focused on the current transfer characteristics to investigate the mechanism of degradation after stress. However, because the current transfer behaviors are affected by the entire degradation regions in the channel, it would be difficult to examine the damaged region of the device after stress in detail. In this work, the effects of these two stress conditions are examined with capacitance-voltage (C-V) measurement, which can further reveal the damaged location and mechanism of these two stress conditions. The frequency response of the capacitance curves would also be helpful in identifying the degradation mechanisms to be the trapped charges or the increased states.

Experimental

The process flow of TFTs is described below. First, the buffer oxide and 50 nm thick a-Si:H films were deposited on glass substrates with plasma-enhanced chemical vapor deposition (PECVD). The samples were then put into the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm^2 was applied. The laser scanned the a-Si:H film with the beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 80 nm SiO_2 and 40 SiN_x films were deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. The lightly doped drain (LDD) and the n$^+$ source/drain doping were formed by PH_3 implantation with dosage 2×10^{13} and 2×10^{15} cm^2 of PH_3, respectively. The LDD implantation was self-aligned and the n$^+$ regions were defined with a separate mask. Then the interlayer of SiN_x was deposited. Subsequently, the rapid thermal annealing was conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated. Finally, the contact hole formation and metallization were performed to complete the fabrication work.

In this study, n-type TFTs with a channel width of 20 μm and a channel length of 5 μm with an LDD structure of length 1.2 μm are fabricated. The C-V curves of the gate-to-source capacitance C_{GS} and gate-to-drain capacitance C_{GD} before and after stress with different frequencies are measured with an HP 4284A precision LCR meter. The concept of operation of the apparatus is to find the effective impedance of the equivalent circuit of the device under test between the probing nodes, and via the circuit theory, the capacitance of the device can then be obtained. Before measuring the capacitance behavior, for every frequency the measure correction is performed with the open-circuit and short-circuit mode, respectively, for the needles before and after probing the electrode to eliminate the effect of the parasitic components in the surrounding and during probing.

Results and Discussion

Hot carrier effect.— Hot carrier effect, as many works have reported, is closely related to the distribution of the lateral electric field in the channel and therefore is in relation with the applied drain voltage V_{DS} and gate voltage V_{GS}. The high electric field near the drain region would accelerate the carriers and these carriers may break the Si bonds, resulting in the increase of tail states. These increased states affect the conduction for the gate voltage larger than the threshold voltage V_{TH} and then degrade the device mobility.[13] Unlike in metal oxide semiconductor field effect transistors (MOSFETs), the hot carrier effect in TFTs becomes most severe as V_{GS} is just above V_{TH} and V_{DS} is large.[14] Because the active region in the poly-Si TFTs contains many grain boundaries, the effect of hot carrier stress may be more complicated than that in MOSFETs. Figure 1 shows the I_D-V_G transfer characteristics before and after 500 s of hot carrier stress with the conventional forward and reverse connection. Here the stress condition is that the drain voltage is equal to 20 V and the gate voltage is 1 V larger than V_{TH}, namely, 2.8 V. It can be seen that as compared with the unstressed device, the stressed

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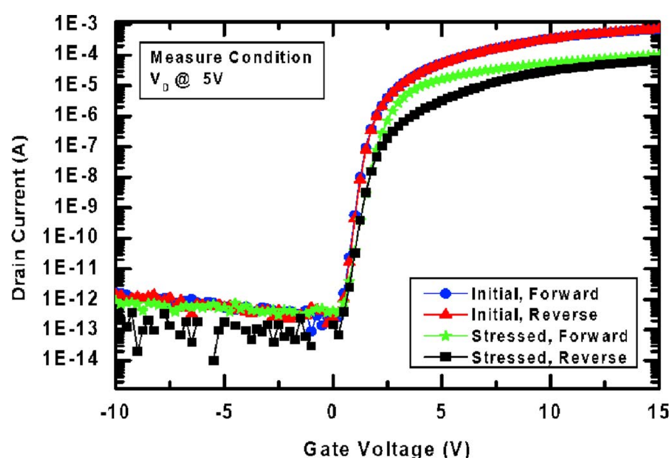
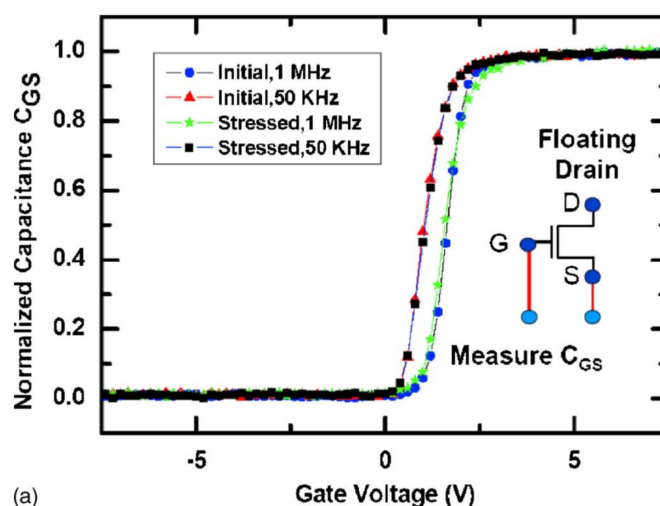


Figure 1. (Color online) Current-transfer characteristics before and after hot carrier stress condition ($V_{GS} = V_{th} + 1$ V = 2.8 V, $V_{DS} = 20$ V, and time duration of 500 s) with the forward and reverse connections.



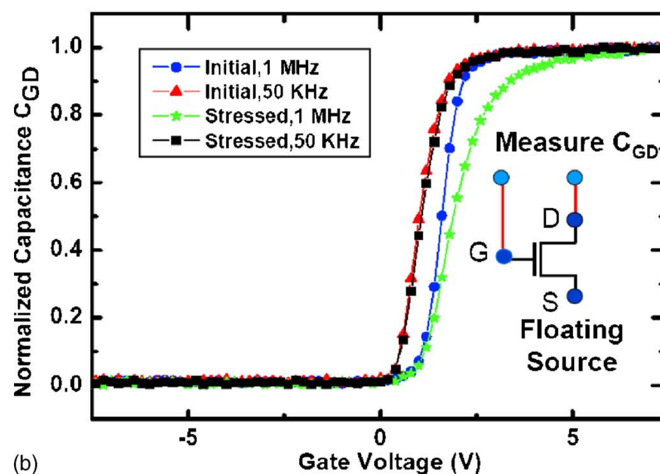


Figure 2. (Color online) (a) and (b) Normalized C_{GS} and C_{GD} curves (before and after hot carrier stress) vs gate voltage at frequencies of 50 kHz and 1 MHz.

device shows lower ON current and almost unchanged subthreshold region. However, the difference in the ON current of the stressed device between the forward and reverse connection indicates that the states distribute closer to the drain. In order to understand the detailed degradation mechanism, *C-V* measurement is employed. Figure 2a shows the normalized gate-to-source capacitance C_{GS} curves before and after stress with different measuring frequencies, and Fig. 2b shows those of the C_{GD} curves. The C_{GS} is measured with the floating drain and C_{GD} is measured with the floating source. The normalized capacitance is the ratio of the measured capacitance to a constant of 40 fF, which is the gate insulator capacitance of the TFT. The C_{GS} curves of the stressed device show almost no difference as compared with the unstressed device. Nevertheless, the C_{GD} curves of the stressed device show peculiar behaviors. The C_{GD} curve of the stressed device measured at 50 kHz is almost the same as that before stress, but the curve at 1 MHz shows that the apparent stretch for the gate voltage is just above the flatband voltage V_{FB}. In other words, the degradation behavior of the C_{GD} curves of the device after hot carrier stress is frequency dependent.

In order to examine the frequency dependence of the *C-V* behavior of the devices after hot carrier stress, the C_{GS} and C_{GD} curves of the stressed devices at different applied frequencies are measured. Figures 3a and b show the C_{GS} and C_{GD} curves of the stressed device at measuring frequencies of 50 kHz, 100 kHz, 500 kHz, and 1 MHz. The C_{GS} curves of the stressed device show only a slight shift for different applied frequencies. However, in addition to the shift, the C_{GD} curves show an apparent stretch between different measuring frequencies for the gate voltage higher than V_{FB}. The higher the measuring frequency applied, the more the C_{GD} curve stretches.

To find the mechanism of this behavior, the 2D simulation program DESSIS is employed. The grain boundaries inside the poly-Si film are accounted for by using the "effective medium approach," which treats the poly-Si film as a uniform material with the density of localized states in the bandgap.[15] Referring to previous reports, the hot carrier effect causes the increase of the tail states in the bandgap of the poly-Si film.[16] Therefore, in simulation the tail states are purposely simulated with the Gaussian distribution in the bandgap of the poly-Si film near the drain. Figures 4a and b, respectively, show the state condition in the bandgap and physical location in the simulation. The tail states are modeled by the Gaussian distribution with standard deviation 0.2 eV and the peak value of the distribution is 10^{20} cm^{-3}. Three kinds of state positions in the bandgap of 0.6 eV are arranged in simulation. The three state conditions are arranged such that the distance between the bottom of the conduction band E_C and the center of the state distributions are 0.2, 0.3, and 0.4 eV. Figure 4c is the simulated *C-V* curves of the proposed device model with the three state conditions. It can be seen that the capacitance curve would apparently stretch for the gate voltage just above V_{FB} for the trap condition *C*, which is the state distribution located just above the Fermi level E_F. When the state locations are drawn near to E_C, as in the case of state conditions A and B, the capacitance curves would stretch more for the gate voltage larger thanV_{FB}.

The simulated curves may fairly explain the capacitance curves for the high measuring frequency, but it may not explain the capacitance curves for different applied frequencies. With the viewpoint of trap and emission, the states in the channel would have enough time to respond to the applied signal at lower measuring frequency and thus the effect of the states can be measured. However, the measured results show the opposite behavior. In order to explain the frequency dependence of the capacitance behavior after stress, a circuit model considering channel resistances and gate insulator capacitances is proposed, as shown in Fig. 5a. For the unstressed device, the model is composed of the distributed insulator capacitance (C_{in}), channel resistance (R_{ch}), junction capacitance (C_j), and contact resistance (R_C). The *C-V* behavior and the *I-V* behavior can be correlated by considering the impedance of the device in this model. As the gate voltage is much higher than V_{TH}, the channel resistance will become very small and the nodes in the channel can be viewed as short-circuited. At this time, the total impedance would be dominated by the gate insulator capacitance and all the distributed capacitance can

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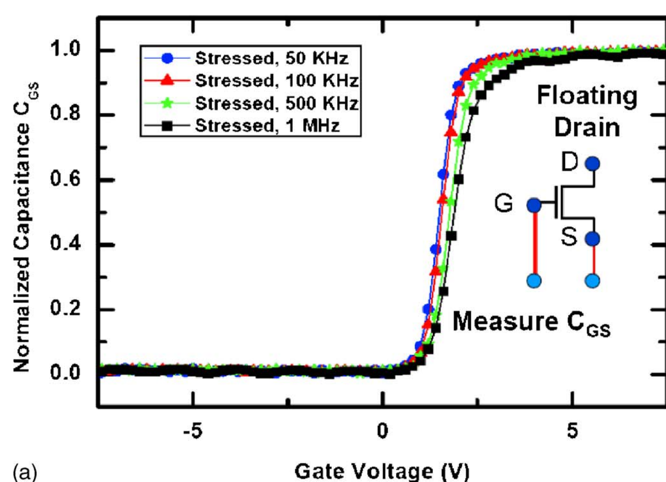


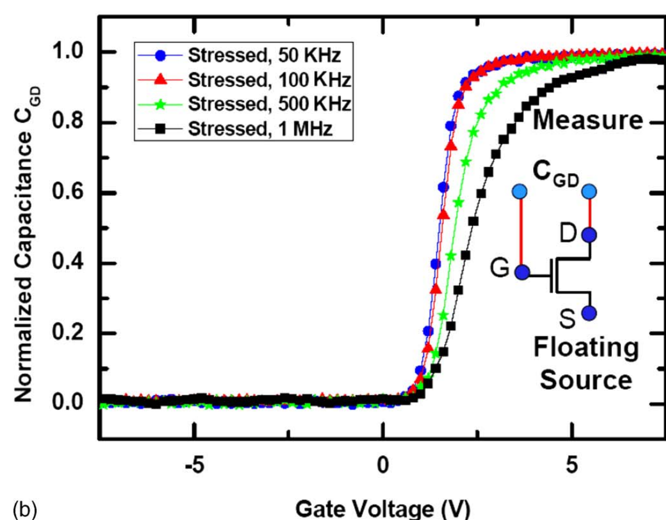
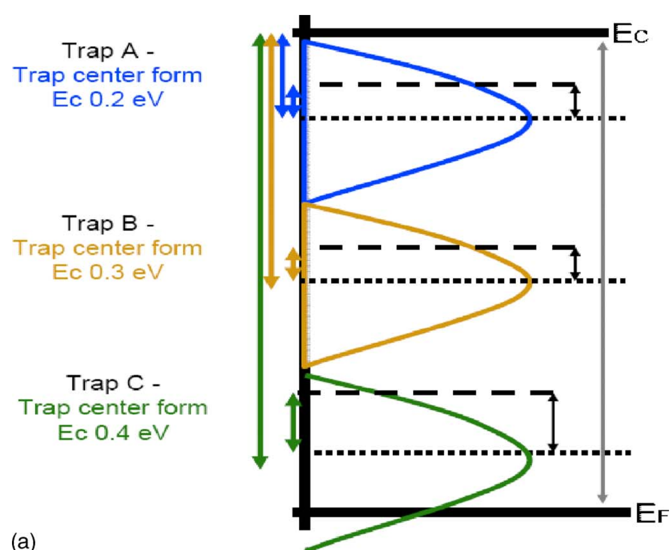
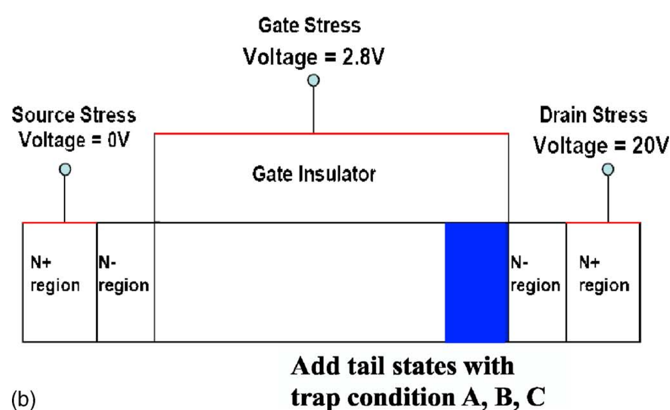


Figure 3. (Color online) Normalized C_{GS} and C_{GD} curves for the device after hot carrier stress with different frequencies of 50 kHz, 100 kHz, 500 kHz, and 1 MHz.

be measured. In other words, the measured capacitance would be the summation of all the gate insulator capacitances. As the gate voltage is far below V_{TH}, the channel resistances are so high that they would block the signal deep in the channel. Therefore, the measured *C-V* behavior in this region may actually represent the capacitance behaviors only near the edges of the channel, which may only represent the capacitance of the overlapped region between the two probed electrodes. However, for the transient region, neither the resistance nor the capacitance would dominate the impedance and hence both the effects of capacitance and resistance should be considered. Because the capacitive impedance is frequency dependent, the frequency dependence of the measured *C-V* curves shown in Fig. 3 can thus be inferred.

Figures 5b show the simulated and measured curves of the normalized capacitance C_{GS} for frequency 50 kHz and 1 MHz, while Fig. 5c shows those of the C_{GD} curves for the fresh device. The simulation of the curves is calculated from the effective impedance of the proposed model between the probed nodes with the simple math tool. To start with, first the R_{DS} curves are extracted from the I_D-V_G curves with the drain voltage at 0.1 V to find the uniform-distributed channel resistance for every gate voltage. The effective impedance between the two nodes can then be calculated with the proposed model. Via circuit theory, the capacitance between the nodes can be calculated from the real and imaginary parts of the





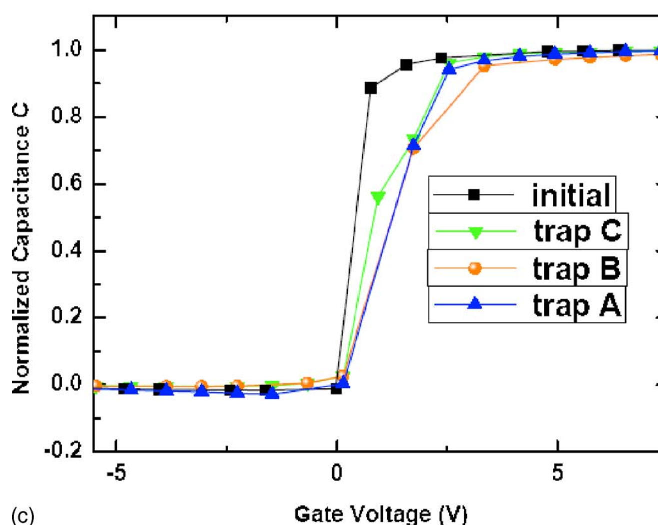


Figure 4. (Color online) The model describing the device after hot carrier stress with the state condition in (a) the bandgap and (b) the physical location, and (c) the simulated *C-V* curves for different state conditions.

effective impedance. For example, the simulation curves of C_{GS} are calculated from the effective impedance between the gate and source electrode. For the simulated curves, it can be seen that the curves for different frequencies can well depict the capacitance behavior for the positive gate voltage with the use of the simple math calculation

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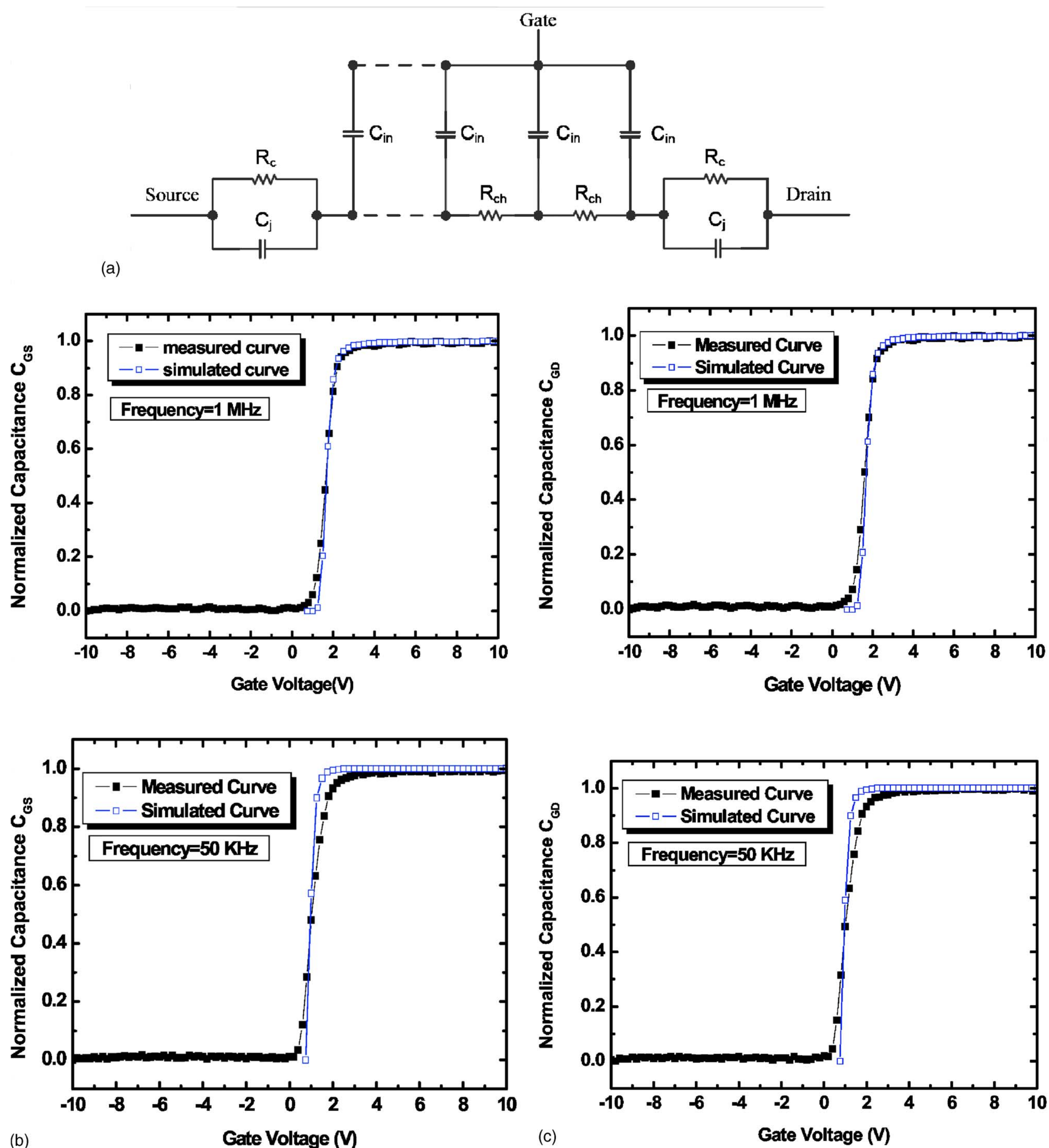

Figure 5. (Color online) (a) The proposed circuit model of the fresh poly-Si TFTs. (b) Simulated curves for the C_{GS} curves for the fresh device with frequency of 1 MHz and 50 kHz. (c) Simulated curves for the C_{GD} curves for the device with frequency of 1 MHz and 50 kHz.

tool, especially for 1 MHz frequency. This reveals that the capacitance behavior for different frequencies may just be the effect of the capacitances measured with the varying channel resistance at different gate voltages, which justifies the proposed model.

Figures 6a and b show the normalized C_{GS} and C_{GD} curves and the total resistance R_{DS} at different *C-V* measuring frequencies, where R_{DS} is extracted from the I_D-V_G curves at $V_D = 0.1$ V. For the gate voltage around V_{TH}, the channel resistance would go through a transient region and the magnitude of the channel resistance would rapidly decrease from around 10^9 to 10^4 Ω. A critical point of the impedance behavior P_c can be selected as the channel resistance R_{ch} equals the capacitance term $1/2\pi f C_{in}$, which falls in the transient region of the C_{GS} and C_{GD} curves for the measuring frequency 50 kHz and 1 MHz. The term f represents the measuring frequency. The solid arrow in Fig. 6 represents the point that the total channel resistance R_{DS} equals the capacitance term $1/2\pi f\ C_{TFT}$ for different *C-V* measuring frequencies, where C_{TFT} is about 40 fF, representing the gate insulator capacitance of the TFT. The upper dashed arrow represents the point P_A where the channel resistance R_{DS} is 10 times

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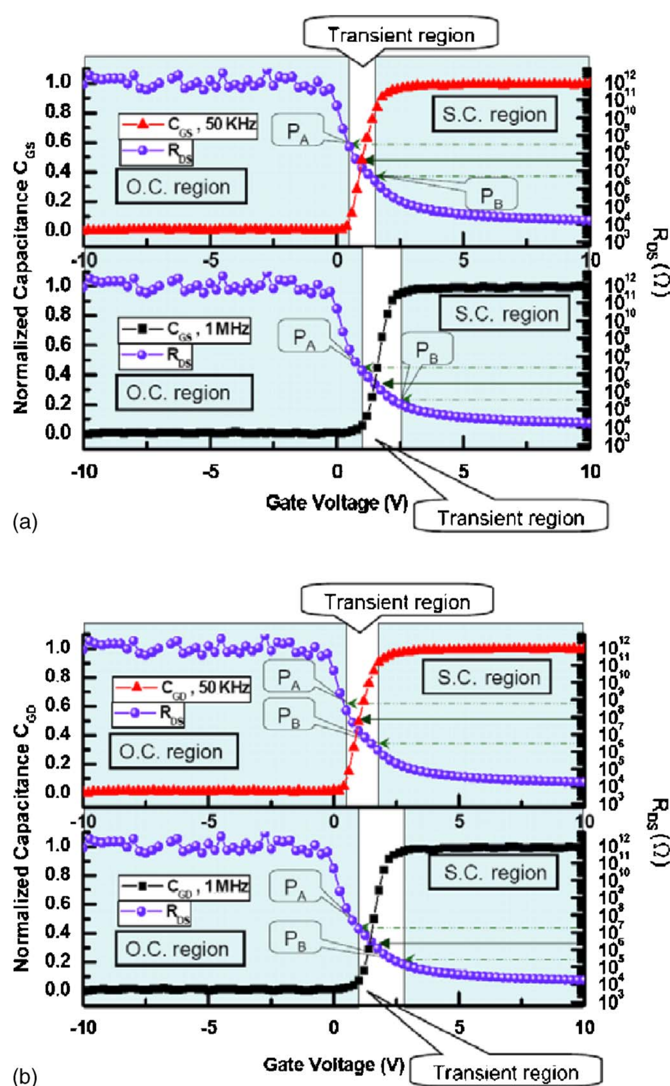

Figure 6. (Color online) (a) Normalized C_{GS} curves and R_{DS} curves at $V_D = 0.1$ V, and (b) the corresponding C_{GD} and R_{DS} curves for the fresh device.

larger than the capacitance term, and the lower dashed arrow represents the point P_B when the channel resistance R_{ch} is 10 times smaller. In Fig. 6, the dashed arrows respectively point out the 80 and 4 MΩ of the R_{DS} curve, which correspond to the impedance of C_{TFT} at the applied frequencies of 50 kHz and 1 MHz. For the gate voltage lower than P_A, the conductivity of the device is considered to be low enough that the channel resistance can be taken as open circuit and is labeled as the "O.C. (open-circuit) region." For the gate voltage larger than P_B, the channel becomes highly conductive to be considered as short circuit and is labeled as the "S.C. (short-circuit) region." Meanwhile, for the gate voltage between P_A and P_B, because the capacitive term and the resistive term of the impedance are comparable, neither of them can be ignored.

Figures 7a show the circuit model for the device after hot carrier stress. The terms C_{deg} and $R_{ch,deg}$ represent the increase of the capacitance and resistance due to the generated tail states during stress. Figure 7b shows the corresponding location in the bandgap of the capacitance C_{deg}. Because the tail states are mainly related to the operation of the gate voltage above V_{TH}, the state capacitance C_{deg} would respond at the gate voltage larger than V_{FB}. Under this gate voltage, the Fermi level is drawn near to the bottom of the conduction band E_C and then fills the capacitance C_{deg}. Figures 8a and b show the normalized capacitance characteristics of C_{GS} and C_{GD}

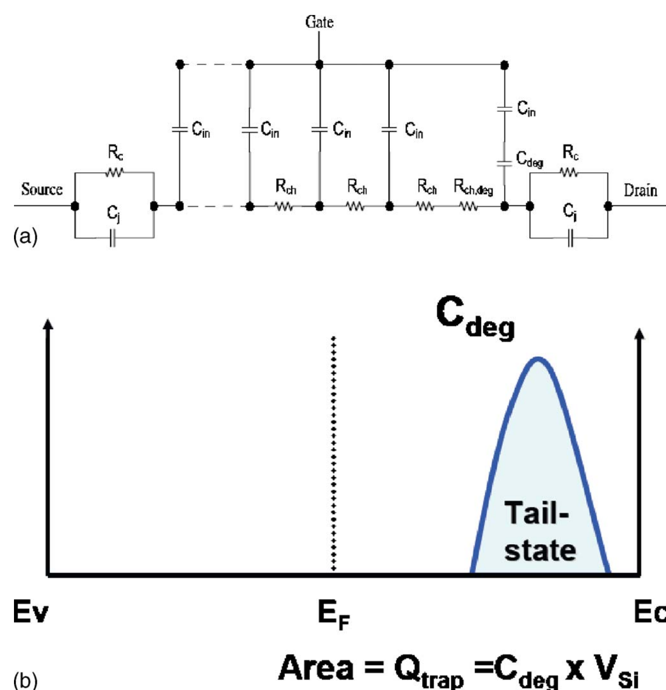

Figure 7. (Color online) (a) Proposed circuit structure for the device after hot carrier stress. (b) The corresponding location of C_{deg} in the bandgap.

with the total resistance R_{DS} extracted from the I_D-V_G curves for the device after hot carrier stress. For the low measuring frequency of 50 kHz, the capacitive term $1/2\pi f \pi C_{TFT}$ is relatively larger than the channel resistance at the gate voltage slightly larger than V_{TH}. Therefore the measured C_{GS} and C_{GD} characteristics would quickly contain the gate capacitance in the channel and saturate at C_{TFT}. Hence, the effect of the degradation component C_{deg} may not be obvious. However, for the high measuring frequency of 1 MHz, the channel resistance can be ignored until the gate voltage is much larger than V_{TH} and thus the effect of the C_{deg} components can be apparent. In other words, the degradation in the *C-V* behaviors for the device may only be observed at higher measuring frequencies, where the effect of the degraded capacitances can be obvious.

Self-heating effect.— Polysilicon TFTs, in most applications, are fabricated on glass substrates which have poor thermal conductivity. Therefore, as the applied V_{GS} and V_{DS} are high, the heat resulting from the high current flow and voltage difference in the channel may be difficult to dissipate. The accumulated heat causes the Si–H bonds to break, which in turn increases the deep states in the channel. These states apparently affect the conduction of the device near the subthreshold and the ON region.[5] Most of the previous works focus on the current-transfer characteristics of the device after self-heating stress, while very few works mention the *C-V* behaviors of this mechanism.[17] In order to find the dominant mechanism and the corresponding circuit model, the *C-V* behavior of device after self-heating stress is examined and discussed in the following section.

Figure 9 shows the *I-V* transfer characteristics for the TFT before and after the 500 s of self-heating stress. The stress condition is that both V_{GS} and V_{DS} equal 18 V. For the stressed device, it can be seen that the threshold voltage V_{TH} and the subthreshold swing increase, and the ON current decreases. Figure 10a shows the C_{GS} curves before and after stress with different frequencies, while Fig. 10b shows the corresponding curves of C_{GD}. Compared with the curves before stress, the stressed C_{GS} and C_{GD} curves exhibit two main changes, namely, the positive shift for the gate voltage near the flatband voltage V_{FB} and the increase for the gate voltage just below V_{FB}. The stretch and shift in the positive direction for the gate volt-

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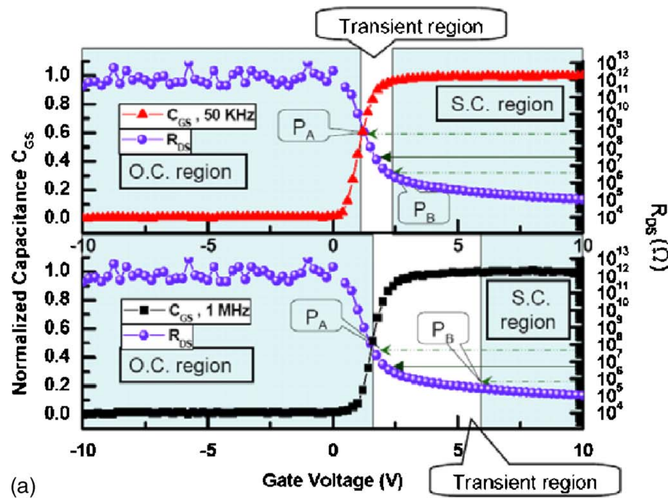
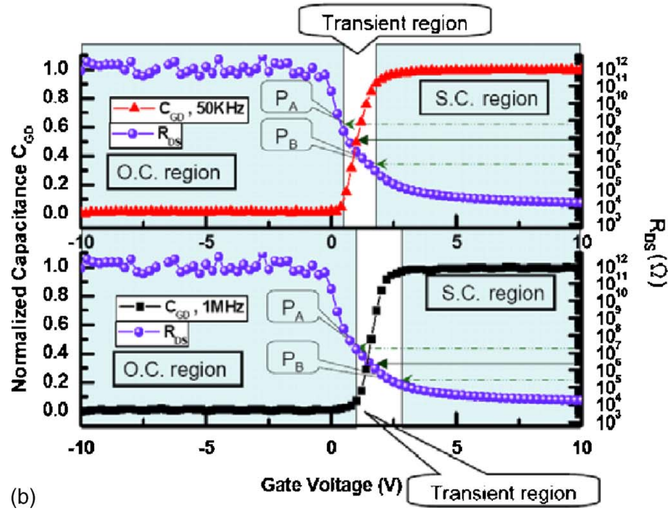


(a)



(b)

Figure 8. (Color online) (a) Normalized C_{GS} curves and R_{DS} curves at V_D = 0.1 V, and (b) the corresponding C_{GD} and R_{DS} curves for the device after hot carrier stress.

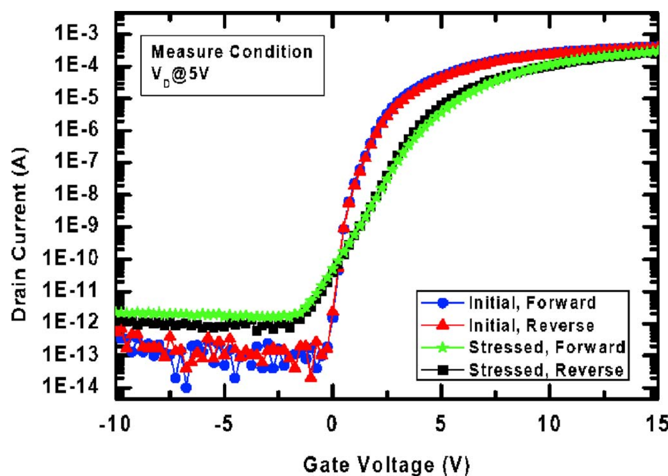
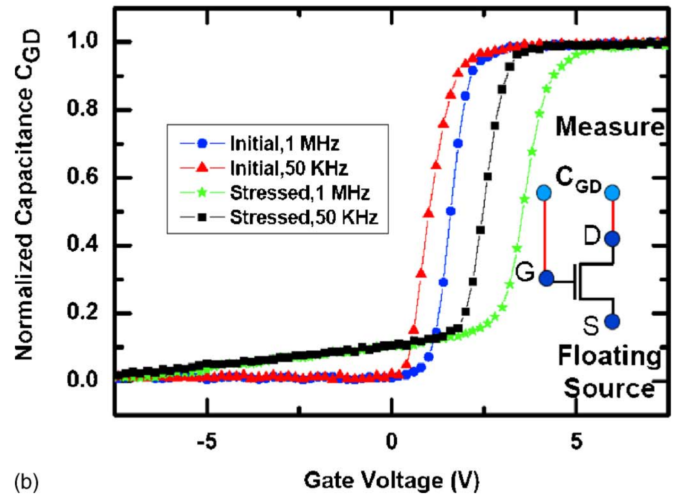


Figure 9. (Color online) Current-transfer characteristics before and after self-heating stress condition ($V_{GS} = V_{DS}$ = 18 V, 500 s) with the forward and reverse connection.

(a)



(b)

Figure 10. (Color online) (a) and (b) Normalized C_{GS} and C_{GD} curves (before and after self-heating stress) vs gate voltage at frequencies 50 kHz and 1 MHz.

age near V_{FB} can be attributed to the increase of the deep states during stress. The increases of the C-V curves for the lower gate voltage possibly come from the interface states.

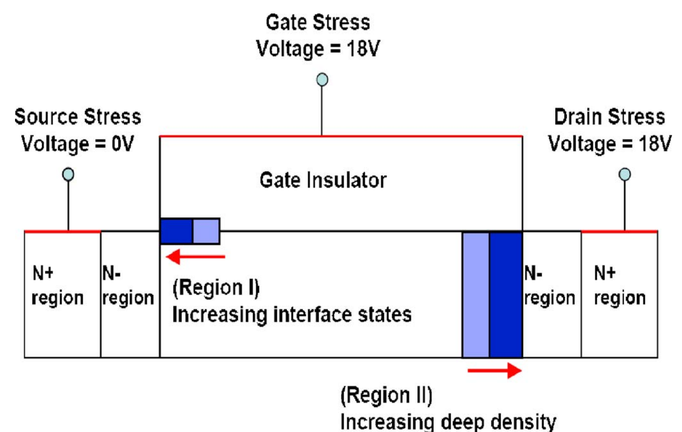


Figure 11. (Color online) The proposed degradation model in TFT structure with interface states and deep states.

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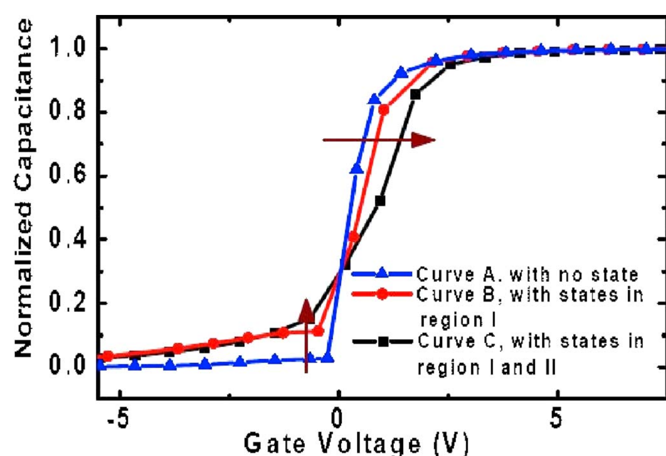

Figure 12. (Color online) Simulation results of the normalized *C-V* curves with different state conditions (region I and region I and II).

To verify this inference, a 2D numerical simulation program DESSIS is applied again to simulate the device characteristics. The model of the cross section of the device after self-heating stress is shown in Fig. 11. The deep states in the poly-Si film are modeled by a Gaussian distribution near the midgap. The peak value of the deep state density changes from 5×10^{18} to 3×10^{17} cm^{-3} in the range of 0.3 um from the drain edge, corresponding to the temperature distribution during self-heating stress.[18] The interface states of 1×10^{15} cm^{-2} decreasing to 1×10^{14} cm^{-2} are spatially arranged from the source edge, reflecting the electric field between the gate and source during stress. Figure 12 shows the simulation results with different degraded regions in the device. Curve A is the *C-V* curve with no degraded region, while curve B is the one with interface states near the source region. Comparing to curve A, curve B increases drastically for the gate voltage below V_{FB}. This reveals that the interface states between the source and gate influence the induced carriers in the channel depletion and weak inversion regions. Curve C further includes the increase of deep states in the poly-Si film near the drain. The difference from curve B is that the curve stretches and shifts in the positive direction near V_{FB}. The similarity between the simulated curves and the measured C_{GS} and C_{GD} curves reveals that the proposed model for the device after self-heating stress should be correct and applicable. However, the different degree of the increase of the C_{GS} and C_{GD} curves at lower gate voltage still may not be explained by the simulation results.

Figure 13a shows the proposed circuit model of the device after self-heating stress. The capacitance C_{deep} is added to the device, representing the increase of the deep states during stress. In addition, C_{deg} is also introduced to represent the capacitance corresponding to the interface states induced by the high voltage difference V_{GS} during stress. Figure 13b shows the corresponding location in the bandgap of the capacitance C_{deep} and C_{deg}. Because the deep states in the channel would affect the operation for the gate voltage near V_{FB}, the position of C_{deep} is located near the Fermi level E_F in the bandgap. Because C_{deg} is found to influence the conduction for the gate voltage below V_{FB}, the corresponding position of C_{deg} is set to locate partly below E_F. Figure 14a and b shows the normalized capacitance C_{GS} and C_{GD} and the total resistance R_{DS} extracted from the I_D-V_G curves. In the O.C. region, because all the channel resistances are taken as opened, the model is reduced to only the capacitances in the device. Thus, the C_{deg} resulting from the interface states and the C_{deep} from the self-heating effect would lead to the increase of the C_{GS} and C_{GD} curves for the lower gate voltage, respectively. In this region, the different frequency dependences for C_{GS} and C_{GD} curves reflect the different responses of the states near the source and the drain, respectively. As the gate voltage increases, two effects make the C_{GS} and C_{GD} curves change with gate voltage. First, the Fermi level is drawn near to E_C and the interface states are thus getting filled. Second, the channel resistance would also be gate voltage dependent. Hence, the stretch and shift of the *C-V* curves in the transient region may include the effect of the increase of the C_{deep} and the decrease of R_{ch}. For the higher gate voltages, all the states are filled and the channel resistances are very low, making the measured capacitance C_{GS} and C_{GD} saturate at C_{TFT}. The proposed model may fairly explain the frequency-dependent degradation of the capacitance curves after both the hot carrier and self-heating stress conditions. It would be of practical importance in further understanding the reliability issues of LTPS TFTs.

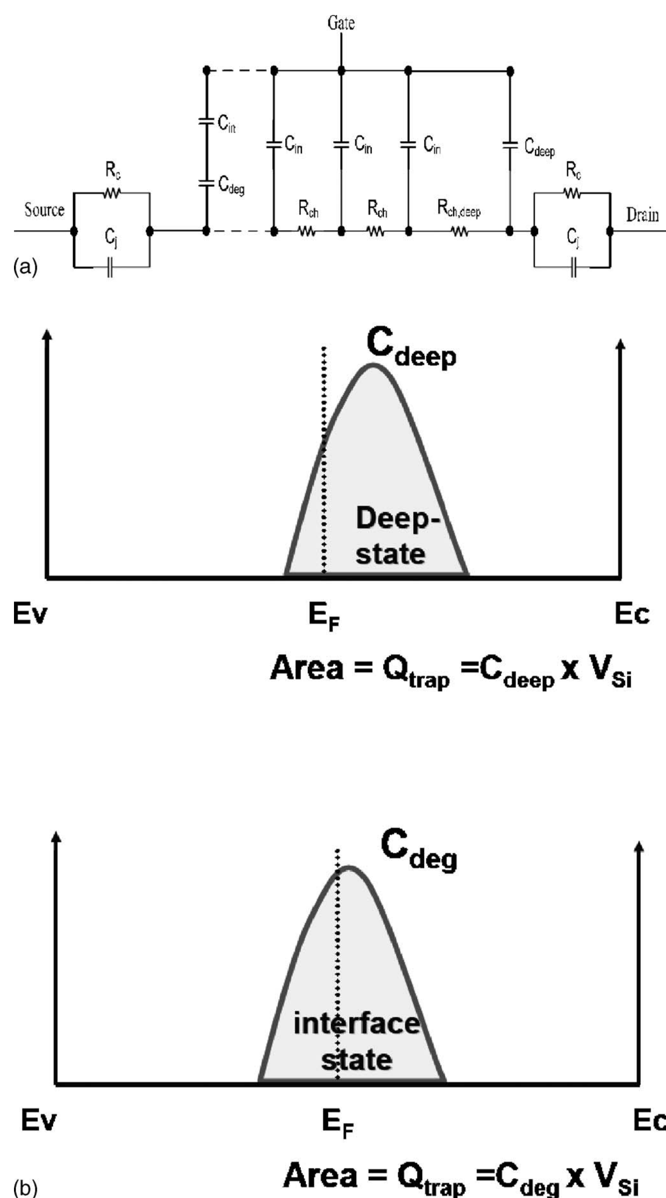

Figure 13. (a) The proposed circuit model of the poly-Si TFTs after self-heating stress. (b) The corresponding location of C_{deg} and C_{deep} in the bandgap.

Conclusion

In this work, the degradation of LTPS TFTs under hot carrier and self-heating stress was investigated using the *C-V* method. For the hot carrier stress, it is found that the degradation of the C_{GD} curves

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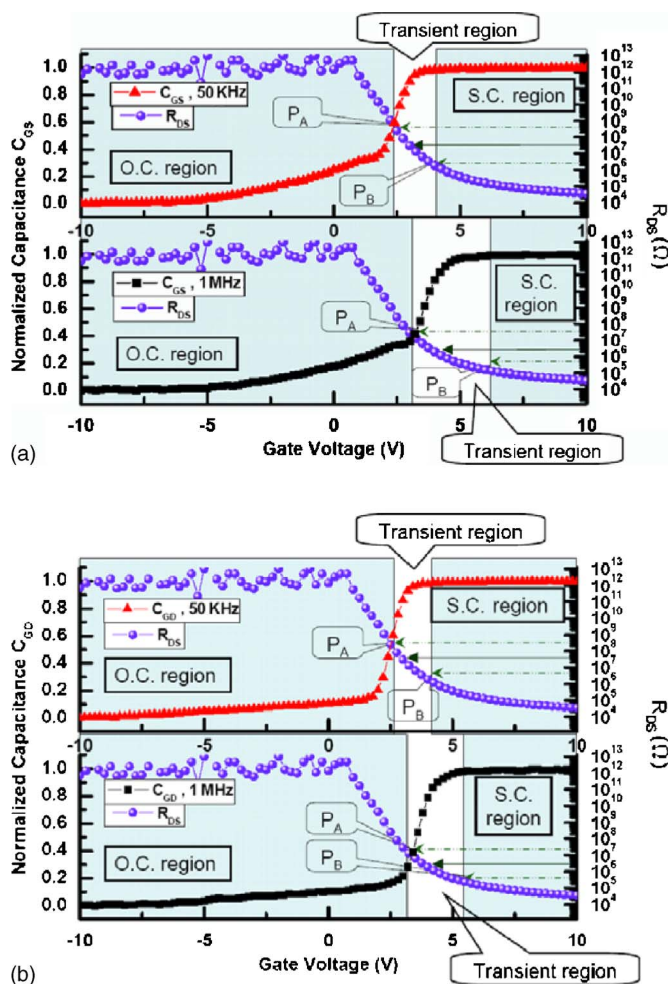

Figure 14. (Color online) (a) The normalized C_{GS} curves and the R_{DS} curves at $V_D = 0.1$ V, and (b) the corresponding C_{GD} and R_{DS} curves for the device after self-heating stress.

would exhibit apparent frequency dependence for different measuring frequencies. A circuit model connecting the *I-V* and *C-V* behaviors is proposed to explain the anomalous *C-V* behavior. With this model, the *C-V* behaviors can be divided into three regions by comparing the resistive term and the capacitive term of the total impedance. It is proposed that the frequency dependence of the C_{GD} curves after hot carrier stress reflects the transient behaviors of the channel resistances and capacitances. In addition, it is discovered that the self-heating stress would cause the increase of deep states in the poly-Si film near the drain and the interface states at the interface in the source region. The proposed model may further reveal that the measured capacitance exhibits the real capacitive behaviors of the states only in the O.C. regions, while the transient region reflects both the effects of resistances and capacitances. This finding would provide important information for further studies of the *C-V* behaviors and its relation to the *I-V* behaviors of LTPS TFTs.

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