*Journal of The Electrochemical Society*, **154** (7) H619-H622 (2007)
0013-4651/2007/154(7)/H619/4/$20.00 © The Electrochemical Society



# Two-Bit Lanthanum Oxide Trapping Layer Nonvolatile Flash Memory

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This paper describes the two-bit characteristics of SONOS-type memories prepared using lanthanum oxide, a high-*k* dielectric material, as the trapping layers. We used "channel hot-electron injection" for programming and "band-to-band hot-hole injection" for erasing to perform the memory operations. We observed large memory windows, a relatively high P/E speed, and good retention characteristics for these SONOS-type memories. It appears that $La_2O_3$ is an excellent candidate for use as the trapping layer in SONOS-type memories.
 [DOI: 10.1149/1.2737345] 

Manuscript submitted July 18, 2006; revised manuscript received March 15, 2007. Available electronically May 15, 2007.

Silicon–oxide–nitride–oxide–silicon (SONOS) charge-trapping-based nonvolatile memories have received a considerable amount of interest recently.[1-3] Obtaining nonvolatile, low-power, fast memories with short dimensions remains a key challenge in the electronics industry. According to the International Technology Roadmap for Semiconductors (ITRS),[4] the key issue for floating-gate nonvolatile semiconductor memories is the scaling of the tunneling oxide; the stress-induced leakage current (SILC), which can discharge the whole floating-gate memory with even one single defect, becomes a severe problem at very thin tunneling oxide thicknesses. This scaling issue remains a formidable challenge, especially for emerging system-on-chip (SOC) integrated circuit designs in which the programming voltage must be scaled for the nonvolatile memories to be compatible with low-voltage logic circuits. High-*k* dielectric materials, such as hafnium oxide ($HfO_2$) and lanthanum oxide ($La_2O_3$), are promising candidates to replace $Si_3N_4$ films as the charge trapping layer of SONOS-type flash memories.[5] Such high-*k* dielectric films are expected to exhibit better charge trapping characteristics than are displayed by conventional $Si_3N_4$ films; their sufficient densities of trap states and deep trap energy levels should result in longer retention times.[6,7] This feature suggests that $HfO_2$ will be more practical for further scaling of the tunnel oxide to enhance the performance and more suitable for the development of SONOS-type memories that perform multibit operations.[8,9] Moreover, a greater voltage drop at the tunnel oxide can be obtained when using the high-*k* material as the trapping layer. Therefore, low-power, high-speed operation at short dimensions is achievable for high-*k* SONOS-type memories.

In this study, we prepared high-*k* SONOS-type memories incorporating lanthanum oxide ($La_2O_3$) as the trapping layer. These memories exhibit good characteristics: considerably large memory windows, high speed programming/erasing, good retention times, high endurance, and low disturbance.

## Device Fabrication

Figure 1 displays the structure and process flow for the preparation of the $La_2O_3$ high-*k* memories. The fabrication of the $La_2O_3$ memory devices involved the LOCOS isolation process on p-type, 5–10 Ω cm, (100) 150 mm silicon substrates. First, a 2 nm thick tunnel oxide was grown thermally at 1000°C in a vertical furnace system. Next, a 4 nm thick lanthanum oxide layer was deposited using the E-gun method with $La_2O_3$ targets. Subsequently, the samples were subjected to RTA treatment under an $O_2$ ambient at 900°C for 1 min. A blocking oxide (ca. 7 nm) was deposited using high density plasma chemical vapor deposition (HDPCVD) followed by a $N_2$ densification process at 900°C for 1 min. Poly-si deposition, gate lithography, gate etching, source/drain (S/D) implanting, substrate and contact patterning, followed by the rest of the subsequent standard complementary metal oxide semiconductor (CMOS) procedure, were then performed to complete the fabricating of the $La_2O_3$-containing high-*k* SONOS-type memory devices.

## Characterization Results and Discussion

Figure 2 displays cross-sectional high-resolution transmission microscopy (HRTEM) images of the gate stacks of the $La_2O_3$ flash memory. For this SONOS-type structure, the thicknesses of the tunnel oxide, $La_2O_3$ trapping, and blocking oxide layers were 2, 4, and 7 nm, respectively. To operate our $La_2O_3$-containing SONOS-type memory, we employed channel hot-electron injection and band-to-band hot-hole injection for programming and erasing, respectively. By using these "hot" carrier injections, we can improve the program/erase speed for our memory operation.[10,11] All devices described in this paper had dimensions (L/W) of 2/1 μm. Figure 3 demonstrates the feasibility of performing two-bit operation with our $La_2O_3$-containing SONOS-type memory through a forward read/reverse read scheme in a single cell.[12] From the $I_{ds} - V_{gs}$ curves, it is clear that we could employ forward and reverse reads to detect the information stored in the programmed bit1 and bit2, respectively. The read operation was achieved using a reverse read scheme. Table I summarizes the bias conditions for two-bit operation.

Figure 4 presents the program characteristics as a function of the pulse width under different operating conditions. Both the source and substrate terminals were biased at 0 V. The "$V_t$ shift" is defined as the change in the threshold voltage of a device between its programmed and erased states. With $V_d$ and $V_g$both set at 9 V, we found that a relatively high speed ($t$ = 100 μs) programming performance was possible with a memory window of ca. 2.2 V. Meanwhile, Fig. 5 displays the erase characteristics as a function of the operating voltage. Again, an excellent erase speed of the memory

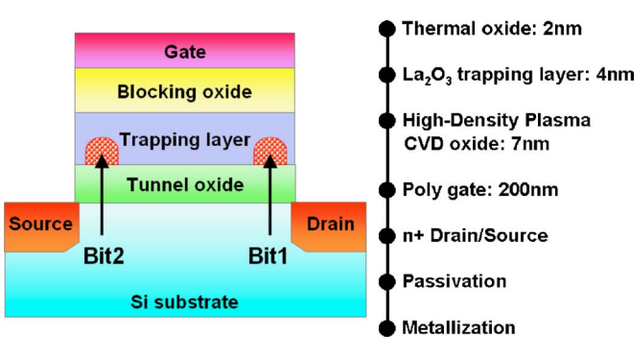


**Figure 1.** (Color online) Schematic representation of the $La_2O_3$-containing SONOS-type flash memory cell structure and localized charge storage.

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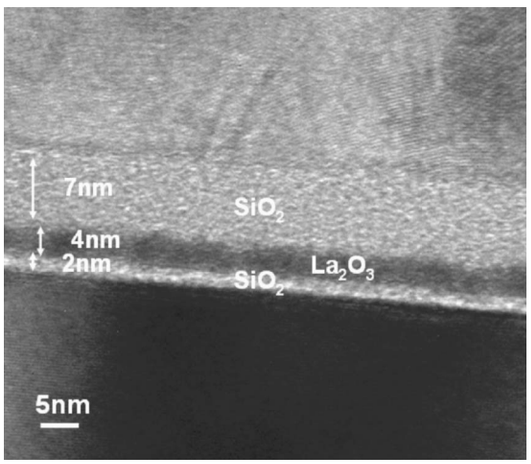


**Figure 2.** HRTEM image (plan view) of the $La_2O_3$-containing SONOS-type memory.

window (ca. 10 ms) was obtained. More importantly, we observed only a very small degree of over-erasing; because we used band-to-band hot-hole injection, the vertical electric field decreased upon decreasing the number of trapped electrons in the trapping layer during erasing, and hole injection into the trapping layer was reduced significantly.

Figure 6 illustrates the retention characteristics observed at temperatures of 25, 85, and 125°C. At room temperature, the charge loss of the memory incorporating the $La_2O_3$ trapping layer was below 19%, which is an estimation based on an extrapolation at $10^8$ s; this behavior is probably related intimately to the trap energy level in high-$k$ dielectrics.[13] The retention behavior deteriorated, however, as the temperature increased: we obtained 38 and 63% charge losses at 85 and 125°C, respectively, after $10^8$ s. We calculated the activation energy of the traps in the $La_2O_3$ layer of a fresh device. Activation energy tracing is widely used to characterize the Arrhenius relation extracted from the temperature dependence of charge loss in a nonvolatile memory as a function of time. For a given charge-loss threshold criterion (in our case, 20%), the failure rates obtained at higher temperatures (125–200°C), with five measurements at each temperature, were then extrapolated to the nominal operating conditions. We obtained an extracted activation energy of 1.25 eV for the

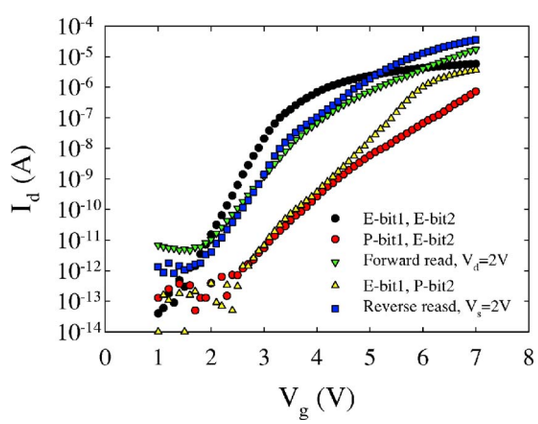


**Figure 3.** (Color online) $I_{ds} - V_{gs}$ curves of the two-bit memory in a cell; forward read and reverse read for programmed bit1 and programmed bit2.

**Table I. Operating principles and bias conditions utilized during the operation of the $La_2O_3$-containing SONOS-type memory cell.**

| | | Program | Erase | Read |
|---|---|---|---|---|
| Bit 1 | $V_g$ | 9 V | −5 V | 4 V |
| | $V_d$ | 9 V | 9 V | 0 V |
| | $V_s$ | 0 V | 0 V | >3 V |
| Bit 2 | $V_g$ | 9 V | −5 V | 4 V |
| | $V_d$ | 0 V | 0 V | >3 V |
| | $V_s$ | 9 V | 9 V | 0 V |

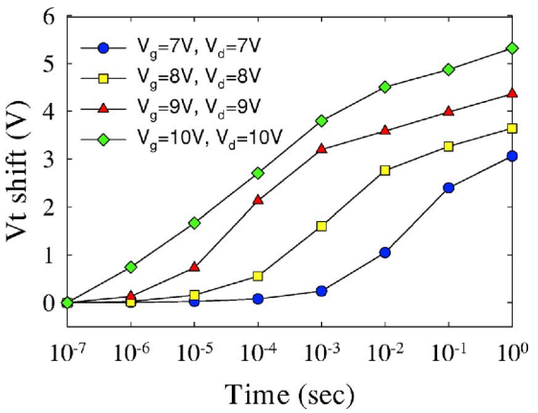


**Figure 4.** (Color online) Program speeds of the $La_2O_3$-containing SONOS-type memory.

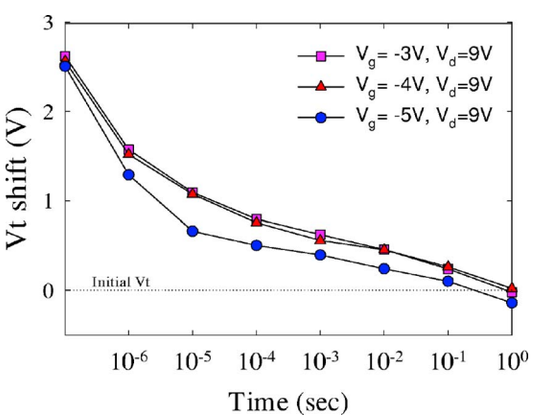


**Figure 5.** (Color online) Erase speeds of the $La_2O_3$-containing SONOS-type memory.

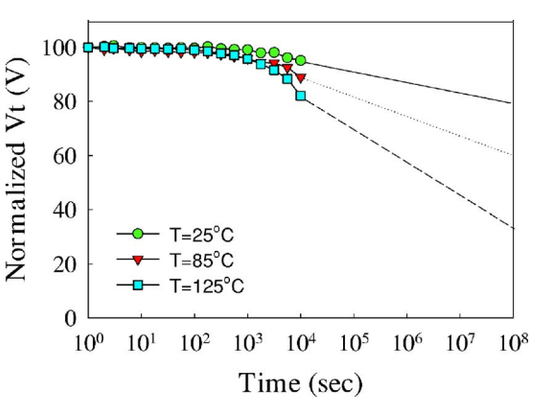


**Figure 6.** (Color online) Retention of the $La_2O_3$ SONOS-type memory at various temperatures. Charge losses of 22 and 40% occurred at 25 and 125°C, respectively, after $10^8$ s.

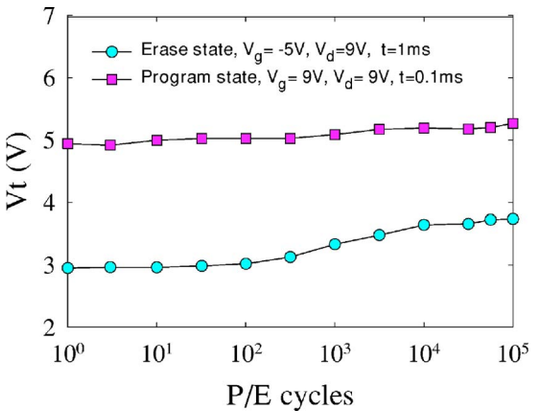


**Figure 7.** (Color online) Endurance characteristics of the $La_2O_3$-containing SONOS-type memory up to $10^5$ P/E cycle.

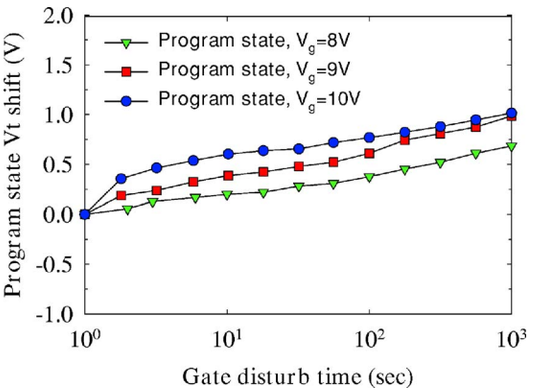


**Figure 9.** (Color online) Gate disturbance characteristics of the $La_2O_3$-containing SONOS-type memory. A threshold voltage shift of only 1 V occurred after stressing at values of $V_g$ of 10 V and $V_s$, $V_d$, and $V_{sub}$ of 0 V for 1000 s.

$La_2O_3$ trapping layer. Obviously, this value is higher than those reported previously for conventional SONOS memories.[14-16]

Figure 7 displays the endurance characteristics after $10^5$ P/E cycles (programming conditions: $V_g = V_d = 9$ V for 100 μs; erasing conditions: $V_g = -5$ V, $V_d = 9$ V for 1 ms). A slight memory window narrowing occurred and individual threshold voltage shifts become visible in the program and erase states after $10^2$ cycles. This finding suggests the formation of operation-induced trapped electrons. Certainly, this feature is related intimately to the use of the ultra-thin tunnel oxide and the minute amount of residual charge remaining in the $La_2O_3$ layer after cycling.

Figure 8 presents the programming drain disturbance of our $La_2O_3$-containing SONOS-type memory. Three different drain voltages ($V_d = 5$, 7, and 9 V) were applied in the programming drain disturbance measurements at room temperature. We observed that a sufficient programming drain disturb margin exists ($\Delta V_t < 1$ V), even after programming at a value of $V_d$ of 9 V under room temperature and after stressing for 1000 s. Figure 9 displays the gate disturbance characteristics in the erasing state. Gate disturbance may occur during programming for cells sharing a common word-line while one of the cells is being programmed. We observed a threshold voltage shift of only 0.9 V under the following conditions: $V_g$10 V; $V_s = V_d = V_{sub} = 0$ V; stressed for 1000 s. Because of the small voltage drop at the tunnel oxide when using the serial capacitor voltage divider model, this memory exhibits good gate disturbance characteristics even with such a thin tunnel oxide.

Figure 10 demonstrates the read disturbance-induced erase-state threshold voltage instability in a localized $La_2O_3$ trapping storage flash memory cell under several operation conditions. For two-bit operation, the applied bit-line voltage in a reverse-read scheme must be sufficiently large (>2 V) to permit "read through" of the trapped charge in the neighboring bit. The read-disturb effect is the result of two factors: the word-line and the bit-line. The word-line voltage during reading may enhance the room-temperature drift in the neighboring bit.[12] On the other hand, a relatively large read bit-line voltage may cause unwanted channel hot-electron injection and, subsequently, result in a significant threshold voltage shift of the neighboring bit. In our measurements, the gate and drain biases were applied and the source was grounded. The results clearly demonstrate that almost no read disturbance occurred in our $La_2O_3$ flash memory under low-voltage reading ($V_g = 3$ V; $V_d = 2.5$ V). For a larger memory window, we found that only a small read disturbance (ca. 0.3 V) occurred after operation at a value of $V_d$ of 4 V for 1000 s at 25°C.

## Conclusion

In this study, we investigated the memory effect during the performance of $La_2O_3$ SONOS-type memories. These devices exhibited good characteristics in terms of their large memory windows, high programming/erasing speeds, good retention times, excellent endurance, and two-bit operation. Hence, $La_2O_3$ is an excellent candidate for use in the trapping layers of SONOS-type memories.

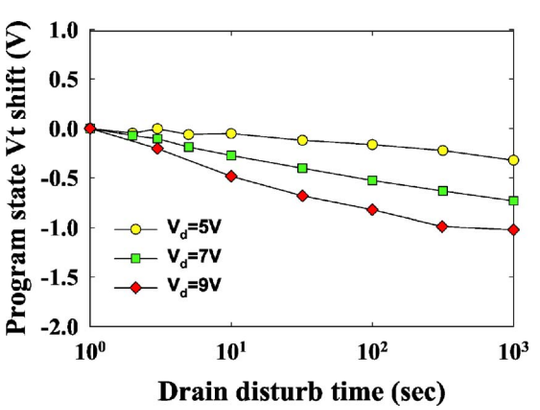


**Figure 8.** (Color online) Drain disturbance characteristics of the $La_2O_3$-containing SONOS-type memory. After 1000 s at 25°C, a drain disturb margin of only 1 V was observed.

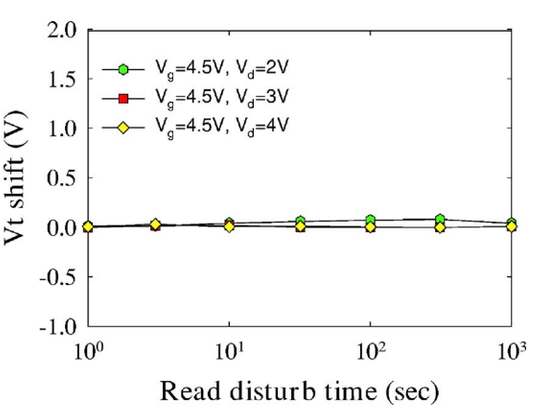


**Figure 10.** (Color online) Read disturbance characteristics of the $La_2O_3$-containing SONOS-type memory devices. No significant $V_t$ shift occurred for values of $V_d$ below 4 V, even after 1000 s at 25°C.

## Acknowledgment

This project was sponsored by the National Science Council, Taiwan, under contract no. 942215E009070.

*The National Nano Device Laboratories assisted in meeting the publication costs of this article.*

## References

1. T. S. Chen, K. H. Wu, H. Chung, and C. H. Kao, *IEEE Electron Device Lett.*, **25**, 205 (2004).
2. T. Sugizaki, M. Kobayashi, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, H. Tanaka, T. Nakanishi, and Y. Nara, in *Proceedings of the IEEE Non-Volatile Semiconductor Memory Workshop*, IEEE, p. 60 (2003).
3. T. Baron, B. Pellissier, L. Perniola, F. Mazen, J. M. Hartmann, and G. Polland, *Appl. Phys. Lett.*, **83**, 1444 (2003).
4. The International Technology Roadmap for Semiconductors (ITRS), p. 27 (2001).
5. T. Sugizaki, M. Kobayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, in *Proceedings of the VLSI Symposium Technical Digest*, p. 27 (2001).
6. T. Sugizaki, M. Kobayashi, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, H. Tanaka, T. Nakanishi, and Y. Nara, in *Proceedings of the IEEE Non-Volatile Semiconductor Memory Workshop*, IEEE, p. 60 (2003).
7. Y. N. Tan, W. K. Chim, W. K. Choi, M. S. Joo, T. H. Ng, and B. J. Cho, *Tech. Dig. - Int. Electron Devices Meet.*, **2004**, 889.
8. Y.-H. Lin, C.-H. Chien, C.-T. Lin, C.-Y. Chang, and T.-F. Lei, *IEEE Electron Device Lett.*, **26**, 154 (2005).
9. D. Montanari, J. Van Houdt, D. Wellekens, G. Vanhorebeek, L. Haspeslagh, L. Deferm, G. Groeseneken, and H. E. Maes, in *IEEE Nonvolatile Memory Technology Conference*, IEEE, p. 80 (1996).
10. P. Pavan, R. Bez, P. Olivo, and E. Zanoni, *Proc. IEEE*, **85**, 1248 (1997).
11. A. Thean and J.-P. Leburton, *IEEE Potentials*, **21**, 35 (2002).
12. W. J. Tsai, C. C. Yeh, N. K. Zous, C. C. Liu, S. K. Cho, T. Wang, S. C. Pan, and C. Y. Lu, *IEEE Trans. Electron Devices*, **51**, 434 (2004).
13. W. J. Zhu, T.-P. Ma, T. Tamagawa, J. Kim, and Y. Di, *IEEE Electron Device Lett.*, **23**, 97 (2002).
14. B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, *IEEE Electron Device Lett.*, **21**, 543 (2000).
15. H. Kameyama, Y. Okuyama, S. Kamohara, K. Kubota, H. Kume, K. Okuyama, Y. Manabe, A. Nozoe, H. Uchida, M. Hidaka, and K. Ogura, in *Reliability Physics Symposium Proceedings*, p. 194 (2000).
16. W. H. Lee, D.-K. Lee, Y.-M. Park, K.-S. Kim, K.-O. Ahn, and K.-D. Suh, in *Reliability Physics Symposium Proceedings*, p. 57 (2001).