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Bias Temperature Instabilities for Low-Temperature Polycrystalline Silicon Complementary Thin-Film Transistors

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The degradation mechanisms of both negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI) were studied for low-temperature polycrystalline silicon complementary thin-film transistors. Measurements show that both NBTI and PBTI are highly bias dependent; however, the effect of the temperature is only functional on the NBTI stress. Furthermore, instead of interfacial trap-state generation during the NBTI stress, the PBTI stress passivates the interface trap states. We conclude that the diffusion-controlled electrochemical reactions dominate the NBTI degradation while charge trapping in the gate dielectric controls the PBTI degradation.
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Due to their high potential for realization of system on panel (SOP), low-temperature polycrystalline silicon complementary thin-film transistors (LTPS CTFTs) have attracted much research interest recently.[1] The major advantages of LTPS CTFTs over amorphous-Si TFTs are their higher field-effect mobility and better stability. The stability of LTPS CTFTs is of significant importance from the fabrication technology point of view and as a long-term reliability concern.[2] Unlike the functionality for pixel switching, the peripheral driving circuits operate with a relatively high duty cycle. Accordingly, the p-channel and n-channel TFTs are subjected to negative and positive bias stress, respectively. Figure 1 gives a more detailed picture of the correlated information, and presents the bias conditions of a complementary metal oxide semiconductor (CMOS) inverter for driving circuit operation. Under its operating parameters, an "0" input state will change the output state to "1" while the p-metal oxide semiconductor field-effect transistor (MOSFET) will be under negative bias stress. Similarly, a "1" input state will force the n-channel TFTs to experience positive bias stress.

In MOSFETs, negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI) have been found to be important issues for reliability.[3-5] NBTI is significant for p-MOSFETs, because it is highly associated with the generation of both interface trap states and positive fixed-oxide charges. It is believed that the diffusion-controlled electrochemical reactions between the holes and the hydrogen species contribute to the NBTI degradation. That is, whenever we perform a negative bias stress on p-MOSFETS, holes will accumulate at the SiO_2/Si interface and react with the hydrogen species which were weakly bound to the Si atoms. The dissociation of hydrogen will then generate interface trap states. In addition, the dissociated-hydrogen species diffuse into the gate oxide and react with it, forming OH groups bonded to Si atoms and resulting in the generation of positive fixed-oxide charges.[6] PBTI degradation originates from electron tunneling into the gate dielectric, making the threshold voltage of the n-channel devices shift. This is especially true for high-*k* dielectric devices, due to their high density of trap states.[7-9] Although PBTI is insignificant for n-MOSFETs with thermally grown silicon-dioxide dielectrics, the effect is important for the LTPS TFTs that have a high density of weak bonds in their low-temperature fabricated gate dielectrics, and should be taken as a reliability issue for n-channel LTPS TFTs. However, few investigations have been conducted into the PBTI in n-channel TFTs, and the mechanisms that induce instabilities in LTPS CTFTs are still not clear. Because the driving circuit is designed using a CTFT structure, mechanisms that dominate the instabilities of LTPS TFTs should be identified to more precisely predict the lifetime.

In this study, the bias temperature measurements were performed. We found that the bias temperature instabilities are very important in LTPS CTFTs. Moreover, the mechanisms that force the instabilities of n- and p-channel TFTs were theoretically analyzed, verified, and successfully demonstrated to be useful for LTPS TFT driving circuitry design.

Experimental

The LTPS CTFTs were fabricated on glass substrates. First, a 40 nm thick amorphous-Si layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) clusters on a SiO_2 buffer layer and then crystallized into polycrystalline silicon film by excimer laser annealing. For the p-channel TFTs, the gate dielectric was deposited with an equivalent 100 nm thick SiO_2 layer after defining the active region. Mo was then deposited and patterned as the gate electrode. The self-aligned source and drain were formed by plasma doping. For the n-channel devices, the source and drain were first formed after defining the active region, and the self-aligned lightly doped source and drain were formed after gate patterning. Then, hydrogenation was performed on the LTPS CTFTs with NH_3 plasma treatment at 300°C to passivate the dangling bonds at the poly-

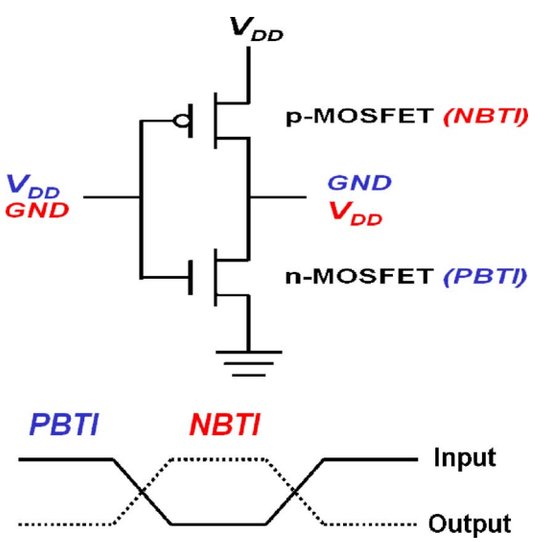

Figure 1. (Color online) Bias conditions of a CMOS inverter during circuit operation.

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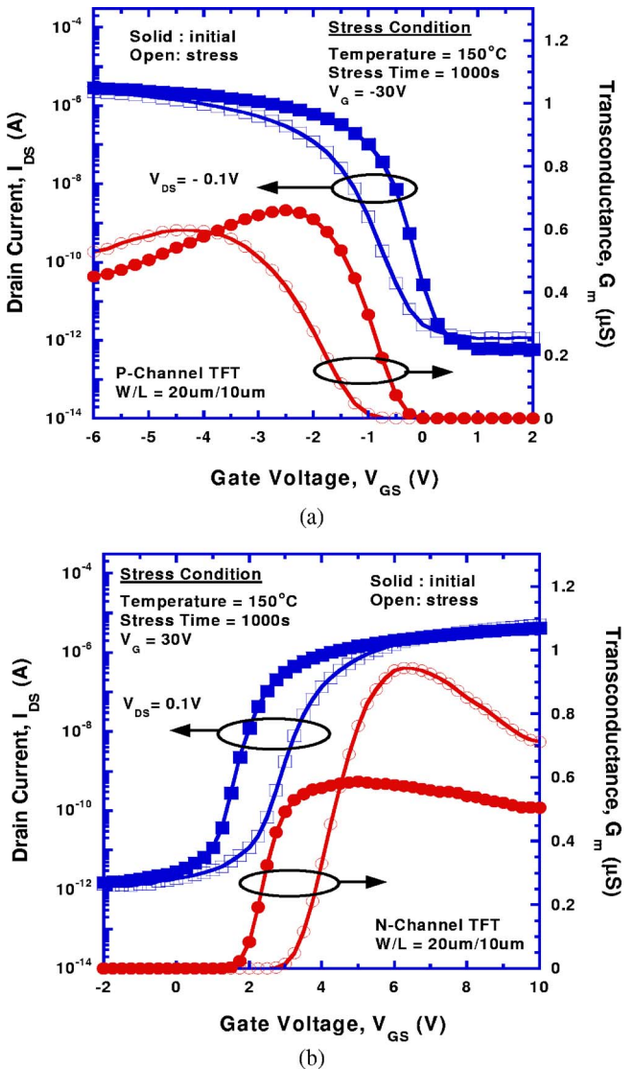


Figure 2. (Color online) Transfer characteristics of the (a) p-channel and (b) n-channel TFTs before and after stress.

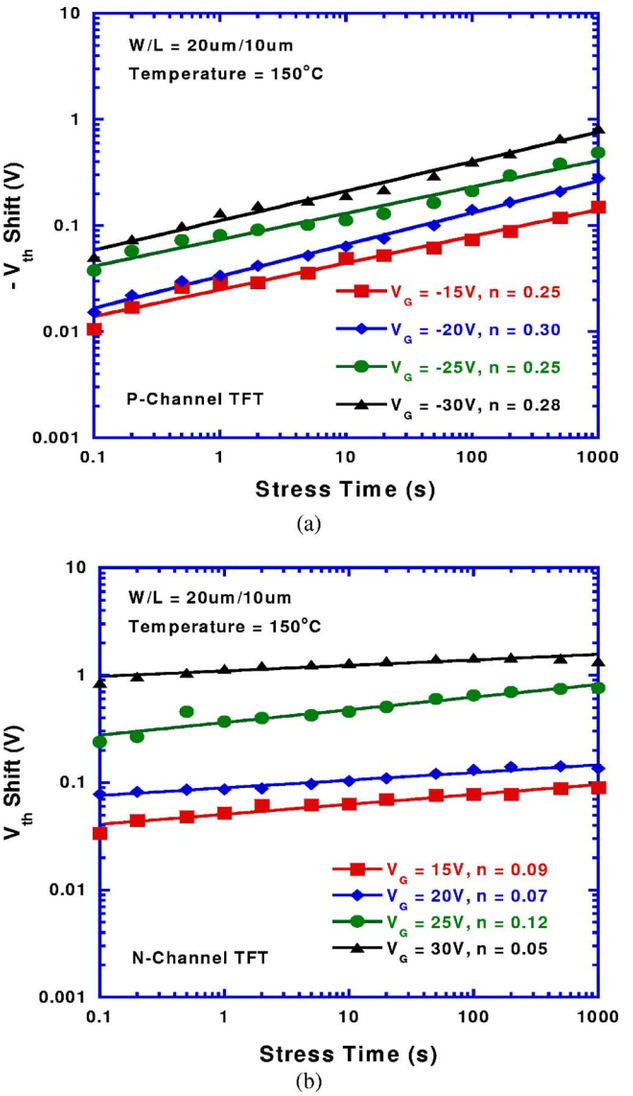


Figure 3. (Color online) Time dependence of the threshold-voltage shift of (a) p-channel and (b) n-channel TFTs under various stress voltages.

Si/SiO_2 interface and in the grain boundaries. Interlayer dielectric was deposited on all of the devices and densified. The dopants were also activated during the densification of the interlayer dielectric. Finally, after contact hole opening, interconnection metal was deposited and patterned.

In the measurement, the bias temperature instability tests were performed under substrate temperatures of 25–150°C, and a dc voltage in the range of ±15 to ± 30 V was applied to the gate with the source and drain grounded. The transfer and output characteristics of CTFTs with a width (W)/length (L) equal to 20/10 μm were extracted using the HP 4156B semiconductor analyzer.

Results and Discussion

Figures 2a and b show the effect of NBTI/PBTI stress on the transfer characteristics of the p-channel/n-channel TFTs. We found that the absolute values of the threshold voltages ($|V_{th}|$) increase after both the NBTI and PBTI stresses are applied. The subthreshold swing (S) degrades after the NBTI stress for p-channel TFT, indicating that the NBTI stress generates more interface trap states in the device. Note, however, that the field-effect mobily (μ_{FE}) increases after the PBTI stress, indicating that the bias temperature stresses affect p- and n-channel TFTs in different ways. That is, instead of the interface trap-state generation in p-channel TFTs under NBTI stress, the interface trap states were passivated during the PBTI stress for the n-channel TFTs.

Figures 3a and b show the time dependence of the threshold-voltage shift (ΔV_{th}) of the p-channel/n-channel TFTs after the NBTI/PBTI stress. The constant current method was used for threshold voltage definition here; the gate voltage at a specified threshold drain current $(I_{DS}) = \pm (W/L) \times 10$ nA for $V_{DS} = \pm 0.1$ V is taken as the threshold voltage. The measurement shows that a larger stress gate voltage will lead to a more severe degradation in the threshold-voltage shift under both NBTI and PBTI stress, which indicates that bias temperature instabilities for both the n- and p-channel TFTs are electrically activated. Furthermore, the threshold-voltage shift shows a power law dependence on the stress time ($|\Delta V_{th}| \sim t^n$) that presents an exponent factor n around 0.25–0.30 for p-channel TFTs, but is slightly lower than 0.12 for n-channel TFTs. In light of previous exploration of polycrystalline silicon TFTs and single crystalline FETs, the NBTI-degradation mechanism for p-channel TFTs can be explained by diffusion-controlled electrochemical reactions that present an exponent factor between 1/3 and 1/4.[11-14] However, because the exponent factors for

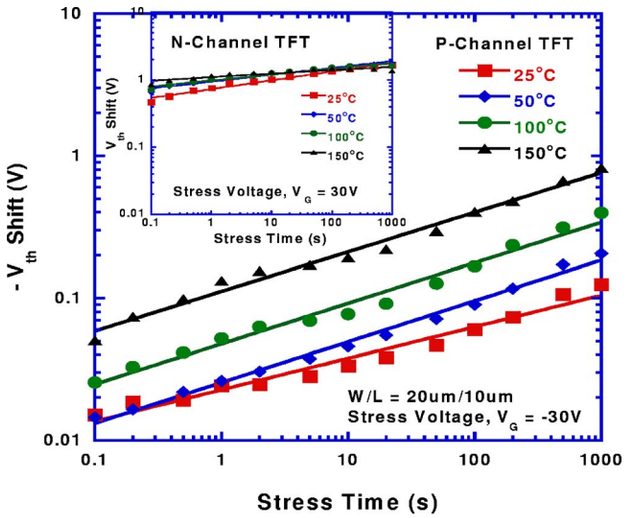
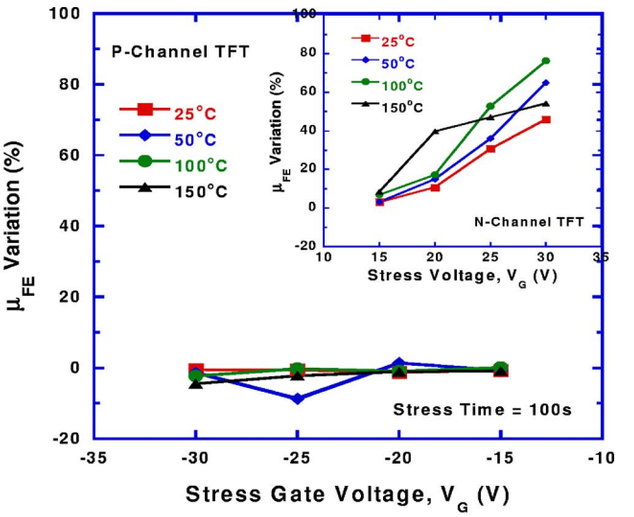
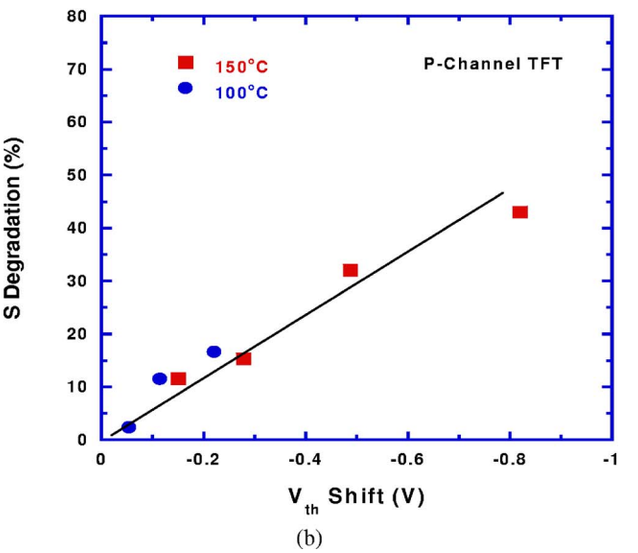


Figure 4. (Color online) Time dependence of the threshold-voltage shift of p-channel and n-channel (inset) TFTs under various stress temperatures.



(a)



(b)

Figure 5. (Color online) (a) Variation of the field-effect mobility for p-channel and n-channel (in the inset) TFTs under bias temperature stress. (b) Correlation between the subthreshold-swing degradation and the threshold-voltage shift of the p-channel TFTs after NBTI stress.

the n-channel TFTs are as low as 0.12, the PBTI-degradation mechanism will be different from that of diffusion-controlled electrochemical reactions.

To further identify the factors that induce the instability in LTPS CTFTs, the devices were measured under different temperature conditions. Figure 4 shows the time dependence of the threshold-voltage shift induced from different measurement temperatures for devices stressed with a gate voltage equal to ±30 V. We can observe from the figure that a higher ambient temperature will cause an increase in the threshold-voltage shift for p-channel TFTs under NBTI stress, but the threshold-voltage shift is nearly unchanged for the n-channel TFTs under PBTI stress. The NBTI-degradation mechanism for p-channel TFTs may be attributed to the thermally and electrically generated interface trap states and fixed-oxide charges.[3,5,10] On the other hand, the PBTI-degradation mechanism for n-channel TFTs can be explained by charge trapping in the gate dielectric; moreover, the temperature independence of the threshold-voltage shift indicates that the PBTI-degradation mechanism is dominated by electron trapping through direct tunneling into the pre-existing traps in the gate oxide.[8,9] In summary, the different mechanisms present different dependencies between the stress temperature and the threshold-voltage shift.

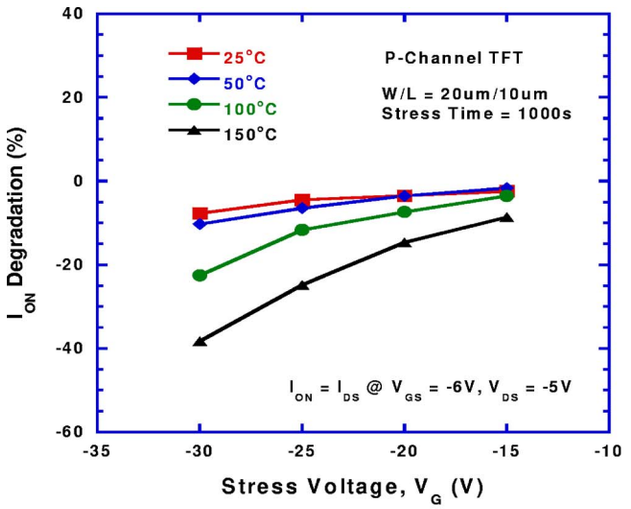
Figure 5a shows the variation in field-effect mobility for p-channel and n-channel (in the inset) TFTs under bias temperature stress. It is known that the mobility is highly associated with the trap states located near the bandedge (tail states), while the subthreshold swing is greatly related to the trap states located near the midgap (deep states).[15] For the p-channel TFTs, the poststressed field-effect mobility is unchanged, indicating that the generation of the tail states can be neglected. In contrast, the poststressed subthreshold swing is greatly degraded for the p-channel TFTs, an effect highly correlated with the threshold-voltage shift, as shown in Fig. 5b. This demonstrates that the dangling-bond formation is the main NBTI-degradation mechanism for p-channel TFTs.

By contrast, n-channel TFTs have a totally different poststressed behavior. It is interesting that the poststressed field-effect mobility is enhanced when the gate bias is increased. Details of the mechanism by which field-effect mobility is enhanced are still not well known. However, because there are many grain boundaries and trap states in the poly-Si channel, we suggest that the hydrogen atoms in the channel may be rearranged during the PBTI stress, leading to the observed enhancement of field-effect mobility.

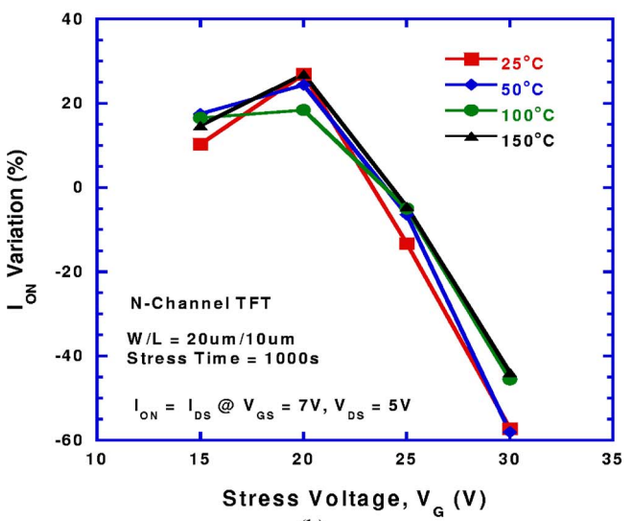
Figures 6a and b show the driving-current (I_{ON}) variation as a function of the stress voltage for the p-channel and n-channel TFTs, respectively. For the p-channel TFTs, the increase of both the stress voltage and temperature will accelerate degradation. This is because the NBTI degradation for the p-channel TFTs is electrically and thermally activated. Therefore, a higher bias voltage and temperature will certainly lead to more severe degradation in the driving current. In n-channel TFTs, the bias temperature stress causes driving-current instability, which may be divided into two regimes. In low gate bias, the driving current increases with the stress voltage. However, when the gate bias exceeds 20 V, an increment of gate bias will reduce the driving current instead. In the low stress voltage regime, the increase of the driving current is due to the enhancement of the field-effect mobility, However, under a high stress voltage regime, the effect of mobility enhancement is trivial in comparison to the threshold-voltage shift, resulting in a decrease in the driving current. The details are shown in Table I.

Conclusions

The mechanisms of bias temperature instabilities for LTPS CTFTs were investigated in this study. It was demonstrated that the



(a)



(b)

Figure 6. (Color online) Driving-current variations as a function of the stress voltage for (a) p-channel and (b) n-channel TFTs.

degradation of n- and p-channel TFTs are electrically activated; however, only the instability of p-channel TFTs is temperature accelerated. Based on our results, we concluded that the instability of p-channel TFTs can be attributed to the diffusion-controlled electrochemical reactions, while the degradation of n-channel TFTs arises from charge tunneling in the gate dielectric. Furthermore, we showed that in the subthreshold swing extraction the bias temperature stress affects p-channel TFTs through the generation of interface trap states, while mobility enhancement for the n-channel TFTs is caused by the passivation of the interface trap states. We also conclude that the bias temperature instability mechanisms of LTPS CTFTs are identified, an especially useful step for in the realization of system on panel.

Table I. Comparison of the NBTI and PBTI effects on the TFT performance.

	NBTI (p-Channel TFT)			PBTI (n-Channel TFT)		
	$\|V_{th}\|$	μ_{FE}	I_{ON}	$\|V_{th}\|$	μ_{FE}	I_{ON}
$\|Vg\| \uparrow$	$\uparrow$	=	$\downarrow$	$\uparrow$	$\uparrow$	$\uparrow\downarrow$
$T \uparrow$	$\uparrow$	=	$\downarrow$	=	$\uparrow$	=
n	0.25–0.30			0.05–0.12		

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