# A CMOS Ratio-Independent and Gain-Insensitive Algorithmic Analog-to-Digital Converter

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*Abstract*— This paper describes the design of a CMOS capacitor-ratio-independent and gain-insensitive algorithmic analog-to-digital (A/D) converter. Using the fully differential switched-capacitor technique, the A/D converter is insensitive to capacitor-ratio accuracy as well as finite gain and offset voltage of operational amplifiers. The switch-induced error voltage becomes the only major error source, which is further suppressed by the fully differential structure. The proposed A/D converter is designed and fabricated by 0.8 $\mu$m double-poly double-metal CMOS technology. The op-amp gain is only 60 dB and no special layout care is done for capacitor matching. Experimental results have shown that 14-b resolution at the sampling frequency of 10 kHz can be achieved in the fabricated A/D converter. Thus it can be used in the applications which require low-cost high-resolution A/D conversion.

## I. INTRODUCTION

AS the chip integration advances toward the VLSI/ULSI integrated systems, on-chip analog-digital interfaces are essential. One of the key technologies in analog-digital interfaces design is the low-cost and high-performance analog-digital data conversion, especially the high-resolution analog-to-digital (A/D) conversion. High-resolution A/D converters are required in many applications, such as scientific and medical instruments, process control, digital audio, and so on. To realize them, the switched-capacitor (SC) technique has been widely used because the matching accuracy of capacitors is superior to that of resistors. In these SC A/D converters, the errors caused by the offset voltage of operational amplifiers (op-amps) can be easily reduced by a factor of $1/A_v$, where $A_v$ is the finite op-amp gain. Therefore, the accuracy of the A/D converters is limited mainly by the matching accuracy of capacitors, the finite-gain effect of op-amps, and the switching noise. However, it is usually difficult to achieve both requirements of high capacitor matching accuracy and high op-amp gain in the design of high-resolution SC A/D converters.

To alleviate the above mentioned limitations, some circuit technologies have been proposed to reduce the requirement of precision components in the A/D converters. One approach is to adopt the self-calibration method [1]–[4] which uses digital methods to memorize and eliminate the capacitor's ratio errors in a binary-weighted capacitor array. Although this method can obtain a very high conversion resolution, it needs more complicated calibration cycles, control logic, and digital memories, which significantly increase chip area. The second
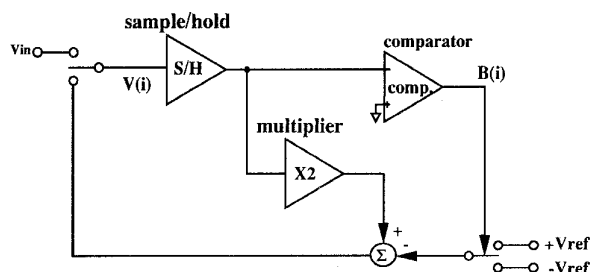
Fig. 1. The conceptual block diagram of the algorithmic A/D converter.

approach uses the ratio-independent technique [5]–[9]. In this technique, the error can be made independent of the capacitor ratios by sampling and integrating the input signal twice, and then interchanging the sampling and the integrating capacitors. This approach has the advantages of high resolution, simple circuit structure, and small die size. However, the dc gain of op-amps should be very high to obtain a high accuracy conversion. For example, 76 and 88 dB are required for 10- and 12-b resolution, respectively [6]. Generally, to increase the resolution by 1 b, it is necessary to increase the op-amp gain by 6 dB. Nevertheless, high-gain op-amps are not easy to design. Recently, some switched-capacitor circuits have been proposed to reduce the finite-gain sensitivity [10]–[13]. Those circuits use SC techniques to compensate the op-amp finite-gain error during a clock interval using the finite gain error in the previous interval. It is shown that this can effectively almost make the op-amp gain squared and reduce the phase error. Although both capacitor-ratio-independent technique and gain-sensitivity reduction technique have been proposed, they have not yet been combined together to implement high-resolution A/D converters.

In this work, an algorithm to reduce the sensitivities of both capacitor ratio and finite op-amp gain simultaneously is applied to the design of an algorithmic A/D converter [14]. Using this algorithm, the effective finite gain of the op-amps can be almost squared and the resolution of the algorithmic A/D converters can be independent of the capacitor ratio. As compared with the conventional algorithmic A/D converters where only 8-b resolution can be achieved with 60 dB op-amp gain [5], the proposed algorithmic A/D converter can obtain a 18-b resolution if the switch-induced error voltage can be eliminated. This has been proved both in theoretical analysis and SWITCAP simulation. Since the errors due to ratio mismatch, finite gain, and offset voltage can be reduced by using the proposed algorithm, the switch-induced error voltage becomes the dominant error source in the proposed
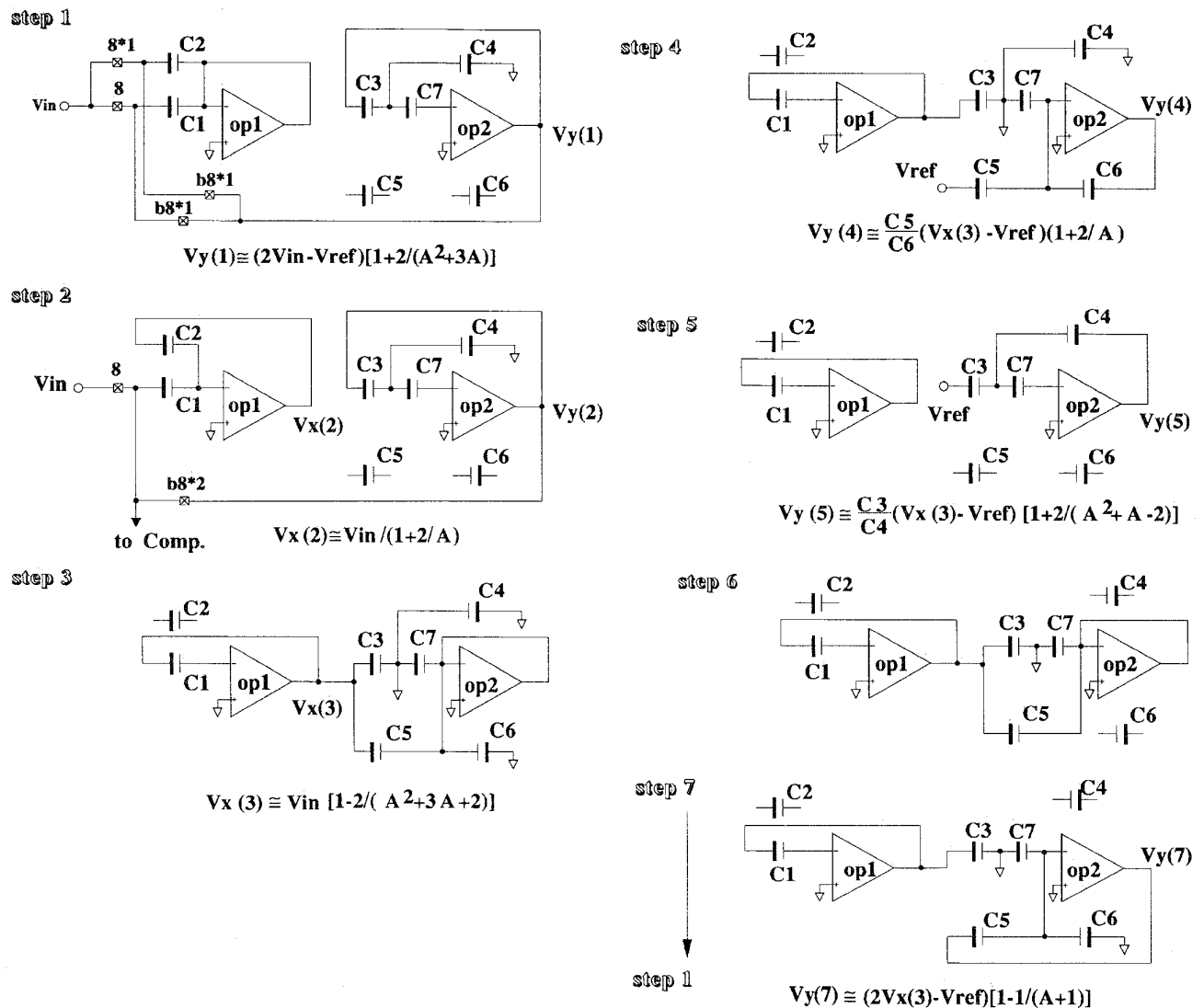
step 1

Vy(1) ≅ (2Vin-Vref)[1+2/(A²+3A)]

step 2

Vx (2)≅Vin /(1+2/ A)

to Comp.

step 3

Vx (3) ≅ Vin [1-2/( A²+3 A +2)]

step 4

$$Vy\ (4) \cong \frac{C5}{C6}(Vx(3) \text{-}Vref)(1+2/\ A\ )$$

step 5

$$Vy\ (5) \cong \frac{C3}{C4}(Vx\ (3)\text{-}\ Vref)\ [1+2/(\ A\ ^2+\ A\ \text{-}2)]$$

step 6

step 7

step 1

Vy(7) ≅ (2Vx(3)-Vref)[1-1/(A+1)]

Fig. 2.  The detailed operating steps of the proposed A/D converter.

Fig. 3.  The clock waveforms of the proposed A/D converter.

algorithmic A/D converter. Generally, CMOS switches, or dummy MOS switches, or fully differential structures can be used to minimize the switching error. In the experimental chip, the proposed A/D converter is designed by using small-size dummy MOS switches, large size capacitors, and fully differential structure to minimize the switch-induced error voltage. With the reduced switching error and 60 dB op-amp gain, the fabricated algorithmic A/D converter can achieve a 14-b resolution at the sampling frequency of 10 kHz.

Section II describes the operational principle, accuracy consideration, and circuit implementation of the proposed algorithmic A/D converter. Section III describes the experimental results. Section IV gives the conclusion.

## II. Gain- and Ratio-Insensitive A/D Converter

### A. General Principle of an Algorithmic A/D Converter

The algorithmic A/D converter, also known as the cyclic A/D converter, has been known and utilized in various forms
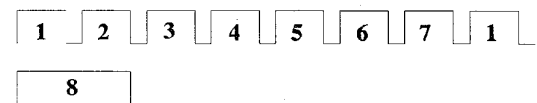
[4]–[9], [14]–[15]. A conceptual block diagram of the algorithmic A/D converter is shown in Fig. 1, which also shows the process of binary coding for the input signal from $-V_{ref}$ to $V_{ref}$, where $V_{ref}$ represents the reference voltage. It can be seen from Fig. 1 that the major circuit of the algorithmic A/D converter is an analog signal loop which contains a sample-and-hold op-amp, a multiply-by-two op-amp, a comparator, and a reference subtraction circuit.

In the implementation of the A/D converter in Fig. 1 using the technology, the major error sources are:

1) capacitor mismatches;
2) finite-gain error of op-amps;
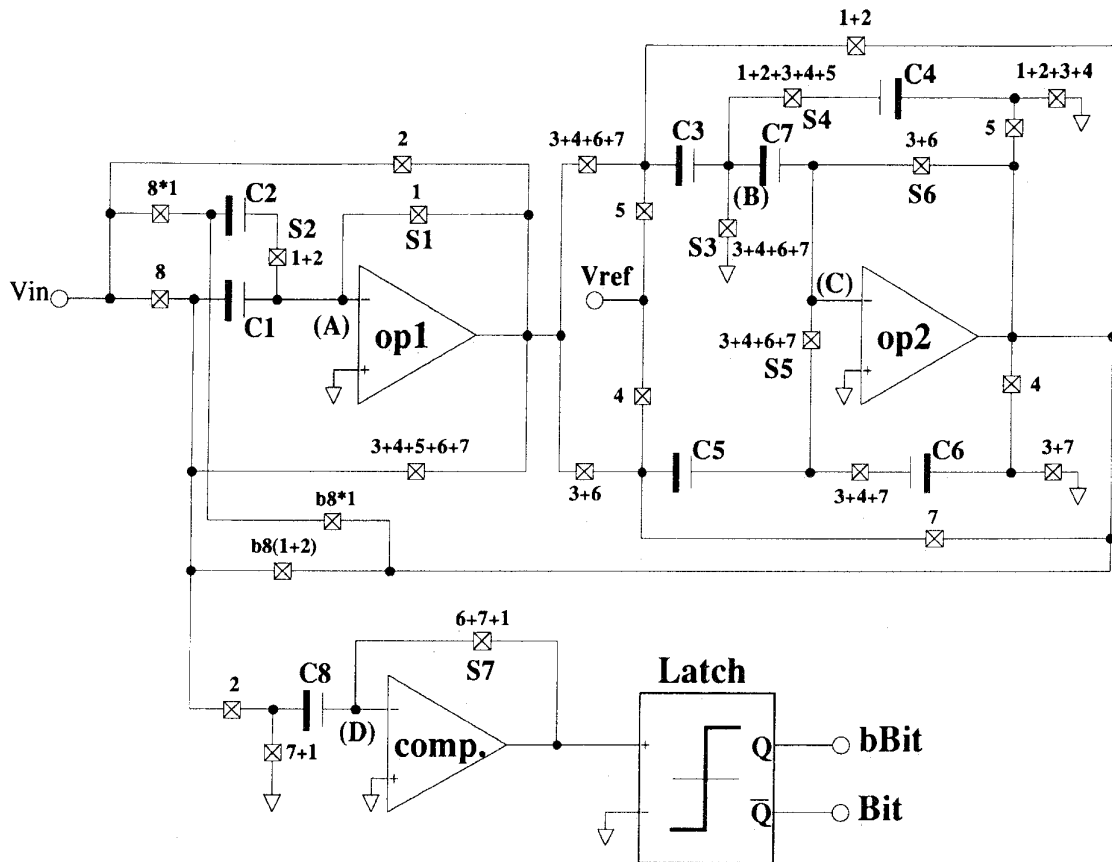3) offset voltage of op-amps;

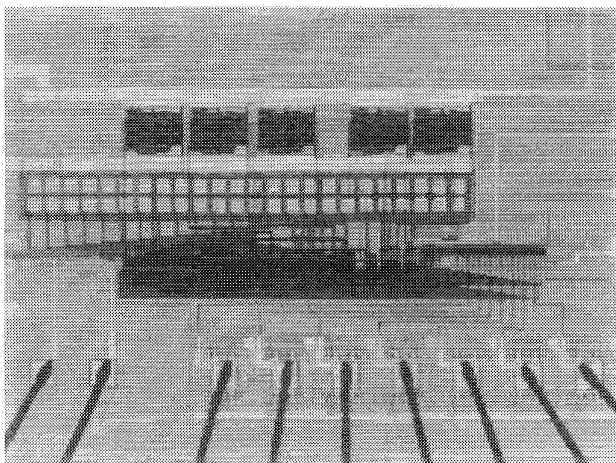Fig. 4. The complete circuit of the A/D converter.



Fig. 5. Chip photograph of the A/D converter.

4) charge injection and clock feedthrough induced by switches.

The capacitor mismatches can be solved by the ratio-independent technique [5]–[9]. The finite-gain error of op-amps can be reduced by the gain-insensitive technique [10]–[13]. The offset error can be reduced by auto-zero method [16]. Finally, the charge injection and clock feedthrough can be reduced by using dummy switches and fully differential structures.

## B. The Operation Sequence of the Proposed A/D Converter

Fig. 2 shows the step-by-step circuit structures of the proposed A/D converter. It needs seven clock steps to determine 1 b polarity. The clock waveforms are shown in Fig. 3. The clock phase eight is high only in the input sampling interval, which determines the polarity of the most significant bit (MSB). The clock phase $b8$ represents the complementary phase of the clock phase eight. The "$*$" symbol between two clock phases presents the logic "and" function whereas the "$+$" symbol presents the logic "or" function. In the step 1, the analog input $V_{in}$ is sampled on $C_1$ and $C_2$ through the switches 8 and $8 * 1$, respectively, to determine the MSB. To determine the bits other than MSB in the other cycles, the output voltage $V_y$ of the $OP_2$ in these cycles is sampled through the switches $b8 * 1$ as the input signal of the next cycle. The signal in the circuit keeps iteratively recirculating until all the desired bits are determined. In this step, $C_5$ and $C_6$ are disconnected from the $OP_2$. The bottom plates of $C_4$ and $C_3$ are shorted to ground and the output node of the $OP_2$, respectively. Also the offset error of $OP_1$ is memorized at the top plate of $C_1$ and $C_2$.

In the step 2, $V_{in}$ (for the MSB determination) or $V_y$ (for the other bits determination) is still sampled by $C_1$ but the bottom plate of $C_2$ is connected to the output node of the $OP_1$. The voltage $V_{in}$ or $V_y$ is also sent to a comparator through the switch $b8 * 2$ to determine the bit polarity. Considering charge conservation, neglecting the switch-induced error voltage and
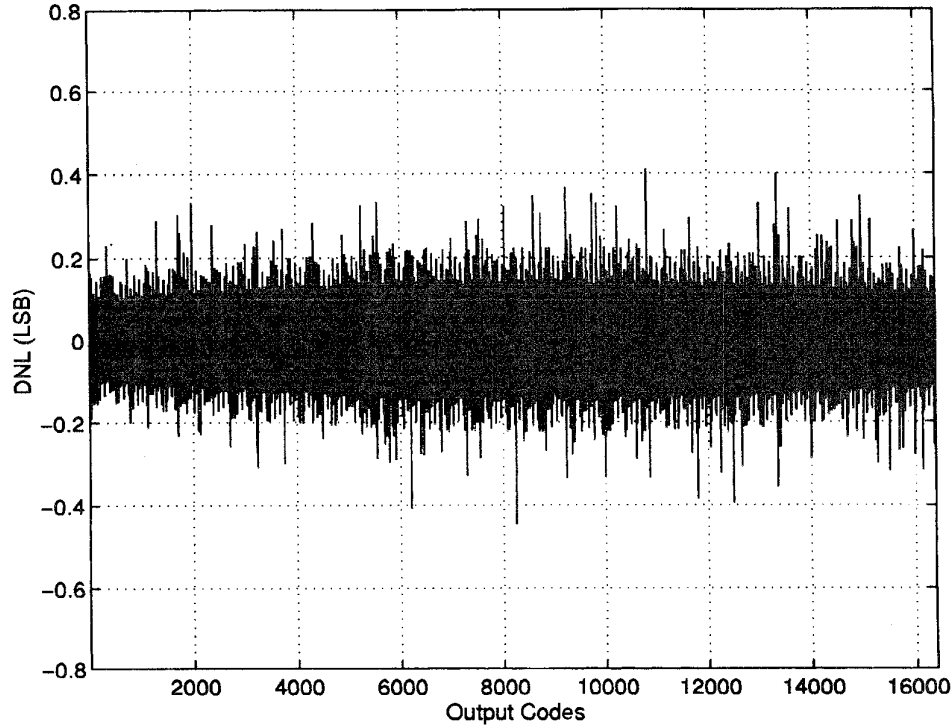
Fig. 6. A typical plot of the differential nonlinearity.

assuming $C_1 = C_2$, the output voltage of the $OP_1$ in this step can be derived as

$$V_{x(2)} \cong V_{\text{in}}/(1 + 2/A) \tag{1}$$

where $A$ is the dc gain of the op-amp. The offset error and finite gain error are now memorized at the input floating point of $OP_1$ and the top plates of $C_1$ and $C_2$.

In step 3, the bottom plate of $C_1$ is shorted to the output node of the $OP_1$ and $C_2$ is disconnected from the $OP_1$. The output voltage of the $OP_1$ is sampled to $C_3$ and $C_5$ while $C_4, C_6$, and $C_7$ are all discharged. In this case, the output voltage of the $OP_1$ can be derived as

$$V_{x(3)} \cong V_{\text{in}}[1 - 2/(A^2 + 3A + 2)]. \tag{2}$$

Equations (1) and (2) show that the sampled/held data is capacitor-ratio independent and the effective gain is almost squared.

In step 4, the bottom plates of $C_5$ and $C_6$ are shorted to $V_{\text{ref}}$ and the output node of the $OP_2$, respectively. The output voltage of the $OP_2$ can be derived as

$$V_{y(4)} \cong (C_5/C_6)(V_{x(3)} - V_{\text{ref}})/(1 + 2/A). \tag{3}$$

In step 5, the bottom plates of $C_3$ and $C_4$ are shorted to $V_{\text{ref}}$ and the output node of the $OP_2$, respectively. The capacitors $C_5$ and $C_6$ are disconnected from the $OP_2$. Assuming $(C_3/C_4) = (C_5/C_6)$, we have

$$V_{y(5)} \cong (C_3/C_4)(V_{x(3)} - V_{\text{ref}})[1 + 2/(A^2 + A - 2)]. \tag{4}$$

In step 6, both $C_4$ and $C_6$ are kept floating to memorize the previous results. The bottom plates of $C_3$ and $C_5$ are both shorted to the output node of the $OP_1$ to resample the signal

TABLE I
THE SWITCAP SIMULATION RESULTS OF THE A/D CONVERTER

| Opamp Gain (dB) | Opamp Vos (mV) | Capacitors Mismatch (%) | Error of 2Vin-Vref (V) | Effective Resoultion (bit) |
|---|---|---|---|---|
| 60 | 0 | 1 | 1.26e-6 | 18 |
| 60 | 0 | 5 | 1.45e-6 | 18 |
| 60 | 0 | 10 | 1.48e-6 | 18 |
| 60 | 10 | 1 | 1.56e-6 | 18 |
| 60 | 15 | 5 | 1.71e-6 | 18 |
| 60 | 20 | 10 | 1.84e-6 | 18 |
| 60 | 25 | 10 | 1.92e-6 | 18 |
| 80 | 10 | 1 | 1.47e-8 | 24 |
| 80 | 15 | 5 | 1.65e-8 | 24 |
| 80 | 20 | 10 | 1.78e-8 | 24 |
| 80 | 25 | 10 | 1.84e-8 | 24 |

$V_x$. In step 7, the bottom plates of $C_6$ and $C_5$ are shorted to ground and the output node of OP2, respectively. The output voltage $V_{y(7)}$ can be derived as

$$V_{y(7)} \cong (2V_{x(3)} - V_{\text{ref}})[1 - 1/(A + 1)]. \tag{5}$$

After step 7, the process step goes back to step 1 and the output voltage of the $OP_2$ is derived as

$$V_{y(1)} \cong (2V_{\text{in}} - V_{\text{ref}})[1 + 2/(A^2 + 3A)]. \tag{6}$$

Now the output voltage of the $OP_2$ is sampled by $C_1$ and $C_2$, instead of the analog input $V_{\text{in}}$, to determine the bits other than the MSB. From (6), it can be seen that the procedure of multiplication-by-two and subtraction is ratio-independent, less gain-sensitive, and offset free. The above sequence is repeated until all the desired number of bits have been obtained.
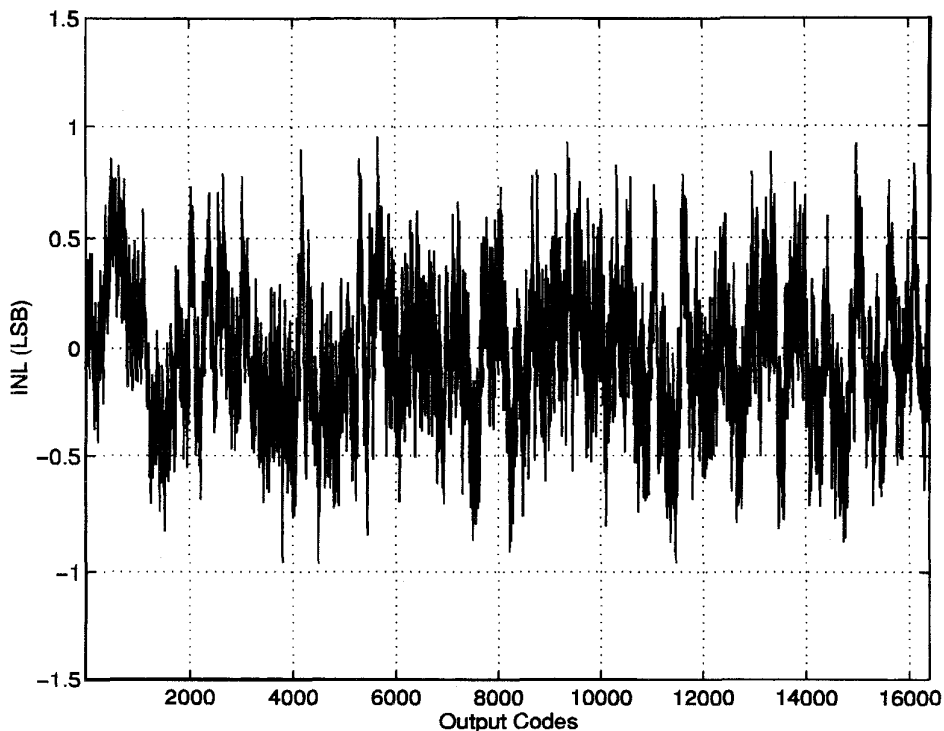
Fig. 7.  A typical plot of the integral nonlinearity.

The complete circuits of the proposed algorithmic A/D converter are shown in Fig. 4. The A/D converter contains two op-amps, one comparator, one latch, seven capacitors, and some switches.

The SWITCAP simulation results of the proposed A/D converter are given in Table I. The effective resolution can be as high as 18 b with the nonlinearity within $\pm 1/2$ LSB when the finite gain of op-amp is 60 dB, the offset voltage is 5 to 25 mV, and the capacitor mismatch is varied from 1% to 10%. This verifies the analysis of capacitor-ratio independence and low gain sensitivity in the proposed A/D converter.

### C. Accuracy Consideration

In this design, since the capacitor ratio mismatch does not cause any error effect, we focus the error analysis on the error sources of op-amps. To keep the maximum absolute error below 1/2 LSB, the maximum allowable gain error of op-amps can be derived from (6) as

$$E_{gain} \cong [2/(A^2 + 3A)] <= 1/2^{n+1}. \tag{7}$$

Equation (7) gives a limitation on the minimum dc gain of op-amps. From (7), it is found that to obtain 10-, 14-, and 18-b conversion, the op-amp dc gain should be greater than 36, 48, and 60 dB, respectively. In the conventional ratio-independent A/D converters [5], [6], 6-dB gain increase is required to increase 1-b accuracy, whereas only 3-dB gain increase is required in this design.

Similarly, the effective offset error caused by op-amps is reduced by a factor of $2/(A^2 + 3A)$ in this design. Since the

TABLE II
THE EXPERIMENTAL RESULTS OF THE PROPOSED A/D CONVERTER

| | |
|---|---|
| Resolution | 14 bits |
| Differential nonlinearity | < ±1/2 LSB |
| Integral nonlinearity | < ± 1 LSB |
| Sampling frequency | 10 KHz |
| Gain of op amp | 60dB |
| Power dissipation | 50 mWatts |
| Supply voltage | ± 2.5 V |
| Process | 0.8um CMOS |
| Chip active area | 2.1mm × 0.8mm |

offset voltage of an op-amp is in the order of 10 mV, the offset error is very small and can be neglected.

### D. Circuit Implementation

Though the operation sequence in the above description uses the single-ended structure for easy understanding, the chip implementation uses fully differential structure for common-mode noise elimination and switching noise reduction. The op-amp uses a fully differential folded-cascode structure [17] with an open-loop gain of 60 dB.

In this design, the fully differential structure is used to minimize the switch-induced error voltage. Small-size dummy-MOS switches (2 $\mu$m/1 $\mu$m) and large-size capacitors (10 pF) are also used to further reduce the switching noise. Because standard techniques have been used to reduce signal-dependent charge injection [5], the resulting error voltage is constant and signal independent. Thus, it can be treated as the offset noise and corrected by digital calibration to further improve the resolution.
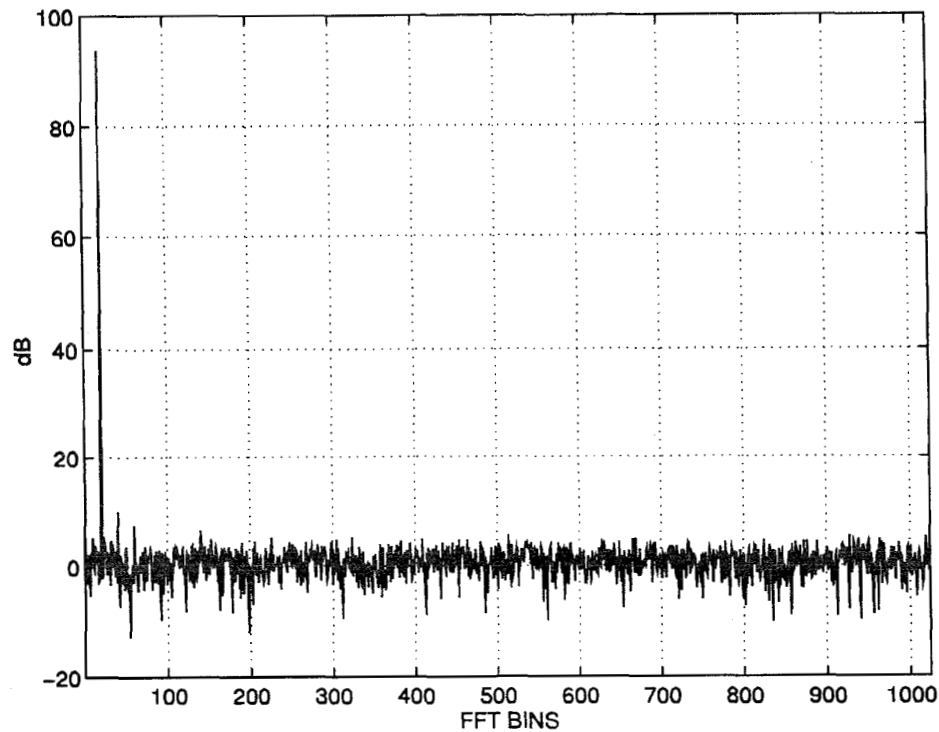
Fig. 8. A typical FFT plot of the A/D converter.

TABLE III
COMPARISON OF THE PROPOSED A/D CONVERTER WITH THE
PREVIOUS RATIO-INDEPENDENT A/D CONVERTERS [5], [6]

| A/D converters / Performance | [5] | [6] | This work |
|---|---|---|---|
| Resolution (bits) | 12 | 8 | 14 |
| Absolute INL (LSB) | <=1.5 | <=0.5 | <=1 |
| Op amp dc Gain (dB) | 92 | 84 | 60 |
| Clock cycles for n bits | 6n | 3n | 7n |
| Sampling rate (KHz) | 8 | 8 | 10 |
| Power (mW) dissipation | 17 | – | 50 |
| CMOS Technology | 5um | 2um | 0.8um |

III. EXPERIMENTAL RESULTS

The experimental chip of the proposed algorithmic A/D converter was designed and fabricated by using 0.8 $\mu$m $n$-well double-poly double-metal CMOS process. The chip photograph of the fabricated A/D converter is shown in Fig. 5. The active chip area is about 2.1 mm $*$ 0.8 mm. Experimental results have shown that at the sampling rate of 10 ksample/s, the prototype chips can achieve 14-b resolution. A typical plot of the measured differential nonlinearity versus the digital output codes and that of the measured integral nonlinearity are shown in Figs. 6 and 7, respectively. It can be seen that

the differential nonlinearity is within $\pm 0.5$ LSB, whereas the integral nonlinearity is within $\pm 1$ LSB at the sampling rate of 10 ksample/s.

A typical FFT plot of the fabricated A/D converter with a full-scale 0.1 kHz sinewave sampled at 10 kHz is shown in Fig. 8. The overall signal-to-noise-and-distortion ratio (SNDR) is 82 dB. From Fig. 8, it can be seen that the SNDR is dominated by the second harmonic distortion. The power consumption of this chip is about 50 mW. The major experimental results of the A/D converter are summarized in Table II.

The comparison of the proposed A/D converter with the previous reported ratio-independent A/D converters [5], [6] is listed in Table III. It can be seen from Table III that the proposed A/D converter can achieve a higher resolution with lower dc gains of op-amps as compared with the other two A/D converters [5], [6]. However, the proposed A/D converter needs extra one clock cycle per bit as compared with the A/D converter in [5].

IV. CONCLUSION

A circuit configuration for an algorithmic A/D converter has been described. It does not require ratio-matched components and is insensitive to finite dc gain and offset of op-amps. An experimental prototype chip has been designed and fabricated. The dc gain of op-amps is 60 dB and no special layout matching method is required for on-chip linear capacitors. The measurement results have shown that differential nonlinearity and integral nonlinearity of the fabricated A/D converter is within $\pm 0.5$ LSB and $\pm 1$ LSB, respectively. The conversion rate is 10 kHz and the power consumption is 50 mW. To

further improve the accuracy of the A/D converter, the switch-induced error voltage should be reduced. This will be done in the future.

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