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Periodically Lateral Silicon Grains Fabricated by Excimer Laser Irradiation with a-Si Spacers for LTPS TFTs

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Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) with a periodic lateral silicon grain structure have been demonstrated to exhibit high-performance electrical characteristics via the amorphous silicon spacers above the amorphous silicon film crystallized with excimer laser. Amorphous silicon spacers allowed the bottom of the under-layered amorphous silicon film to serve as seed crystals. The periodic grain structure could be artificially controlled via the super lateral growth phenomenon during excimer laser irradiation. Consequently, such periodically large and lateral grains in the TFTs would achieve high field-effect-mobility of 298 cm^2/V s, as compared with the conventional ones of 128 cm^2/V s. In addition, the uniformity of device-to-device could be improved due to this location-manipulated lateral silicon grains.
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Low-temperature polycrystalline silicon (LTPS) thin-film transistors fabricated by excimer laser crystallization (ELC) have been extensively studied for active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs) owing to their high driving-current capability.[1,2] Although field-effect-mobility of 200 cm^2/V s for TFTs has been attained by ELC, it is difficult to make the laser energy density hit the super lateral growth regime everywhere due to the fluctuation of pulse-to-pulse energy and amorphous silicon (a-Si) layer thickness.[3-5] Furthermore, in the applications of system-on-panel (SOP), high-performance LTPS TFTs are still needed to integrate memory and controller with driver circuits on a single substrate. Thus, there is a great interest in improving the performance of LTPS TFTs by laser crystallization approaches, including sequential lateral solidification by laser beam scanning within several micrometers step by step,[6-9] phase-modulated ELC using an optical phase-shift mask,[10-12] μ-Czochralski (grain filters) method,[13-15] ELC of selectively floating a-Si layer,[16,17] CLC method using the diode-pumped solid state continuous wave laser,[18,19] and selectively enlarging laser crystallization (SELAX).[20] However, most of them are complicated or not easy to control from the viewpoints of LTPS TFTs fabrication.

In this work, a novel crystallization process for producing high-mobility poly-Si TFTs is proposed. Periodically lateral silicon grains with 2 μm in length can be artificially grown in the channel regions via the amorphous silicon spacer structure with excimer laser irradiation. It leads to the enhancement of device performance and the improvement of device uniformity. The effect of the number of grain boundary on large dimension TFTs is also investigated.

Experimental

The maximum process temperature of n-channel LTPS TFTs fabrication is 550°C for the deposition of a-Si thin films with low-pressure chemical vapor deposition (LPCVD). Figure 1 illustrates the key processes for the fabrication of LTPS TFTs crystallized with a-Si spacer structure. At first, a 1000 Å thick amorphous silicon (a-Si) layer was deposited by pyrolysis of pure silane (SiH_4) by LPCVD at 550°C on oxidized silicon wafer with oxide thickness of 1 μm. Then, a 500 Å thick tetraethyl orthosilicate (TEOS) oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385°C. Next, the TEOS oxide layer in some regions was removed to form individual islands following by another 1000 Å thick a-Si layer deposition by LPCVD at 550°C. Subsequently, the upper a-Si layer was etched by transformer-coupled plasma reactive ion etching (TCP-RIE) to leave the a-Si spacer on the initial a-Si thin film. After stripping-off the remains of TEOS oxide by buffer oxide etchant (BOE), excimer laser crystallization (ELC) was performed by KrF excimer laser (λ = 248 nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-3} Torr and substrate was maintained at 400°C. The number of laser shots per area was 20 (i.e., 95% overlapping) and laser energy density was varied. After defining the device active region, a 1000 Å thick TEOS gate oxide was deposited by PECVD at 385°C. Then, a 2000 Å thick a-Si thin film was then deposited by LPCVD at 550°C for gate electrode. The a-Si thin film and gate oxide were etched by TCP-RIE to form the gate electrode. A self-aligned phosphorous ion implantation with dose of 5×10^{15} cm^{-2} was carried out to form source and drain regions. Next, a 3000 Å thick TEOS passivation oxide was deposited and the implanted dopants were activated by thermal annealing at 600°C for 12 h. Finally, contact holes opening and metallization were carried out to complete the fabrication of TFTs with spacer structure. No hydrogenation plasma treatment was performed during the device fabrication process. For the sake of comparison, the conventional excimer-laser-crystallized LTPS TFTs with a channel thickness of 1000 Å were also fabricated.

Results and Discussion

Atomic force microscopy (AFM) analysis is used to investigate the surface morphology of silicon thin film before and after laser crystallization. Figure 2a and b display the AFM images of silicon thin film with 1500 Å thick spacer height before and after excimer laser irradiation, respectively. Three apparent silicon spacer lines are indicated by white dashed lines formed using dry-etching of the a-Si/TEOS-SiO_2 step structure following the TEOS stripping-off before laser irradiation in Fig. 2a. After laser crystallization, the spacers disappear and the silicon thin film becomes smooth due to the effect of surface tension during excimer laser irradiation. The location of a-Si spacers has been verified by protecting some spacers from excimer laser crystallization. The ridge and hillock configurational occurs at the grain boundaries due to the freezing of capillary waves excited in the melting silicon during laser crystallization.[21] Figure 3 shows the Raman spectra from poly-Si film with periodic lateral grains, from the conventional excimer-laser-crystallized poly-Si film, and from a silicon wafer for reference. The insets describe that full width at half-maximum (fwhm) and normalized peak intensity of the poly-Si film with periodic lateral silicon grains (PLSG) are close to those of silicon wafer, reflecting the fact that the crystallinity of PLSG poly-Si film is better than that of conventional ELC poly-Si film.

Figure 4a and b show the SEMs of excimer laser crystallized poly-Si with a-Si spacer structure after Secco etching and the dis-

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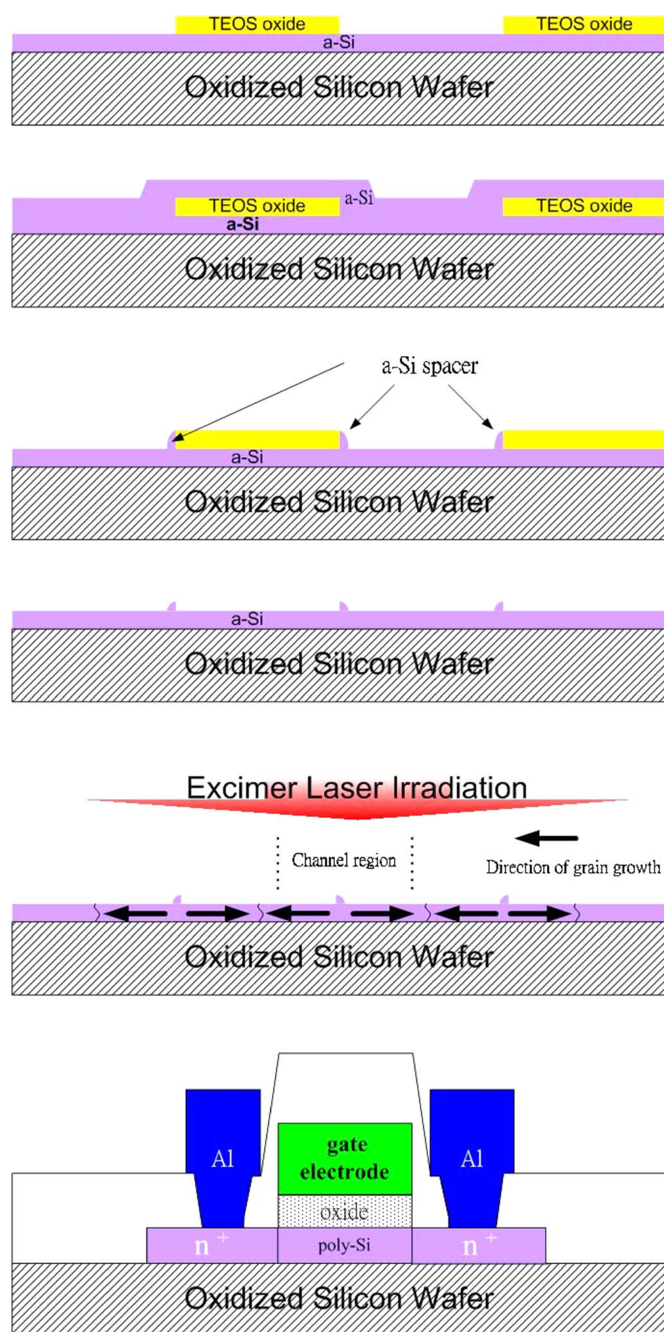

Figure 1. (Color online) The key processes for fabricating small-dimension LTPS TFTs with a-Si spacer structure.

tances between adjacent a-Si spacers are 2 and 3 μm, respectively. The inset in Fig. 4a shows the microstructure of conventional ELC poly-Si with the same scale. The location of a-Si spacer is indicated by white dash lines. It can be observed that Fig. 4a shows the transverse grains with 2 μm in length formed periodically in the laser crystallized poly-Si thin film, while small and fine grains which are present in Fig. 4b, are caused by spontaneous homogeneous nucleation. It has been reported that lateral thermal gradient could arise as a result of the heat generated at moving solid-melting interfaces.[5,22] As a proper laser energy density is performed on the amorphous silicon thin film containing different thickness, the thin silicon region is completely melted while the thick region is partially melted, and the lateral grain growth starts from the unmelted solid Si toward the completely melted thin region. In this experiment, as excimer laser irradiation is performed on the amorphous silicon thin film with a-Si spacers, the laser energy densities can cause complete melting 1000 Å thick silicon thin film but partial melting 1500 Å thick a-Si film. Therefore, the 1000 Å thick poly-Si film with the 500 Å thick spacer will proceed the lateral grain growth starting from the unmelted silicon solid seed under the spacer, and extend toward the completely melted region until the solid-melt interface from opposite direction impinges. If the a-Si seeds were arranged in a proper distance, periodic grain growth will be manufactured without any spontaneous nucleation. Thus, the grain boundaries in the channel region can be controlled and reduced. From the SEM analyses, the maximum achievable length of lateral grain growth in this crystallization method is ~2.5 μm. Because the number of spontaneous small grain and grain boundary is reduced, the uniformity of TFTs performance can be improved with artificially periodic lateral grains.

Typical transfer characteristics and output characteristics of LTPS TFTs with periodic lateral silicon grains and conventional ones for $W = L = 2$ μm are shown in Fig. 5a and b, respectively. Several important electrical characteristics of the TFTs are listed in Table I. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_{ds} = (W/L) \times 10^{-8}$ A at $V_{ds} = 0.1$ V. The field-effect-mobility and subthreshold swing were extracted at $V_{ds} = 0.1$ V, and the I_{on}/I_{off} current ratio was defined at $V_{ds} = 5$ V. Owing to the uniformly large transverse grains grown in the device channel region, TFTs with periodic lateral grains exhibit better electrical characteristics than the conventional ones. Poly-Si TFT with field-effect-mobility of 298 cm^2/V s can be achieved using this a-Si spacer crystallization method while the mobility of the conventional counterpart is ~128 cm^2/V s. It is generally believed that the grain boundary acts as a strong trapping center which degrades the performance of TFTs resulting from grain boundary potential barrier height. The high field-effect-mobility is attributed to that the carrier transport is not interrupted by the grain boundary parallel to the channel direction for the periodic lateral grain silicon structure. Although small and fine grains are located in the channel region as the distance between neighboring a-Si spacers exceeds 2.5 μm, the characteristics of TFTs crystallized with a-Si spacer structure are still better than those of conventional TFTs.

In addition to the improvement of LTPS TFTs performance, TFTs with periodic lateral grains demonstrate better uniformity due to the wide laser process window. Figures 6a and b show the dependences of field effect mobility and threshold voltage on laser energy densities for LTPS TFTs crystallized with two different structures whose channel length is 2 μm. In Fig. 6a and b, twenty TFTs for each laser irradiation condition are measured to study the device-to-device variation. The vertical bars in the figures indicate the maximum and minimum characteristic values and the solid symbols are the average calculated characteristic values at the specific laser energy density. Unlike the conventional devices, it is found that the threshold voltage and field-effect-mobility of LTPS TFTs with periodic lateral grains are much less sensitive for different laser energy densities.

Because periodic lateral silicon grains can be arranged periodically inside the channel region (Fig. 4a), this proposed crystallization method is also suitable for large dimension TFTs. Figure 7 displays the schematic illustration of the positions of a-Si spacer in the channel region for large-sized device. Periodic lateral grains are constructed inside the channel and the number of longitudinal grain boundaries can be varied by adjusting the distance of adjacent a-Si spacers. Figure 8a and b show the typical transfer characteristics and output characteristics of LTPS TFT crystallized with periodic lateral silicon grains, in which the distance between neighboring a-Si spacers is 2.5 μm, and conventional one for $W = L = 10$ μm, respectively. Table II summarizes several important electrical characteristics of the TFTs crystallized with conventional and a-Si spacer structures, in which the distances between adjacent spacers are 1, 2, 2.5, 3, and 4 μm, respectively. The device channel width and length are equal 10 μm. Periodic lateral grains in the channel region make

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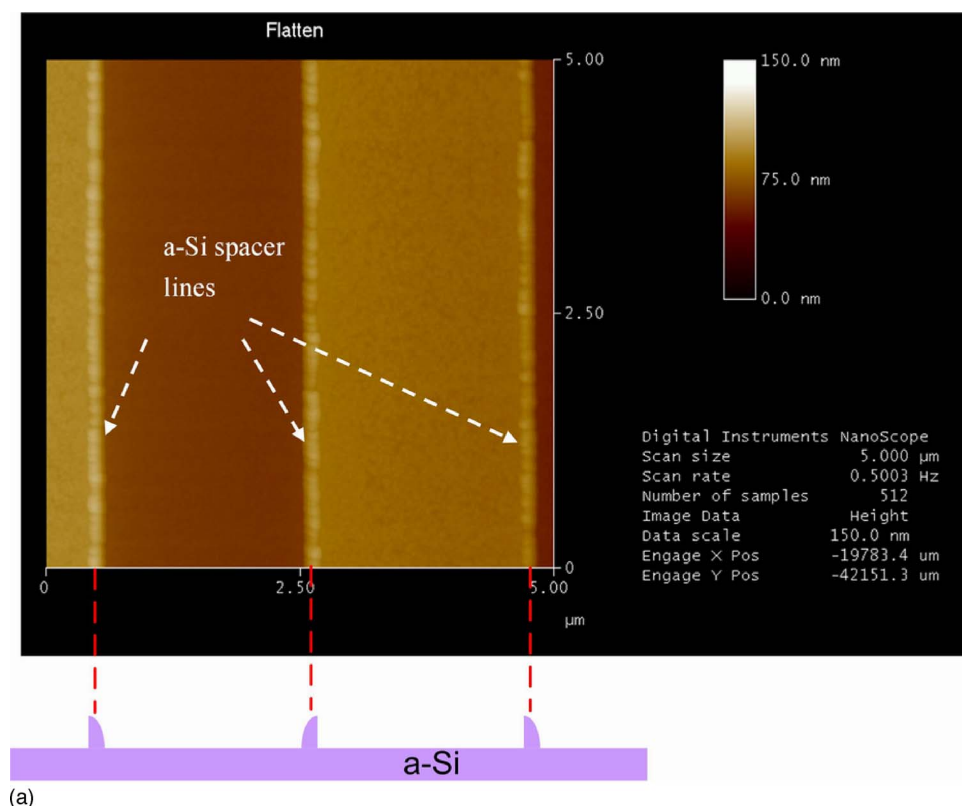

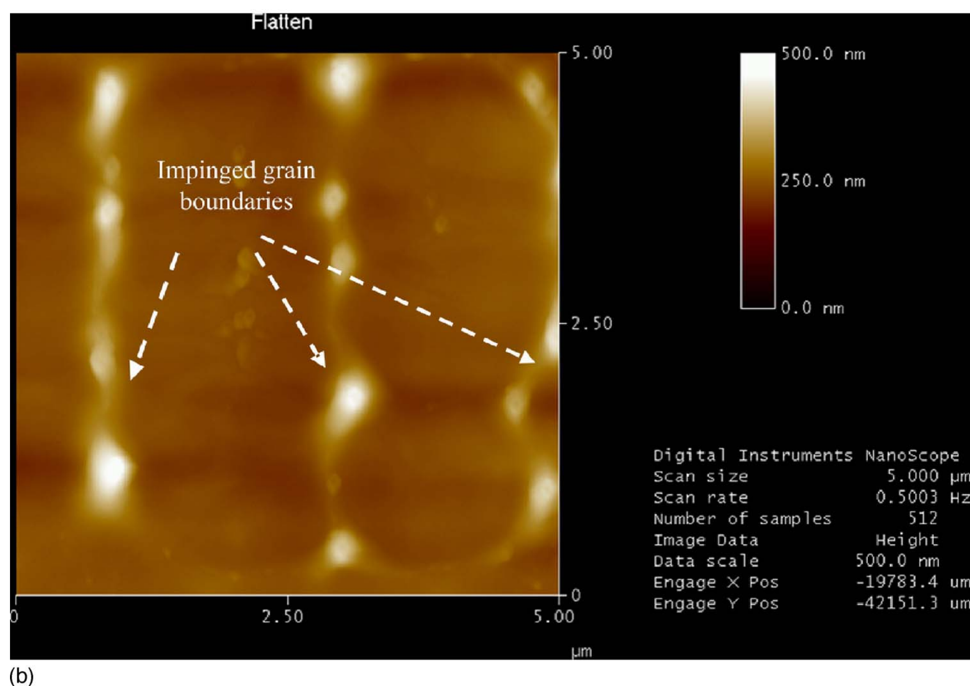

Figure 2. (Color online) AFMs of poly-Si thin film with spacers of 1500 Å height, (a) before and (b) after laser irradiation.

the performance of poly-Si TFTs better than that of conventional TFTs. Besides the enhancement of field-effect-mobility, high on/off current ratio, and low threshold voltage are also demonstrated in these devices. These electrical characteristics are gradually improved due to the decrease of the number of longitudinal grain boundaries in the channel region as the distance between adjacent a-Si spacer increases. The optimal electrical characteristics are obtained when the distance between neighboring a-Si spacers is 2.5 μm. This result is consistent with the SEM analyses, which reveal that the largest lateral grain crystallized made by this technique is $\sim$2.5 μm.

Conclusions

A new crystallization technology for producing periodic lateral silicon gains has been developed by excimer laser irradiation with a-Si spacers. In addition to the high-performance n-channel LTPS

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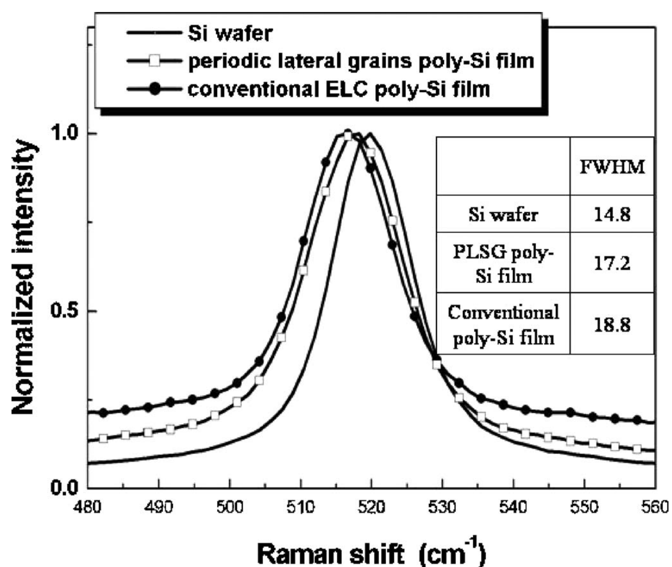
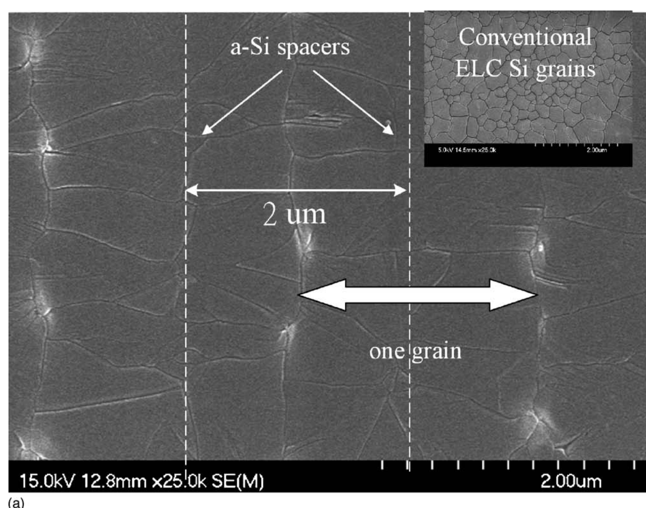


Figure 3. Raman spectra for poly-Si film with periodic lateral grains and those for conventional ELC poly-Si film.



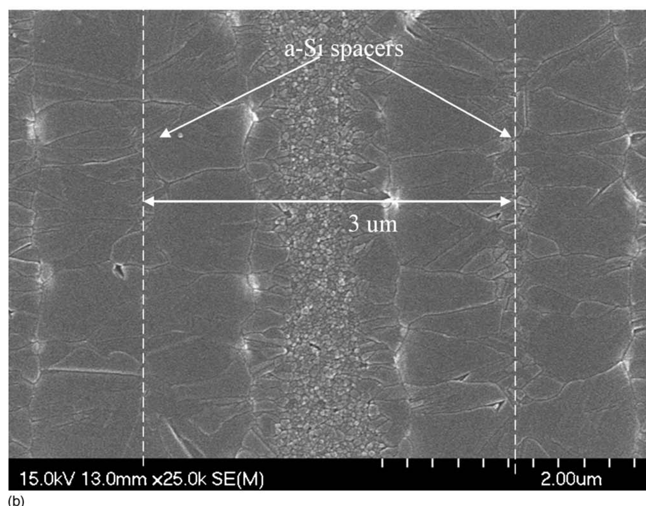
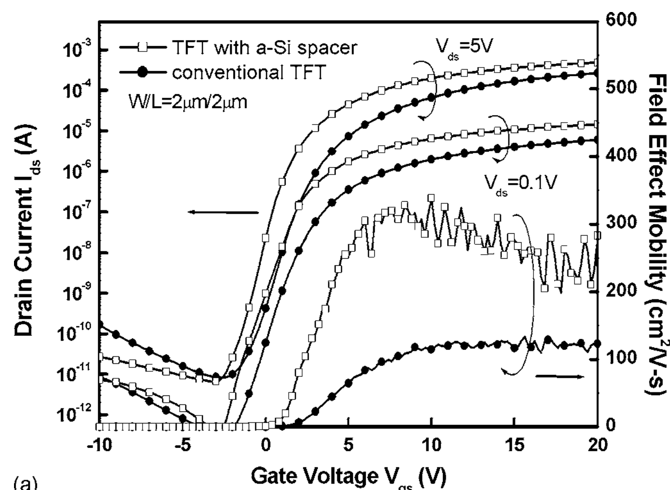


Figure 4. SEMs of excimer laser crystallized poly-Si film with amorphous Si spacer structure after Secco etch and the distances between adjacent a-Si spacers are (a) 2 and (b) 3 μm, respectively. Inset in (a) is a conventional ELC poly-Si film.



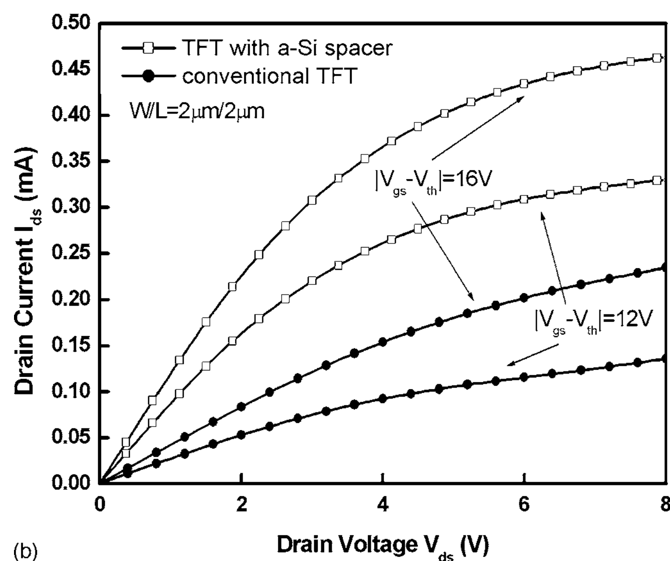


Figure 5. *I-V* curves of LTPS TFT with a-Si spacer and conventional structure. (a) Transfer characteristics. (b) Output characteristics.

TFTs with field-effect-mobility reaching 298 cm^2/V s in 2 μm design rule, excellent uniformity of device performance was also demonstrated owing to the artificially controlled periodic lateral grain growth. Large-dimension TFTs crystallized with the distance between adjacent a-Si spacers of 2.5 μm also exhibited the better characteristics resulting from the minimum number of longitudinal grain

Table I. Measured electrical characteristics of LTPS TFTs crystallized with a-Si spacer and conventional structures.

Structure	Threshold voltage (V)	Field-effect-mobility (cm^2/V s)	Subthreshold swing (mV/dec)	On/off current ratio (10^7)
Conventional ($W = L = 1.5$ μm)	−0.652	155	1072	0.17
a-Si spacer ($W = L = 1.5$ μm)	0.46	312	310	8.2
Conventional ($W = L = 2$ μm)	1.94	128	738	3.3
a-Si spacer ($W = L = 2$ μm)	0.86	298	477	6.3

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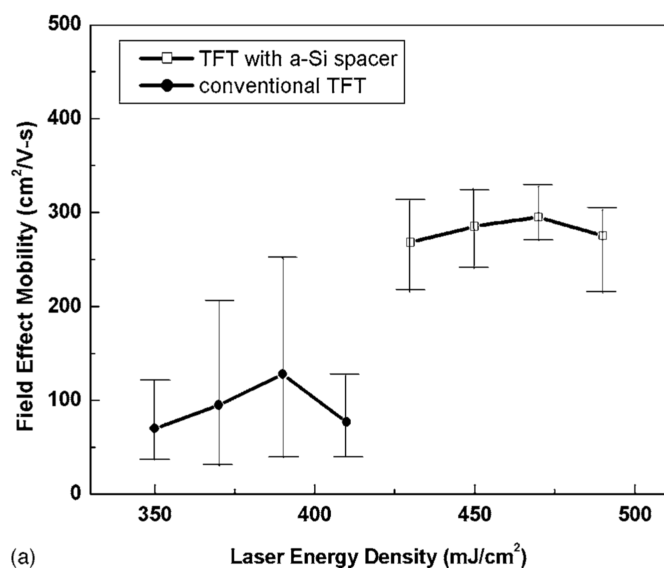


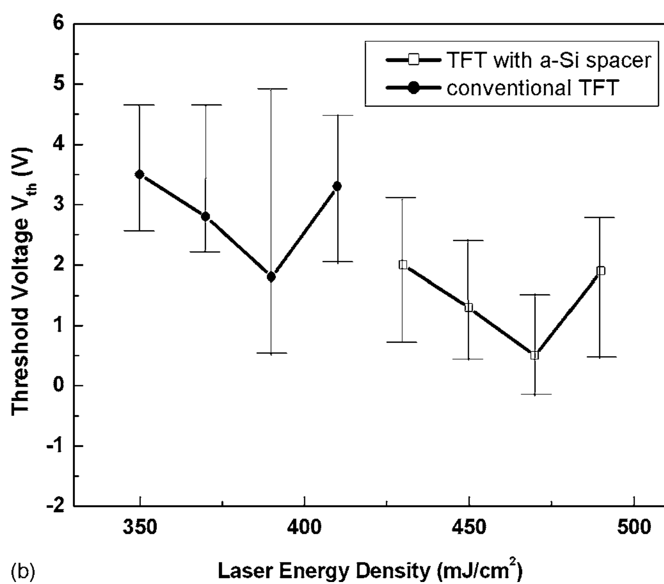


Figure 6. Dependences of (a) field-effect-mobility and (b) threshold voltage on applied laser energy density for TFTs with a-Si spacer and conventional TFTs.

Table II. Measured optimal electrical characteristics of LTPS TFTs crystallized with conventional and a-Si spacer structures, respectively.

Structure (W/L = 10/10 μm)	Threshold voltage (V)	Field-effect-mobility (cm^2/V s)	Subthreshold swing (V/dec)	On/off current ratio (10^7)
Conventional	6.16	114	1.61	0.93
Spacer distance =1 μm	5.88	141	1.68	2.5
Spacer distance =2 μm	4.88	170	1.27	7.7
Spacer distance =2.5 μm	5.35	176	1.13	8.9
Spacer distance =3 μm	6.40	176	1.81	6.8
Spacer distance =4 μm	5.99	168	1.73	14

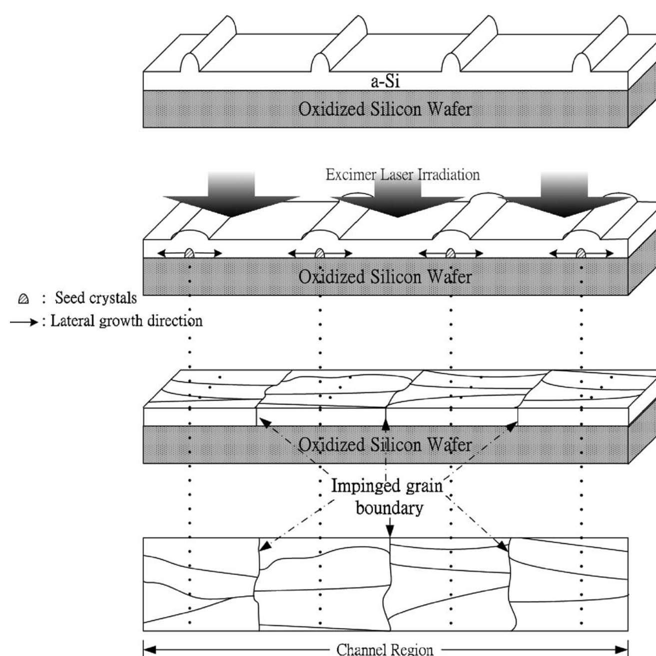
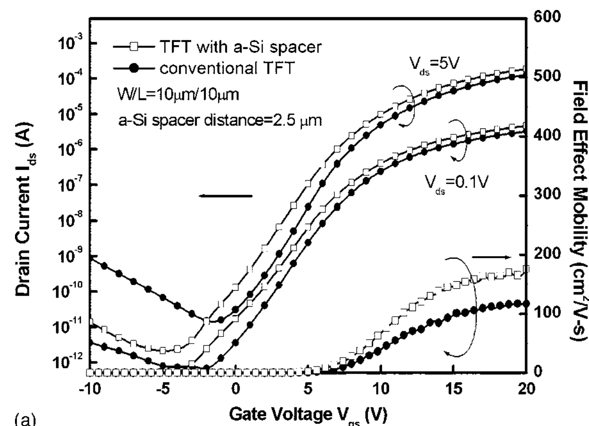


Figure 7. Schematic of poly-Si film with periodic lateral grains applied to large-dimension TFTs.



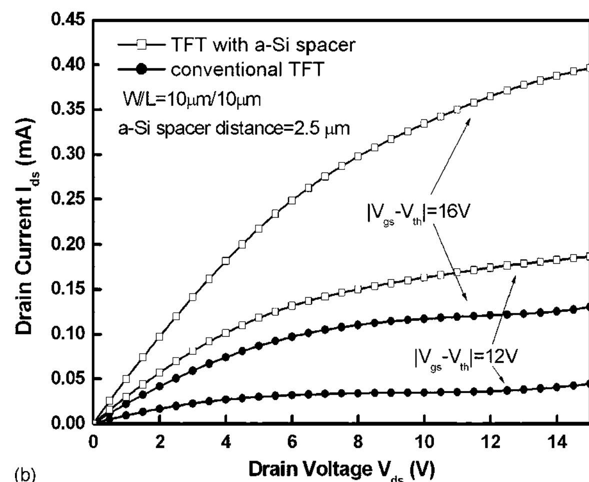


Figure 8. (a) Typical transfer characteristics and (b) output characteristics of LTPS TFT crystallized with periodic lateral silicon grains, in which the distance between neighboring a-Si spacers is 2.5 μm, and conventional one for $W = L = 10$ μm.

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boundary in the channel region. LTPS TFTs with periodic lateral silicon grains were therefore promising for future system-on-panel applications.

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