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Improvement of Negative-Bias-Temperature Instability in SiN-Capped p-Channel Metal-Oxide-Semiconductor Field-Effect Transistors Using Ultrathin HfO_2 Buffer Layer

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Characteristics of p-channel SiN-capped metal-oxide-semiconductor field-effect transistors (PMOSFETs) with a thin HfO_2 buffer layer were investigated. The compressive strain in the channel was deliberately induced in this study by a SiN capping layer over the gate using plasma-enhanced chemical vapor deposition (PECVD). Although a compressive SiN capping effectively boosts the drive current of PMOSFET devices, its presence also worsens the negative bias temperature instability (NBTI) characteristics due to the high hydrogen content in the SiN layer, which could diffuse into the channel region during the deposition process. To address this issue, the insertion of a 3 nm thick HfO_2 buffer layer between the gate and SiN capping is proposed and demonstrated to improve NBTI reliability without sacrificing the device performance enhancement.
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Negative bias temperature instability (NBTI) is known to be a critical reliability concern and represents one of the major bottlenecks for product lifetime in nanoscale p-channel metal-oxide-semiconductor field-effect transistors (PMOSFETs).[1-7] Usually the creation of interface traps and positive fixed charges by the dissociation of Si–H bonds at the SiO_2/Si interface could cause a large threshold voltage shift, thus diminishing the current drive and transconductance of the device, and may eventually lead to circuit malfunction.

Using process techniques to induce uniaxial strain in the channel for enhancing carrier mobility and thus drive current has recently received a lot of attention.[8-16] Several approaches have been reported to induce compressive channel strain beneficial for improving the hole mobility, including embedded SiGe in the source/drain (S/D) region[10,11] and the SiN contact etch-stop layer (CESL).[12-14] The latter approach is typically carried out by depositing the SiN layer using plasma-enhanced chemical vapor deposition (PECVD). In contrast to the complex and costly SiGe refill scheme, the simplicity and maturity of the PECVD SiN (PE-SiN) process seem much more attractive and practical. Although strain channel could boost device performance, the strain energy stored in the channel and a high amount of hydrogen species contained in the PE-SiN layer could potentially worsen the NBTI reliability.[15,16] To address this issue, this paper presents a different approach by inserting a thin buffer layer prior to SiN capping for suppressing hydrogen diffusion into the channel.

Device Fabrication

The PMOSFETs in this study were fabricated on 6 in. n-type Si wafers with conventional local oxidation of silicon (LOCOS) isolation. Gate oxide with a thickness of 3 nm was grown in a vertical furnace in O_2 at 800°C. After gate oxide growth, a 200 nm thick polycrystalline silicon (poly-Si) was deposited by low-pressure chemical vapor deposition (LPCVD), followed by standard plasma gate etch to form the patterned gate. Afterward, standard procedures were applied to form tetraethoxysilane (TEOS) spacer and S/D junctions. Subsequently, a rapid thermal annealing at 900°C for 30 s was performed to activate dopants in the gate and S/D regions. A 300 nm thick PE-SiN was then deposited onto the device surface, followed by the deposition of TEOS passivation by PECVD. For some SiN-capped samples, a 3 nm thick HfO_2 buffer layer deposited by metallorganic chemical vapor deposition (MOCVD) was capped prior to SiN deposition (denoted as HfO_2-buffered split). The thickness measured from cross-sectional transmission electron microscope (TEM) pictures for SiN and HfO_2 layer is ~310 and 3 nm, respectively, as shown in Fig. 1a and b. Contact holes and metallization processes were subsequently performed. Finally, the processing steps were completed with a forming gas anneal at 400°C. Electrical characteristics were measured using an Agilent 4156 system. NBTI stress measurements were performed using a temperature-regulated hot chuck at 125°C. Interface traps were evaluated using charge pumping method with fixed amplitude of 1.5 V at 1 MHz.

Devices Characteristics

The stress of PE-SiN layer with and without an HfO_2 buffer layer (3 nm) was first examined by probing blanket monitor samples deposited on Si wafers. We confirmed that the stress was compressive in nature with a magnitude of around −700 MPa for all samples, irrespective of the HfO_2 presence. This indicates that the insertion of such ultrathin buffer layer will not relax the strain introduced by the SiN capping.

Figure 2 compares transconductance data for all splits with channel width/length $(W/L) = 10/0.4\ \mu m$. It can be seen that the transconductance of all SiN-capped samples, with or without HfO_2 buffer layer, depicts significant and identical enhancement of ~26% with respect to that of the control counterparts without SiN capping. Output characteristics of PMOSFETs are shown and compared in Fig. 3. Similar enhancement trend in the drive current is also observed for the two SiN-capping splits. These findings confirm the results obtained in stress measurements that the insertion of an ultrathin HfO_2 buffer layer does not compromise the performance enhancement induced by the SiN capping.

Figure 4 shows the percentage increase in transconductance for SiN-capped and HfO_2-buffered splits, compared to the control split, as a function of channel length. Each data represents the mean measurement result performed on eight devices in Fig. 4. Note that the strain is distributed locally inside the channel region and is concentrated near the source and drain region.[17,18] As the channel length becomes shorter, the distance from the edge of the spacer to the center of the channel becomes shorter; thus, the induced strain becomes stronger. Therefore, we can see that the transconductance enhancement increases with decreasing channel length, a unique feature for uniaxial strain induced by SiN capping.[17,18] Moreover, the induced compressive strain is not relieved by the insertion of the buffer layer. Capacitance–voltage (C-V) characteristics of all splits of samples coincide altogether, as shown in Fig. 5. Negligible differences in oxide thickness among these devices are observed, indicating that the above-mentioned observations, indeed, are not caused by the oxide thickness difference among splits. The subthreshold characteristics of PMOSFETs for all splits of samples are shown in Fig. 6. We can see that the subthreshold characteristics are not af-

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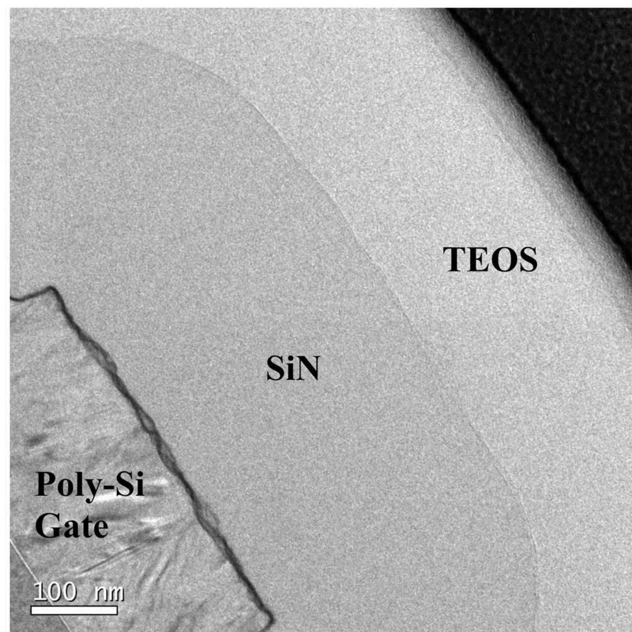

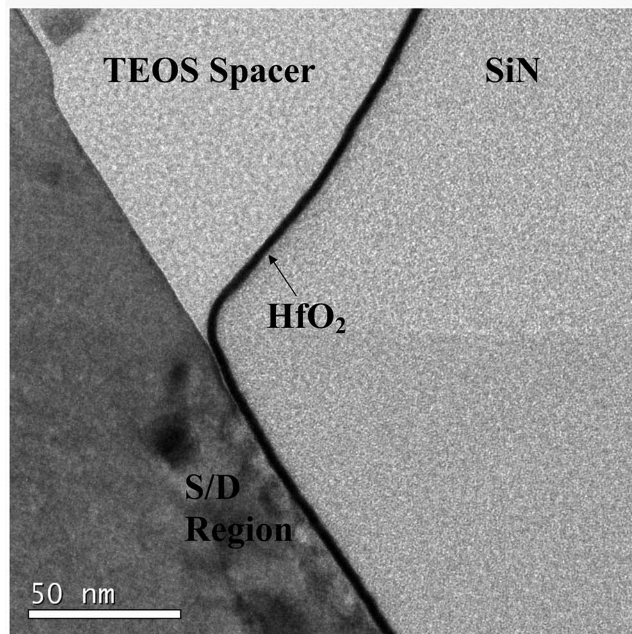

Figure 1. Cross-sectional TEM pictures of HfO_2-buffered samples taken in (a) the passivation region and (b) the spacer region. The thickness of SiN and HfO_2 buffer layer is roughly 310 and 3 nm, respectively.

fected by the presence of SiN and HfO_2-buffer layers. This is further convinced in Fig. 7, in which the mean value of the extracted subthreshold swing from ten devices is the same for the three splits of devices.

NBTI Characteristics

Figure 8 shows the results of NBTI stress performed at three different gate biases for HfO_2-buffered samples. It can be seen that larger gate bias leads to larger threshold voltage shift (ΔV_{th}), implying that more defects are being generated at higher bias. The shift curves show a fractional power-law dependence on time ($\Delta V_{th} \propto t^n$), and the values of the exponent (n) are roughly 0.3 for these

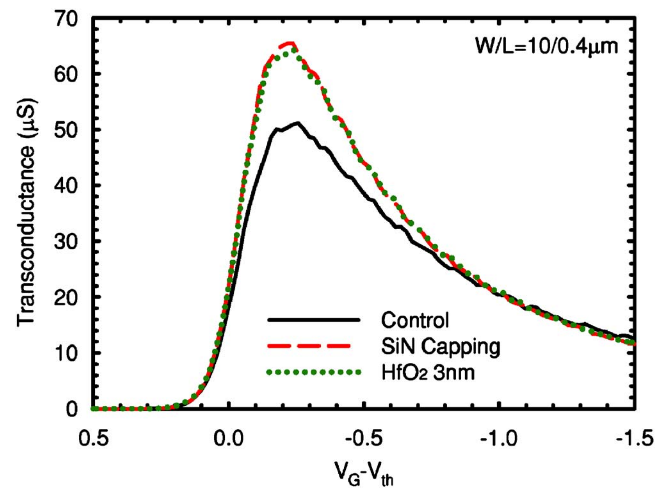

Figure 2. (Color online) Transconductance vs $V_G - V_{th}$ for all splits of samples. For the SiN-capped devices, with or without inserting the buffer layer, the transconductance is clearly increased with respective to the control.

samples. A comparison among the three splits of samples is given in Fig. 9, under the same stress condition, $V_G - V_{th} = -3.5$ V. It is seen that the SiN-capped split depicts much larger ΔV_{th} as compared to the control split. Such degradation is relieved when the HfO_2 buffer layer is added. After 1000 s stress, the ΔV_{th} is 46.12, 197.23, and 274.72 mV for control, HfO_2-buffered, and SiN-capped splits, respectively. Figure 10 compares the increase in interface state density (ΔN_{it}) and subthreshold swing shift (ΔSwing) for all samples extracted using the charge pumping technique. Basically the trends are similar to those shown in Fig. 9. Figure 11 shows the transconductance degradation ratio as a function of stress time. The transconductance degradation ratio for SiN-capped split depicts the severest degradation among all three splits, reaching 16% after 1000 s stress, implying that NBT stress grossly degrades the device performance and negates the benefit gained from the SiN capping, though the SiN capping can enhance carrier mobility in a fresh device. More importantly, the transconductance degradation is alleviated for HfO_2-buffered split. These results clearly indicate that the use of PE-SiN capping may aggravate NBTI, while the insertion of HfO_2 buffer layer can be helpful to relieve the situation. In short, although the capping of SiN tends to worsen the device reliability character-

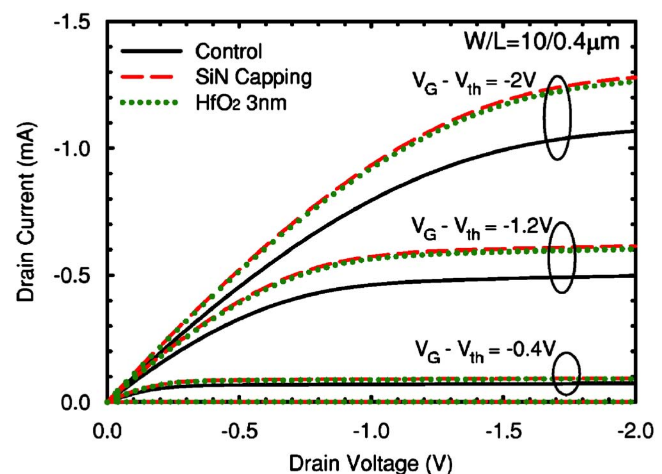

Figure 3. (Color online) Output characteristics of PMOSFETs for all splits. The insertion of the HfO_2 buffer in the SiN-capped device does not compromise the drive current enhancement with respective to the control.

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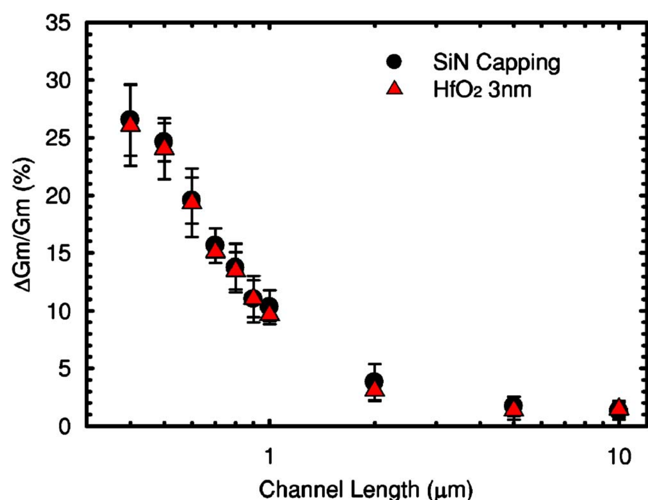

Figure 4. (Color online) Transconductance increase vs channel length. Each data point represents the mean measurement result performed on eight devices.

istics, the insertion of a thin HfO_2 buffer layer between the gate and the SiN can effectively shield the device against the degradation.

These findings are postulated to be related to the hydrogen species contained in the PE-SiN layer. Owing to the use of SiH_4 and NH_3 as the reaction precursors, the deposited SiN contains abundant hydrogen, as confirmed by the FTIR analysis shown in Fig. 12. In Fig. 12, visible H-bonding signals from the PE-SiN layer can be detected by Fourier transform infrared spectrometer (FTIR), indicating that the film indeed contains a substantial amount of hydrogen. It thus acts as a diffusion source for hydrogen to diffuse into the channel during the deposition process and subsequent thermal cycles, including the forming gas anneal. Although hydrogen can effectively passivate the dangling bonds at the SiO_2/Si interface, the passivated Si–H bonds are more easily broken during subsequent stressing; thus, the voluminous hydrogen species aggravate NBTI. The insertion of a thin HfO_2 buffer layer between the gate and SiN capping can effectively suppress the diffusion of hydrogen into the gate oxide and oxide/channel interface, resulting in less broken Si–H bonds and thus less newly generated interface states during stressing, as compared to the SiN-capped split. It is well known that the deposited HfO_2 layers typically contain a high density of structural defects.[19,20] We postulate that these defects tend to trap the hydrogen

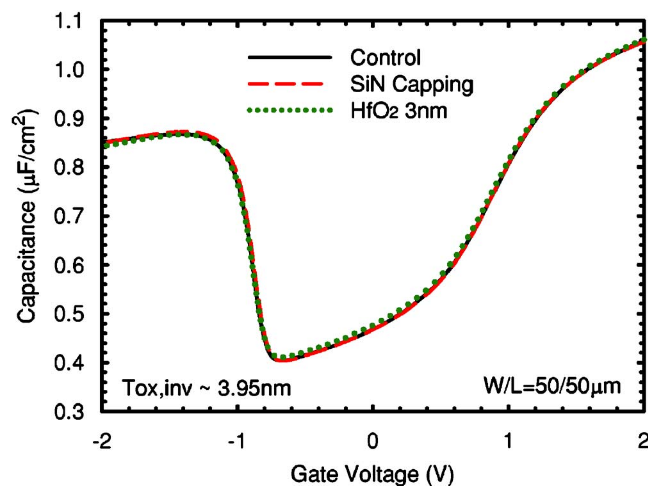

Figure 5. (Color online) Capacitance–voltage (C–V) characteristics of all splits. The curves are almost coincided with each other, indicating that the oxide thickness difference among the three splits is negligible.

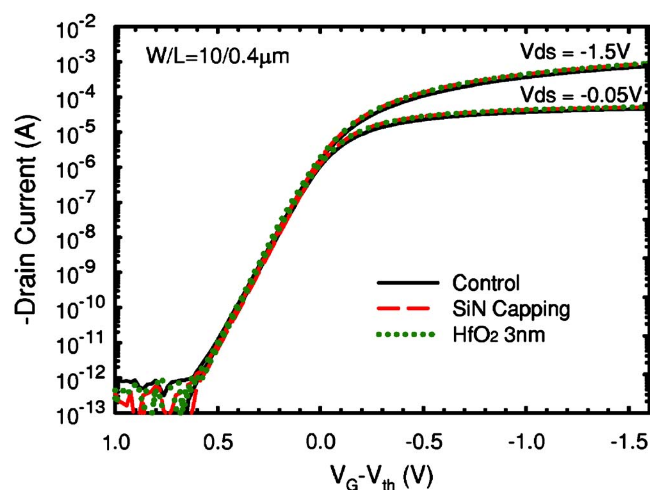

Figure 6. (Color online) Subthreshold characteristics of all splits.

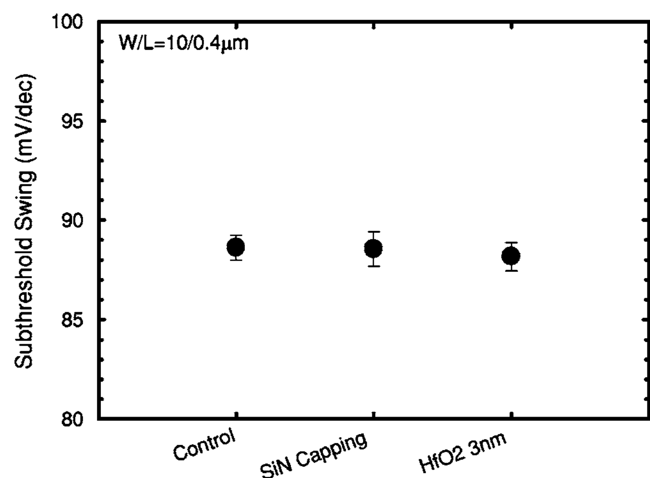

Figure 7. Subthreshold swing of all splits.

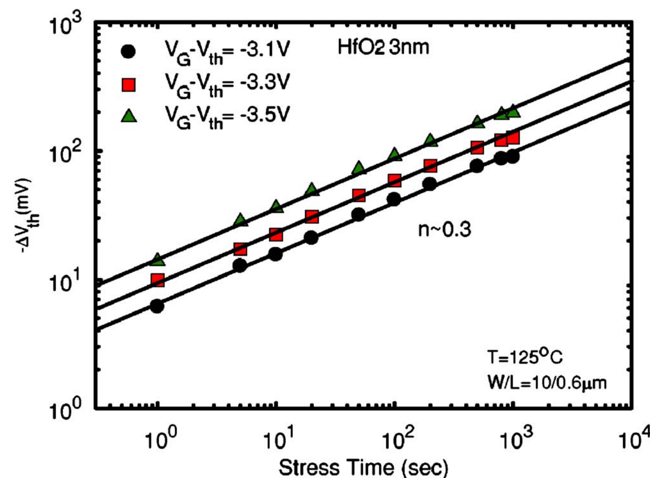

Figure 8. (Color online) Threshold voltage shift (ΔV_{th}) vs stress time for HfO_2-buffered split under three different gate biases at 125°C.

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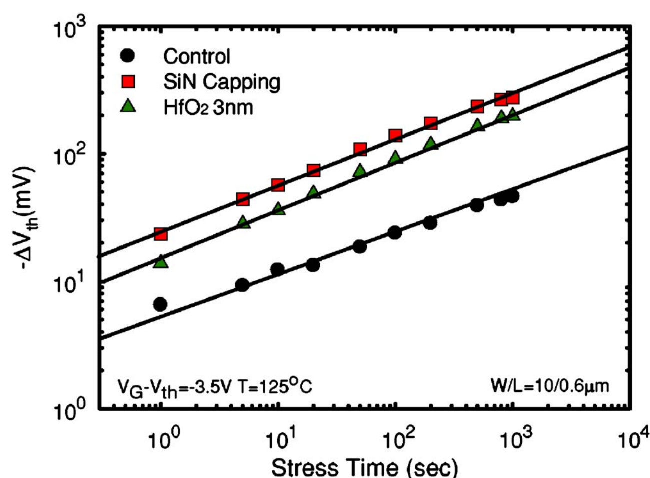

Figure 9. (Color online) Threshold voltage shift (ΔV_{th}) vs stress time for all three splits with $V_G - V_{th} = -3.5$ V at 125°C.

species diffusing during the SiN deposition and subsequent thermal cycles. As a result, the inserted HfO_2 acts as a diffusion barrier for hydrogen.

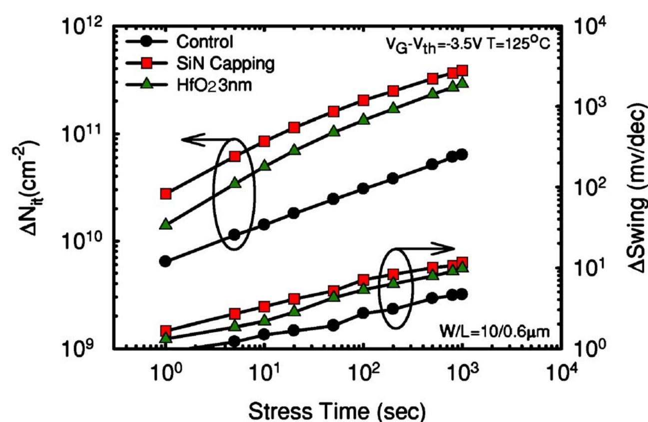

Figure 10. (Color online) Interface state generation (ΔN_{it}) and subthreshold swing degradation (ΔSwing) vs stress time for all three splits with $V_G - V_{th} = -3.5$ V at 125°C.

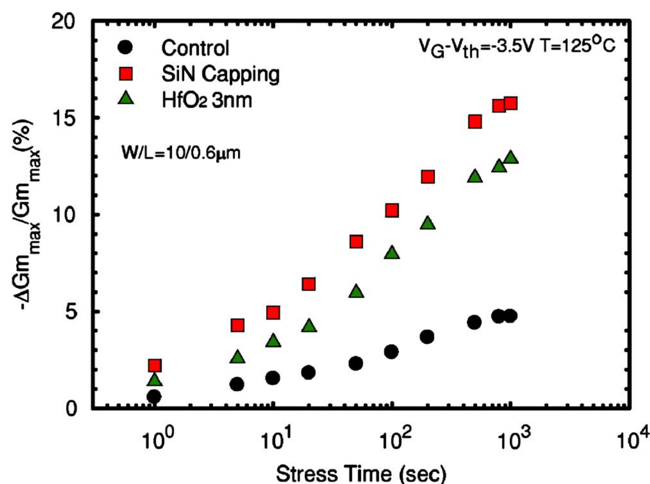

Figure 11. (Color online) Transconductance degradation vs stress time for all three splits with $V_G - V_{th} = -3.5$ V at 125°C.

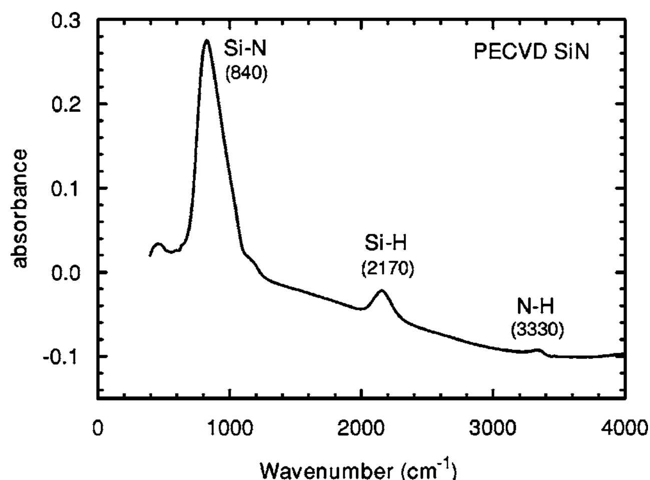

Figure 12. Bonding signals of PECVD-SiN layer by Fourier transform infrared spectrometer (FTIR).

In this study, the thickness of the HfO_2 buffer is fixed at 3 nm. Such a thin buffer layer would not compromise the performance gain obtained from the channel strain. In the meantime, the immunity against NBTI degradation is clearly demonstrated. However, it should be noted that the optimum thickness is yet to be determined. In this aspect more effort is in progress, and it is expected that further improvement in NBTI immunity is possible when the condition is optimized.

Conclusion

SiN-capped PMOSFETs with a thin HfO_2 buffer layer were fabricated and characterized in this study. Although the SiN layer tends to worsen the NBTI characteristics, our results demonstrate the usefulness of inserting a buffer layer in relieving the situation. Furthermore, no performance gain from the channel strain is compromised at all as the buffer layer is inserted. Such improvement is ascribed to the suppression of hydrogen diffusion from the SiN to the gate oxide and the oxide/channel interface with the insertion of the buffer layer.

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References

1. S. Ogawa, M. Shimaya, and N. Shiono, *J. Appl. Phys.*, **77**, 1137 (1995).
2. C. H. Liu, M. T. Lee, C. Y. Lin, J. Chen, Y. T. Loh, F. T. Liou, K. Schruefer, A. A. Katsetos, Z. Yang, N. Rovedo, et al., *Jpn. J. Appl. Phys., Part 1*, **41**, 2423 (2002).
3. D. K. Schroder and J. A. Babcock, *J. Appl. Phys.*, **94**, 1 (2003).
4. X. J. Zhou, L. Tsetseris, S. N. Rashkeev, D. M. Fleetwood, R. D. Schrimpf, S. T. Pantelides, J. A. Felix, E. P. Gusev, and C. D'Emic, *Appl. Phys. Lett.*, **84**, 4394 (2004).
5. M. A. Alam and S. Mahapatra, *Microelectron. Reliab.*, **45**, 71 (2005).
6. J. Ushio, T. Maruizumi, and K. K-Abdelghafar, *Appl. Phys. Lett.*, **81**, 1818 (2002).
7. S. Mahapatra, M. A. Alam, P. B. Kumar, T. R. Dalei, and D. Saha, *Tech. Dig. - Int. Electron Devices Meet.*, **2004**, 105.
8. S. Pidin, T. Mori, K. Inoue, S. Fututa, N. Itoh, E. Mutoh, K. Ohkoshi, R. Nakamura, K. Kobayashi, K. Kawamura, et al., *Tech. Dig. - Int. Electron Devices Meet.*, **2004**, 213.
9. K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, T. Hoffmann, A. Murthy, J. Sandford, R. Shaheed, et al., *Symp. VLSI Tech. Dig.*, **2004**, 50.
10. K. Ota, T. Sanuki, K. Yahashi, Y. Miyanami, K. Matsuo, J. Idebuchi, M. Moriya, K. Nakayama, R. Yamaguchi, H. Tanaka, et al., *Symp. VLSI Tech. Dig.*, **2006**, 78.
11. K. J. Chui, K. W. Ang, A. Madan, H. Wang, C. H. Tung, L. Y. Wong, Y. Wang, S. F. Choy, N. Balasubramanian, M. F. Li, et al., *Tech. Dig. - Int. Electron Devices Meet.*, **2005**, 493.

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12. C. Y. Lu, H. C. Lin, Y. F. Chang, and T. Y. Huang, *Jpn. J. Appl. Phys., Part 1*, **45**, 3064 (2006).
13. A. V.-Y. Thean, L. Prabhu, V. Vartanian, M. Ramon, B.-Y. Nguyen, T. White, H. Collard, Q.-H. Xie, S. Murphy, J. Cheek, et al., *Tech. Dig. - Int. Electron Devices Meet.*, **2005**, 409.
14. X. Chen, S. Fang, W. Gao, T. Dyer, Y. W. Teh, S. S. Tan, Y. Ko, C. Baiocco, A. Ajmera, J. Park, et al., *Symp. VLSI Tech. Dig.*, **2006**, 74.
15. C. Y. Lu, H. C. Lin, and T. Y. Huang, *Electrochem. Solid-State Lett.*, **9**, G138 (2006).
16. M. Yamamura, T. Matsuki, T. Robata, T. Watanabe, S. Inumiya, K. Torii, T. Saitou, H. Amai, Y. Nara, M. Kitazoe, et al., *Symp. VLSI Tech. Dig.*, **2005**, 88.
17. S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, *IEEE Electron Device Lett.*, **53**, 1010 (2006).
18. Q. Xu, X. Duan, H. Qian, H. Liu, H. Li, Z. Han, M. Liu, and W. Gao, *IEEE Electron Device Lett.*, **27**, 179 (2006).
19. K. Tse and J. Robertson, *Microelectron. Eng.*, **84**, 663 (2007).
20. A. S. Foster, F. L. Gejo, A. L. Shluger, and R. M. Nieminen, *Phys. Rev. B*, **65**, 174117 (2002).

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