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Electrical and Reliability Improvement in Polyoxide by Fluorine Implantation

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We show that the incorporation of fluorine into the oxide grown on polysilicon (polyoxide) not only improves the electrical characteristics (i.e., lower leakage current, higher electrical breakdown field), but also improves the reliability (lower electron trapping rate, larger Q_{bd}). This improvement is believed to be due to the stress relaxation of the polyoxide and smoother polysilicon/polyoxide interface by the fluorine incorporation. The optimum fluorine dose (2×10^{14}) shows the best characteristics such as E_{bd} over 12 MV/cm and $Q_{bd} \sim 2$ C/cm^2. However, excessive fluorination (1×10^{15}) seems to result in performance degradation due to the generation of nonbridging oxygen centers.
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Fluorinated gate oxide dielectrics have attracted considerable attention over the past years.[1-8] The incorporation of approximate amounts of F into the oxide near the Si/SiO_2 interface was shown to improve the oxide breakdown distribution and the interface hardness against hot-electron and radiation damages of metal-oxide-semiconductor (MOS) devices.[9-14] The improved reliability is that fluorine can break strained Si–O–Si bonds to cause local strain relaxation, and fluorine in the oxide can replace weak Si–H bonds to form strong Si–F bonds.[15] The oxides grown incorporated with fluorine had also been reported to cause local strain-stress relaxation and to exhibit less interface state density because of the passivation of interface defects such as dangling bonds and strain bonds.[16] Recently, the effects of fluorine on the defect passivation and the hot carrier endurance of polysilicon thin-film transistors (TFTs) due to the similarity between the poly-Si/SiO_2 interface and the polysilicon grain boundaries were investigated.[17-19] The fluorine implantation not only improved the electrical characteristics such as on current, subthreshold swings, and mobility, but also improved the hot carrier immunity of the device[20,21] due to the fluorine passivation more uniformly reducing the trap states in the band tail and those in the midgap.

The quality of polysilicon oxide (polyoxide) plays an important role in the performance of polysilicon TFTs[22] and nonvolatile memories.[23] The electrical properties of the polyoxide are mainly determined by the polysilicon/polyoxide interface roughness.[24] It had been demonstrated that the rough and nonuniform surface at the polysilicon/polyoxide interface enhanced the local electric field and resulted in low breakdown strength as compared to single crystalline silicon oxide.[25] It had also been reported that a compressive stress two or more times larger than the stress in the thermal oxide of single crystal was formed on the thermally grown polyoxide. This increased stress in thermal polyoxide is due to the oxidized polysilicon at grain boundaries enhancing the interface roughness, and causing an additionally compressive stress.[26]

In this work, we show that the fluorine ions are directly implanted into the bottom polysilicon and the fluorinated polyoxides are grown in dilute ($N_2 + O_2$) ambient. It is found that the introduction of fluorine into polyoxide not only reduces the leakage current and increases the breakdown strength of the polysilicon/polyoxide interface, but also improves the reliability such as smaller trapping rates and larger charge-to-breakdown (Q_{bd}). This improvement is believed to be due to the stress relaxation of the polyoxide and smoother polysilicon/polyoxide interface by the fluorine incorporation.

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Experimental

At first, the p-type Si wafers were thermally oxidized to have an oxidized layer of 100 nm thickness. A polysilicon film (bottom polysilicon) of 300 nm thickness was then deposited at 625°C and subsequently doped with $POCl_3$ at 950°C. A half-hour drive-in process was performed in a $N_2 + O_2$ dilute ambient at 1000°C not only to obtain a sheet resistance of 30 Ω/cm, but also to grow a 200 Å pad oxide. Fluorine ions with various doses of 5×10^{13}, 2×10^{14}, and 1×10^{15} cm^{-2} at 40 keV were implanted through the pad oxide to the bottom polysilicon and then annealed at 900°C for 60 min in a N_2 ambient. The pad oxide was removed and then a 120 Å polyoxide was grown at 900°C for 20 min in dilute ($N_2 + O_2$) ambient. Another 300 nm polysilicon film (top polysilicon) was deposited and also doped with $POCl_3$ at 950°C. After defining the top gate pattern, 100 nm oxides were grown on all samples, as passivation layers, via wet oxidation. Contact holes were opened, and Al was deposited and then patterned. Finally, all devices were sintered at 350°C for 40 min in a N_2 gas.

Polyoxide thickness was determined by high-frequency (100 kHz or 1 MHz) capacitance-voltage (C-V) measurements. The amounts of fluorine in the polyoxide were measured using secondary ion mass spectroscopy (SIMS) with Cs^+ as the primary ions. The morphology of the polyoxide/polysilicon interface was studied by atomic force microscope (AFM). For the AFM measurement of the surface to reveal the polyoxide/poly-1 interface, the polyoxide layer was removed by wet etching by using buffered HF acid. The true replica of the interface may be preserved by such a treatment because the poly-Si is not attacked by the HF-based solution.[27] The electrical characteristics were obtained by an HP4145B semiconductor parameter analyzer.

Results and Discussion

The SIMS profiles of fluorine for the devices implanted with 5×10^{13}, 2×10^{14}, 1×10^{15} F^+/cm^2 and without fluorine implantation followed by annealing at 900°C in N_2 ambient are shown in Fig. 1. Most of the fluorine accumulated within the polyoxide, and the higher the fluorine dose, the higher the fluorine peak value. There are also some amounts of fluorine existing, especially within the bottom polysilicon. A set of the typical J-E characteristics of nonimplanted and fluorine-implanted polyoxides is shown in Fig. 2a and b, respectively. It is clear that all the fluorine-implanted polyoxides have lower leakage currents and higher breakdown electric fields than those of the nonimplanted polyoxide for both cases of positive gate bias (electron injection from the bottom polysilicon interface) and negative gate bias (electron injection from the top polysilicon interface). The improvements of the electrical characteristics are believed to be due to the fact that the implanted fluorines can passivate the dangling bonds and break the strained Si–O–Si bonds to form Si–F bonds in the polysilicon grain boundaries and polyoxide/polysilicon interface.[16,28,20] So, the local stress can be re-

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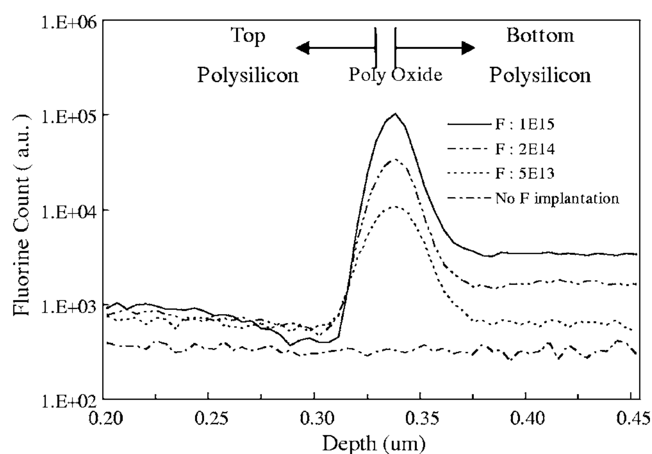

Figure 1. The SIMS profiles of fluorine for the devices implanted with 5×10^{13}, 2×10^{14}, 1×10^{15} F^+/cm^2 and without fluorine implantation, respectively.

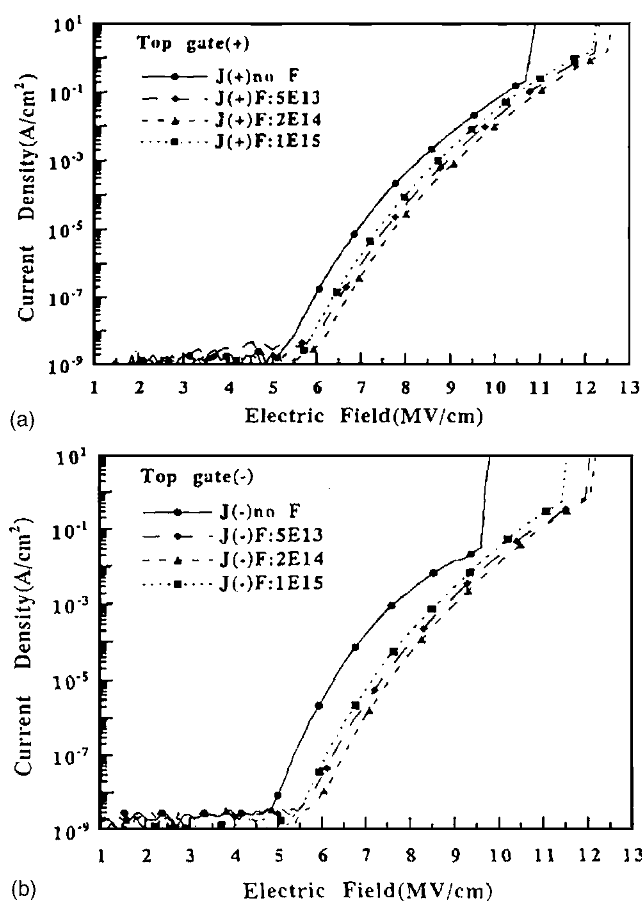

Figure 2. The *J-E* characteristics of the polyoxides implanted with different doses of fluorine under (a) the positive gate bias, and (b) the negative gate bias.

laxed in the oxide network and make the polysilicon/polyoxide interface morphology smoother. Because the stress between the polyoxide and the polysilicon affects the polyoxide breakdown strength, the lower the oxide stress, the higher the oxide breakdown strength.[29]

In this experiment, we found that the optimum dose of fluorine to obtain the best polyoxide *J-E* characteristics is 2×10^{14} cm^{-2}. But too much fluorine (1×10^{15} cm^{-2}) seems to cause degradation of the polyoxide characteristics. The degradation observed for the highest implanted (1×10^{15} cm^{-2}) sample could be due to higher implantation damage in bottom polysilicon at a higher dose, and during annealing defect distribution can cause degradation in oxide characteristics. Besides, Nishioka et al.[30] have reported that excessive fluorination may result in a high density of nonbridging oxygen centers to induce performance degradation through the O displacement by F from strained Si–O–Si bonds, despite accompanying a local strain relaxation which suppresses the defect migration. However, it still had better characteristics than that of the nonimplanted sample. Figure 3a-c shows the AFM images of bottom polysilicon surface for nonimplanted and 2×10^{14}, 1×10^{15} fluorine/cm^2 implanted samples, and the average roughness (R_a) values of AFM are 58, 35, and 32 Å, respectively. It is clearly seen that the fluorine-implanted samples had more smooth surfaces than that of the nonimplanted sample. This is due to the incorporated fluorine breaking the strain bonds to form stronger Si–F bonds in the interface, thereby making the surface morphology smoother. Although the 1×10^{15} dosage sample had similar surface morphology as 2×10^{14} dosage sample, too much fluorine (1×10^{15}) still results in inferior characteristics as shown in Fig. 2.

The fluorine-implanted polyoxides also exhibit larger reliability improvement. The charge trapping characteristics of the fluorine-implanted polyoxides were investigated. Figure 4 shows the curves of gate voltage shift (ΔV_g) vs time of the polyoxides without and with different dosages of fluorine implantation under a constant ± 100 $\mu A/cm^2$ current stressing. The test capacitor area was 5×10^{-4} cm^2. All the increase in the gate voltage is due to electron trappings. All the fluorine-implanted samples had smaller voltage shifts than the nonimplanted sample under the positive and negative current stresses. This means that the fluorine can passivate or reduce the generated traps and defects by the dangling and strain bonds in the polyoxide/polysilicon interface and grain boundaries, so the fluorine-implanted polyoxides trap fewer electrons than the nonimplanted polyoxide.[31] The optimum dose of fluorine (2×10^{14}) also had the best trapping characteristics for both direction current stresses. In nonvolatile memory cells, the charge-to-breakdown (Q_{bd}) is also a critical parameter of interest. Figure 5 shows the Weibull charge-to-breakdown (Q_{bd}) plot for the polyoxides without and with different fluorine doses implantation under ± 10 mA/cm^2 stress. The fluorine-implanted polyoxides had larger Q_{bd} with narrower Q_{bd} distribution than those of the nonimplanted polyoxide. This should be due to the reduced electron trapping shown in Fig.4. The values of the charge-to-breakdown (Q_{bd}) under the positive stress were larger than those under the negative stress for all the polyoxides. Moreover, the Q_{bd} improvement of the fluorine-implanted polyoxide is apparent for the $+V_g$ stress. This is also due to the incorporated fluorine breaking the strain bonds to form more strong Si–F bonds in the interface, thereby making the surface morphology smoother to reduce electron trapping rate. The fluorine implanted dose (2×10^{14} cm^{-2}) of polyoxide has the largest Q_{bd} (~ 2 C/cm^2) for the $+V_g$ stress. However, excess amount of fluorine (1×10^{15} cm^{-2}) seemed to reduce the Q_{bd} improvement.

Conclusion

In conclusion, the above results show that the incorporation of fluorine in the polyoxide not only improves the electrical characteristics (i.e., lower leakage current, higher electrical breakdown field), but also improves the reliability (lower electron trapping rate, larger Q_{bd}). This improvement is believed to be due to the stress relaxation of the polyoxide and smoother polysilicon/polyoxide interface by the fluorine incorporation. The optimum fluorine dose (2×10^{14}) shows the best characteristics such as E_{bd} over 12 MV/cm and $Q_{bd} \sim 2$ C/cm^2. However, excessive fluorination (1×10^{15}) seems to result in performance degradation due to the generation of nonbridging oxygen centers.

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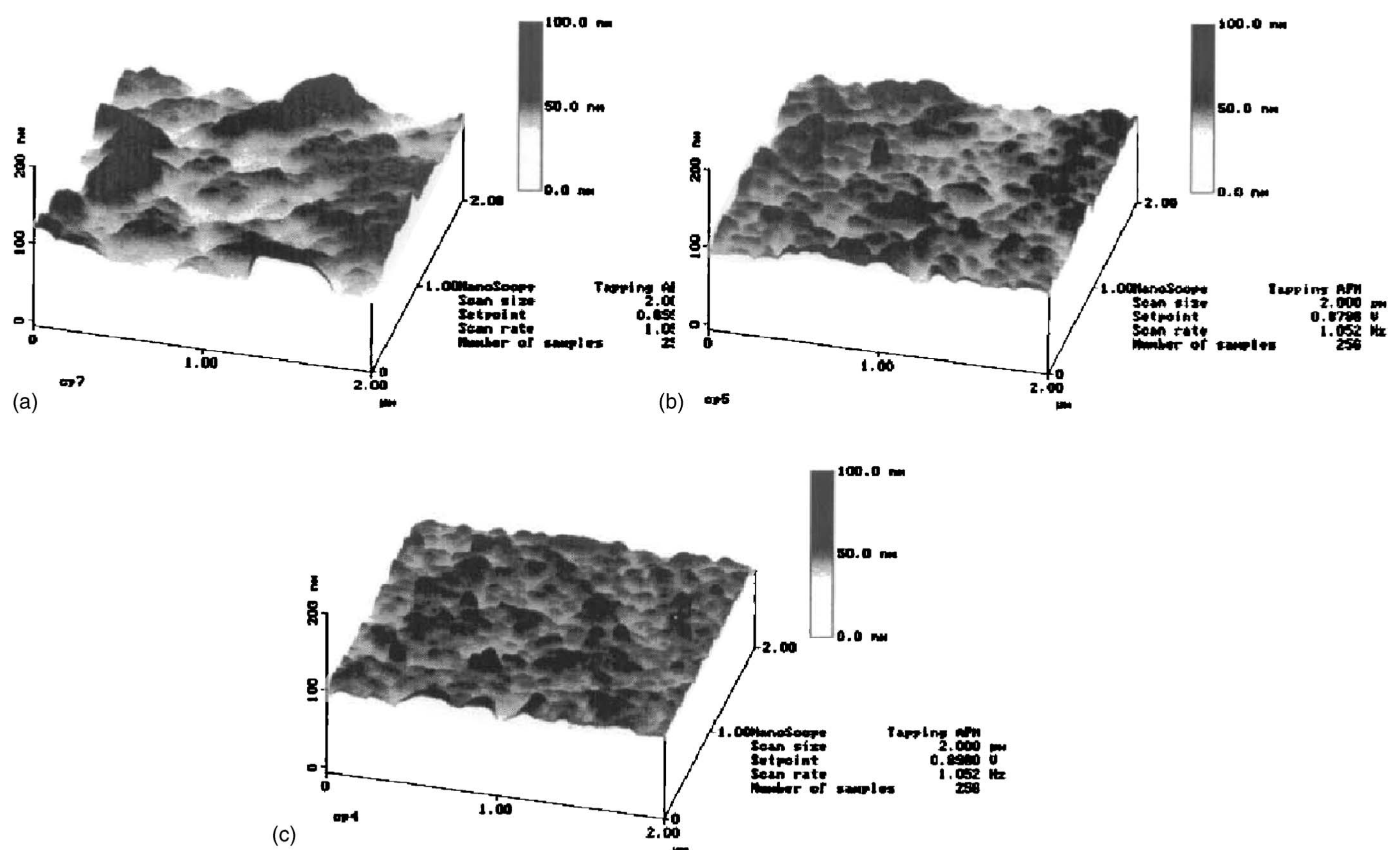

Figure 3. The AFM images of bottom polysilicon surface for (a) nonimplanted, (b) 2×10^{14}, and (c) 1×10^{15} F^+/cm^2 implanted samples, respectively.

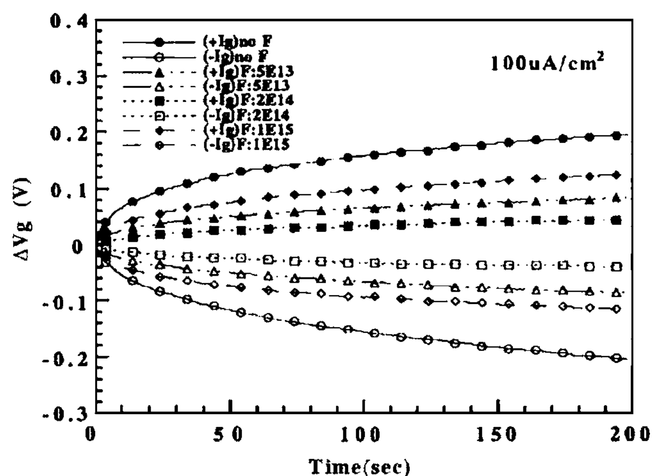

Figure 4. The curves of gate voltage shift (ΔV_g) vs time of the polyoxides without and with different dosages of fluorine implantation under a constant ± 100 $\mu A/cm^2$ current stressing.

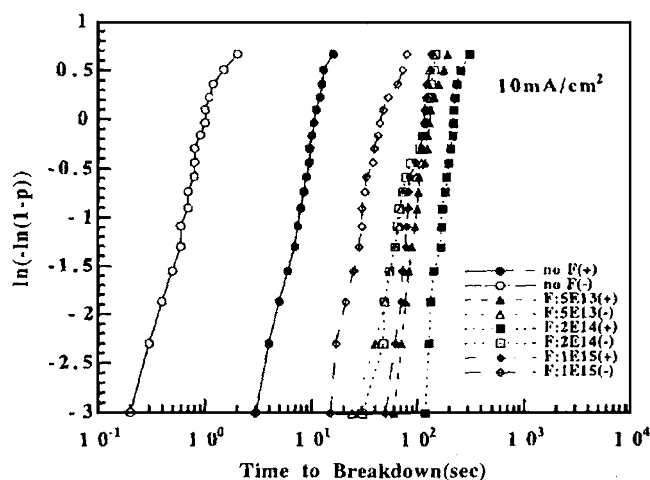

Figure 5. The Weibull charge-to-breakdown plots for the implanted polyoxides and nonimplanted polyoxide devices under both positive and negative current stress. A constant current density of 10 mA/cm^2 was applied to capacitors with an area of 5×10^{-4} cm^2.

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