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Plasma-Induced Damage on the Performance and Reliability of Low-Temperature Polycrystalline Silicon Thin-Film Transistors

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We have investigated the impact of plasma-induced damage on the performance and reliability of low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs). The LTPS TFTs having different antenna structures were used to study the effects of the plasma-etching process. We observed that performance instability occurred for the devices having a relatively large-area antenna. Plasma damage mainly caused nonuniform distribution of the threshold voltages in the LTPS TFTs, presumably because of charge trapping in the gate dielectric during the plasma-etching process. The reliabilities of the LTPS TFTs having larger antenna areas were found to be more degraded under gate-bias stress and hot-carrier stress than those of the samples having smaller antenna areas. Because of their enhanced plasma damage, we speculate that the LTPS TFTs having larger antenna areas possess more trap states in the gate dielectrics. During gate-bias stress or hot-carrier stress, therefore, charges can be injected into the gate dielectric through trap-assisted tunneling, resulting in significant degradation of both the performance and reliability.
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Polycrystalline silicon thin-film transistors (poly-Si TFTs) are key devices in flat-panel displays (FPDs), such as active-matrix liquid crystal displays (AMLCDs).[1] The high mobility of poly-Si TFTs enables the integration of the pixels and the driving circuit onto a single panel. This yields a light and thin display with a reduced number of connection pins; it also improves both the reliability of the panels and the resolution of the displays.[2] To achieve good process repeatability and precise control over the feature sizes in the insulators, semiconductors, and metals, plasma-etching processes are widely adopted during very-large-scale integration (VLSI) and poly-Si TFT fabrication. Many reports have highlighted that plasma processing during VLSI manufacturing may induce device degradation.[3,4] When an isolated object comes into contact with plasma, a net negative charge accumulates very rapidly on the object because electrons are the lightest and hottest particles. This situation leads to the buildup of negative potential, called the floating potential (V_f), with respect to the plasma potential (V_p). The floating potential continues to increase until the net flux of arriving negative charges on the isolated object is equal to the net flux of positive charges.[5] However, plasma nonuniformity leads to a local imbalance between the flux of the positive and negative charges, causing charge accumulation by the isolated object.[6] If a conducting layer is connected to the gate oxide and then subjected to plasma etching, the layer completely covers the wafer during most of the etching process; charges flow through the layer to balance the local nonuniformity of the charge flux such that no charge accumulates on the layer. When the conducting layer is nearly completely etched, however, the layer eventually becomes discontinuous, leading to the onset of local charge accumulation and damage to the gate oxide.[7] In addition, during the overetching step of the photoresist stripping process, the entire wafer surface is exposed to the plasma, causing charge to accumulate on the conducting layer. The charge collected by the conducting layer causes stress to the gate oxide. When the plasma nonuniformity is sufficiently large and the electric field across the gate oxide exceeds a critical value, electron injects through the gate oxide via Fowler-Nordheim tunneling, causing deterioration of the oxide quality and integrity.[8] The injection process could occur through either substrate injection or gate injection, depending upon the potential distribution at the wafer surface during the plasma process.[9] Moreover, the degree of plasma damage is strongly related to the topography of the gate interconnect. The charging effect is amplified by the ratio of the areas of the conducting layer and the gate, the so-called antenna area ratio (AR). This phenomenon, however, has only rarely been investigated in low-temperature polycrystalline (LTPS) TFTs. Some studies have indicated that plasma processing may degrade the performance of poly-Si TFTs through such phenomena as crystal damage, exposure damage, radiation damage, and charging damage;[10,11] however, the effect of plasma processing on the performance and reliability of LTPS TFTs has not been explored to an appropriate degree.

In this study, we investigated the impacts of plasma-induced damage on LTPS TFTs having various antenna structures. Moreover, to investigate the effects of plasma damage on the reliability of the LTPS TFTs, we applied both gate-bias stress and hot-carrier stress to the samples.

Experimental

n-Channel LTPS TFTs with lightly doped drain (LDD) were fabricated on glass substrates with top-gate structures. A 400 Å amorphous-Si layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300°C on a buffer layer and then crystallized into a poly-Si film by excimer laser annealing. Channel doping was then performed through implantation for threshold voltage adjustment. After source and drain formation through plasma doping, the gate dielectric was deposited with 1000 Å SiO_2 by plasma enhanced chemical vapor deposition (PECVD) at 300°C. Mo was deposited with a thickness of 3000 Å and patterned as the gate electrode. After gate formation, the LDD with a length of 1.5 μm was formed by self-aligned process. Then, 5000 Å SiO_2 was deposited as the interlayer dielectric and densified through rapid thermal annealing at 700°C for 30 s. The dopants were also activated during the densification process. Finally, 5000 Å Al was deposited and patterned as the interconnection metal.

A schematic cross-sectional diagram and the antenna geometry of the test structure are presented in Fig. 1a and b, respectively. The antenna AR is defined as

$$\mathrm{AR} = \frac{\text{antenna area}}{\text{gate area on active region } (L \times W)} \quad [1]$$

To study the effects of antenna area on the characteristics of the LTPS TFTs, two sets of antenna patterns were designed; their parameters are detailed in Tables I and II. The first series of devices were designed to have fixed channel widths (W) and channel lengths

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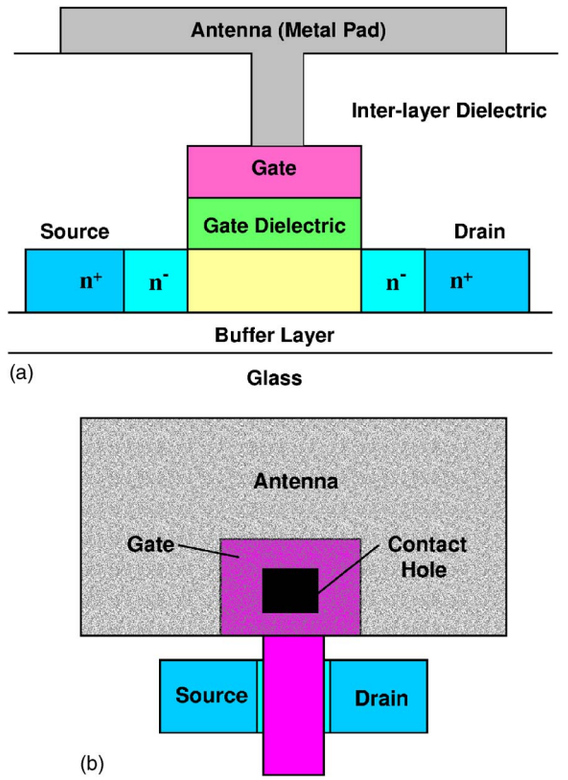


Figure 1. (Color online) (a) Schematic cross-sectional diagram and (b) antenna geometry of the test LTPS TFT structure used in this study. The antenna AR is defined as the antenna area divided by the gate area on the active region.

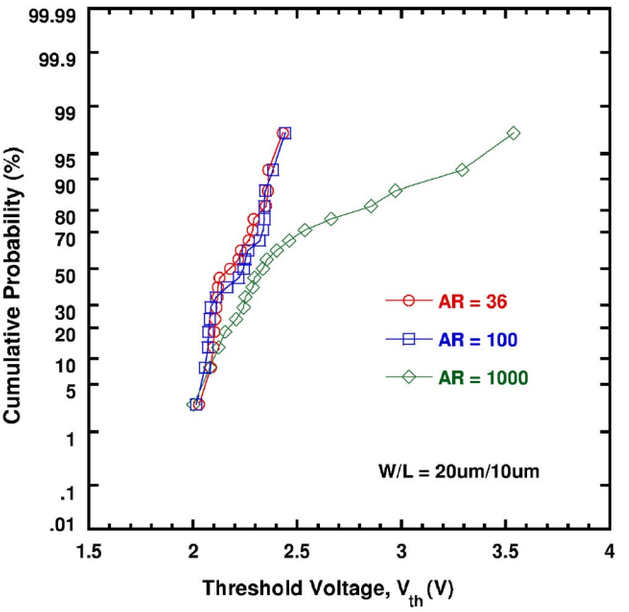


Figure 2. (Color online) Cumulative probabilities of the threshold voltages for the LTPS TFTs having various antenna ARs. The threshold voltage was measured a constant drain current I_{DS} of 10 nA × (W/L) at a value of V_{DS} of 0.1 V.

(L) of 20 and 10 μm, respectively; their values of AR were varied from 36 to 1000. The second series of devices were designed to have a fixed AR of 1000, and the channel widths were varied from 5 to 30 μm at a fixed channel length of 5 μm.

Results and Discussion

Fixed device size/various AR.— There are many device parameters that can be used to check plasma-induced damage, such as the threshold voltage, drive current, and gate-leakage current.[12] In our experiments, we found that the threshold voltage distribution of the LTPS TFTs displayed a clear dependence on the AR (Fig. 2). The threshold voltage distribution degraded as the AR increased up to 1000. When the device was exposed to plasma, local charge accumulated on the conducting layer to create a voltage across the gate dielectric. Such stress causes charge injection through the gate oxide and creates numerous trap states within it.[11] Therefore, as a result of the enhanced degree of plasma damage, the LTPS TFTs having larger values of AR exhibited greater instability in their threshold voltages than did those having smaller values of AR.

Figure 3a displays the transfer characteristics of the LTPS TFTs before and after gate-bias stress for 1000 s. The gate-bias stress was performed by applying a voltage of 30 V to the gate while the source and drain were grounded. Obviously, the threshold voltage shifted to the positive direction after gate-bias stress, while the subthreshold swing changed only slightly. It has been reported that the subthreshold swing degradation is closely related to the generation of interface states located near the mid-gap (deep interface states); in contrast, the threshold voltage shift is closely related to deep interface-state generation and charge injection into the gate oxide.[13] Because the subthreshold swing remained almost unchanged in our experiment after gate-bias stress, the generation of deep interface states can be ruled out. As a result, we conclude that the threshold voltage shift was due mainly to charge injection into the gate dielectric. Figure 3b displays the time dependence of the threshold voltage shift of the LTPS TFTs having various values of AR under gate-bias stress. Although the rate of threshold voltage shift for each of the three devices was almost identical, the LTPS TFT having the largest AR exhibited the largest threshold voltage shift, indicating that more charges were trapped in the gate dielectric.

Because we applied a stress voltage of 30 V to the gate, there are probabilities that holes could be injected into the gate dielectric from the metal gate and that holes could be generated in the gate dielectric. However, holes have a much higher tunneling barrier and a larger effective mass than do electrons, which leads us to neglect the tunneling effects of holes. Furthermore, due to the thick gate dielectric, the oxide field (ca. 3 MV/cm) was not sufficiently high to make electrons tunnel into the gate oxide and generate electron–hole pairs in it. Therefore, the generation of holes in the gate oxide can be neglected. The experimental results show that the threshold voltage

Table I. Antenna patterns having a fixed gate area on the active region and various values of ARs.

W/L (μm/μm)	AR	Antenna area = ($W \times L$) × AR (μm^2)
20/10	36	7200
20/10	100	20000
20/10	1000	200000

Table II. Antenna patterns having a fixed AR of 1000 and various channel widths.

W/L (μm/μm)	AR	Antenna area = ($W \times L$) × AR (μm^2)
5/5	1000	25000
20/5	1000	100000
30/5	1000	150000

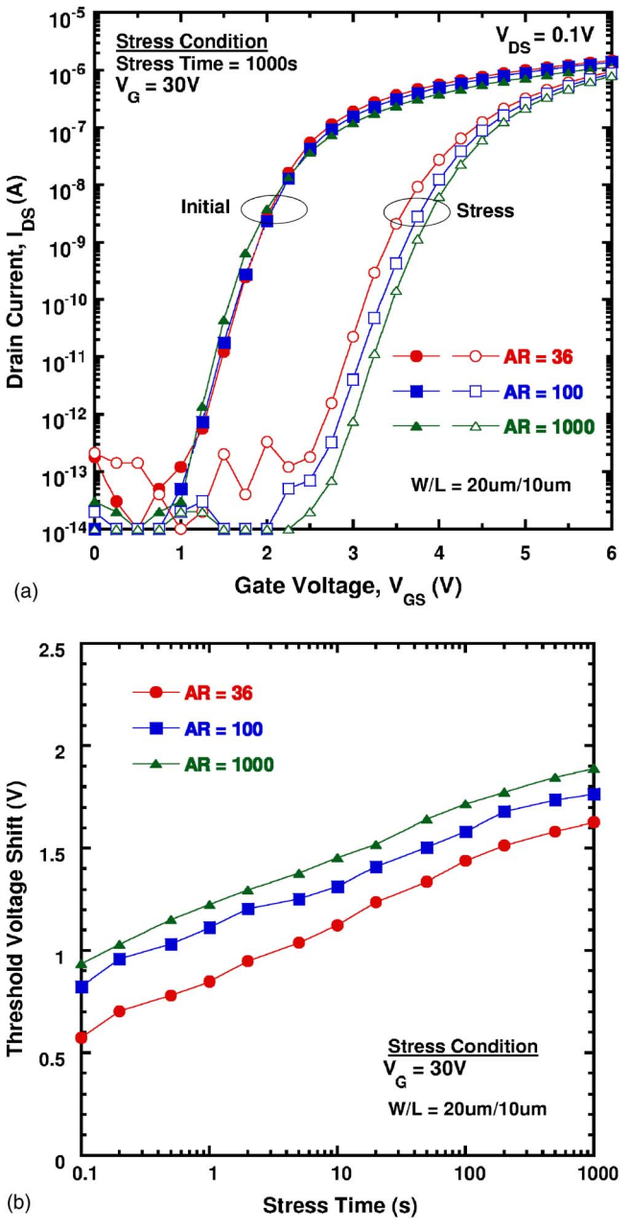


Figure 3. (Color online) (a) Transfer characteristics and (b) time dependence of the threshold voltage shifts of the LTPS TFTs having various values of AR under a gate-bias stress. Stress conditions: $V_D = V_S = 0$ V; $V_G = 30$ V.

moved in the positive direction after stress; this further confirms that the degradation mechanism was not dominated by hole injection or generation in the gate oxide.

It has been reported that plasma-induced damage creates numerous trap states in the gate dielectric and that the number of these trap states depends on the degree of damage.[14] The LTPS TFTs having larger values of AR experienced a greater degree of plasma damage, therefore, more trap states were generated in the gate dielectric. When a gate bias of 30 V was applied to stress the device, the oxide field (ca. 3 MV/cm) was not sufficiently high to damage the gate dielectric; this situation, however, was true for the oxide that had not been subjected to plasma damage. The plasma processes induce many trap states in the gate dielectric. Those trap states enhance the probabilities of both electron injection and trapping in the gate dielectric through trap-assisted tunneling, which results in a threshold voltage shift during stress.[15] Figure 4 presents the schematic diagram illustrating the degradation mechanism of the LTPS TFT under gate-bias stress. Therefore, because of the greater number of trap states in the gate dielectric, we suggest that more electrons were trapped in the gate dielectric through trap-assisted tunneling for the device having a large value of AR, resulting in a large threshold voltage shift.

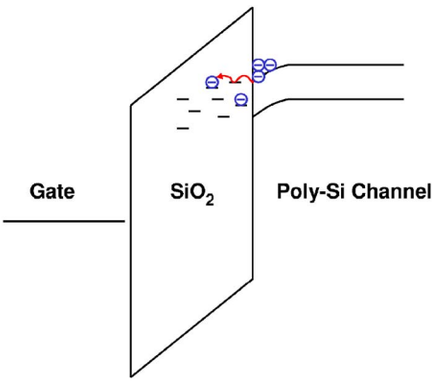
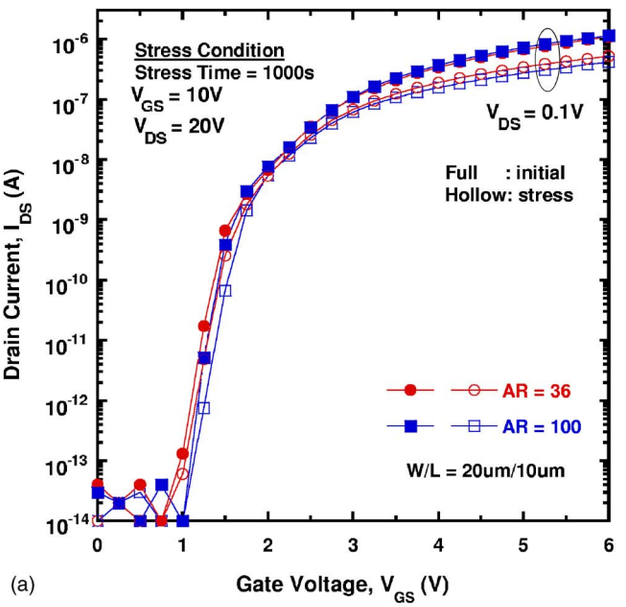


Figure 4. (Color online) Schematic representation of trap-assisted tunneling under a positive gate-bias stress.

In this study, hot-carrier stress ($V_{GS} = 10$ V; $V_{DS} = 20$ V) was also applied to identify the effects the plasma damage. Figure 5a displays the transfer characteristics of the LTPS TFTs having values of AR of 36 and 100 both before and after hot-carrier stress. Figure 5b presents the time dependence of the drive-current degradations, defined as $-\Delta I_{DS}/I_{DS} \times 100\%$, of the LTPS TFTs having various values of AR under hot-carrier stress. Although the threshold voltage and subthreshold swing remained almost unchanged after stress, the drive current decreased accordingly. When a hot-carrier stress is applied to the device, a high field is induced near the drain junction, causing impact ionization and leading to the generation of electron–hole pairs. The generated hot carriers create trap states near the drain junction and reduce the field-effect mobility by increasing the potential barrier for the carriers to migrate from the source to the drain.[16,17] Moreover, because the drive current and field-effect mobility degraded similarly in our experiments, we attribute the drive-current degradation to the degradation of the field-effect mobility. We found that the LTPS TFTs having larger values of AR exhibited greater degrees of drive-current degradation; therefore, we conclude that plasma damage affected the immunity of the LTPS TFTs against hot-carrier stress.

Fixed AR/various device sizes.— Figures 6-9 show the results of the same series of experiments performed using the second series of devices. The devices were designed to have a fixed AR of 1000, with the channel widths varied from 5 to 30 μm at a fixed channel length of 5 μm. Figure 6 presents the threshold voltage distributions of these devices. The antenna area was proportional to the gate area on the active region ($L \times W$) to maintain the values of AR constant at 1000. As the channel width increases, the antenna area increases. The larger antenna area may induce a greater degree of plasma damage on the gate dielectric. Therefore, the TFT having a 30 μm wide channel exhibited a poorer threshold voltage distribution than those having smaller channel widths because different antenna areas were exposed to the plasma.

Figure 7 reveals the time dependence of the threshold voltage shift of the LTPS TFTs under gate-bias stress. The LTPS TFTs having larger channel widths exhibited larger threshold voltage shifts. Because a greater antenna area enhances the plasma damage and creates a greater number of trap states in the gate dielectric, electrons are more likely to be injected into the gate dielectric through trap-assisted tunneling, leading to a larger threshold voltage shift. Therefore, devices having larger channel widths display a greater threshold voltage shift under gate-bias stress.



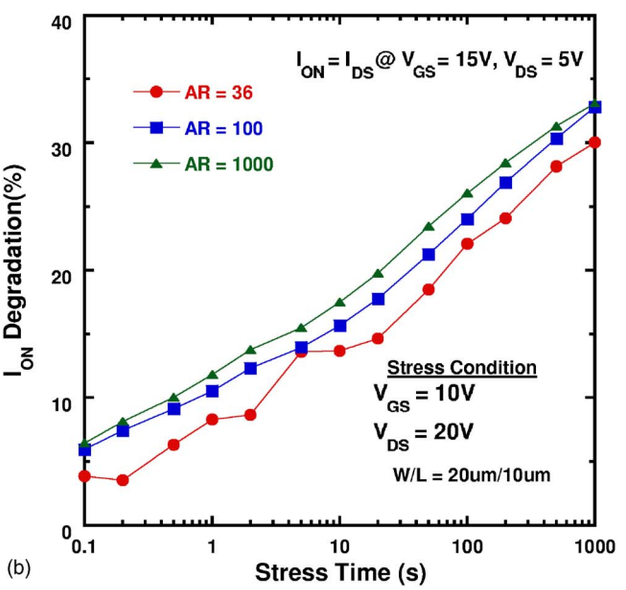


Figure 5. (Color online) (a) Transfer characteristics and (b) drive current degradation of the LTPS TFTs having various values of AR under a hot-carrier stress. Stress conditions: V_{GS} = 10 V; V_{DS} = 20 V.

Figure 8a shows the threshold voltage shifts of the LTPS TFTs under hot-carrier stress. The LTPS TFT having the smallest channel width exhibited the smallest threshold voltage shift. The threshold voltage shifts of the devices having channel widths of 20 and 30 μm exhibited two degradation regimes. In the first regime, the threshold voltage shift moved increasingly toward negative values upon increasing the stress time; in the second regime, however, the threshold voltage shift moved toward a positive value after a certain time. To explain these phenomena, the output characteristics of the pre-stress devices were monitored and shown in Fig. 8b. We found that the drain current increased upon increasing the drain voltage in the saturation region; this phenomenon is referred to as the so-called "kink effect."[18,19] The small circles (O) in this figure mark the hot-carrier stress conditions that we used in this study. The kink effect increased upon increasing the channel width under our hot-carrier stress conditions (V_{GS} = 10 V; V_{DS} = 20 V).

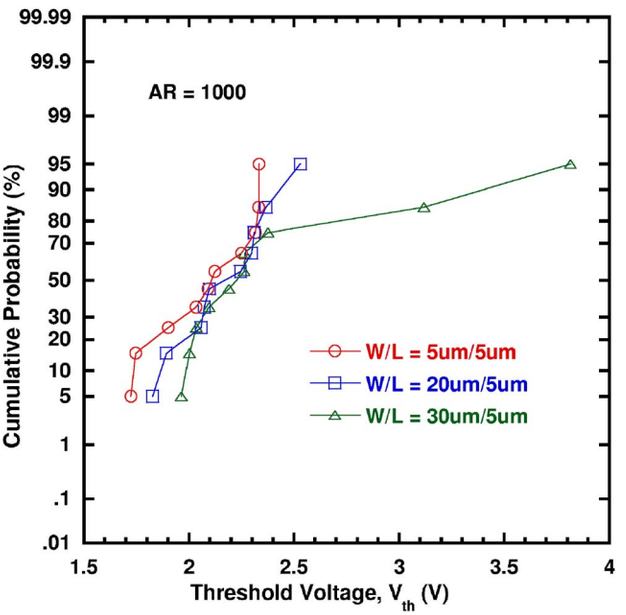


Figure 6. (Color online) Cumulative probabilities of the threshold voltages for the LTPS TFTs having different channel widths and a fixed AR of 1000. The antenna area was proportional to the gate area on the active region to maintain a constant AR.

For the devices having channel widths of 20 and 30 μm we believe that the kink effect was responsible for the negative shift of the threshold voltages. During hot-carrier stress, the impact-ionization-generated holes accumulate in the channel region. These holes may be initially trapped or compensate the trapped electrons that are pre-existing at the Si/SiO_2 interface and grain boundaries. Besides, at a fixed AR of 1000, the plasma damage is enhanced for the device having a larger channel width that may also create a larger amount of both hole traps and pre-existing trapped electrons.

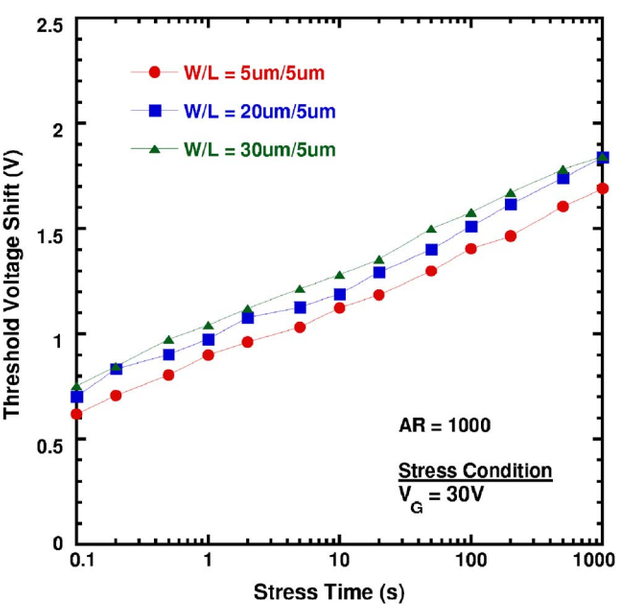
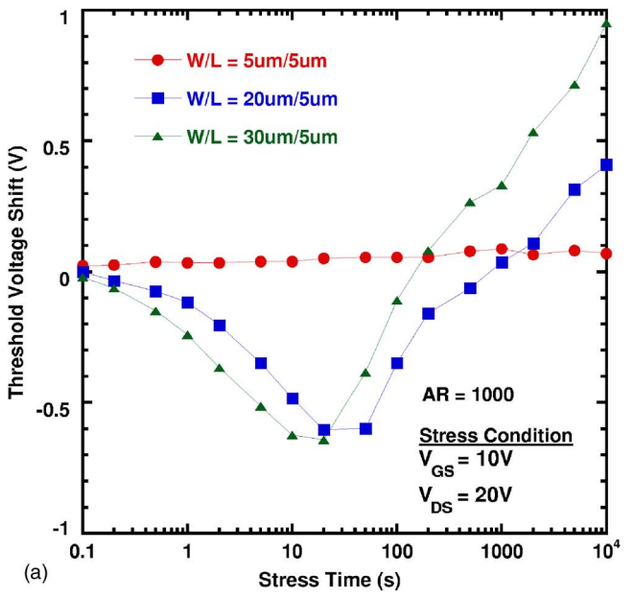


Figure 7. (Color online) Time dependence of the threshold voltage shift for the LTPS TFTs having different channel widths and a fixed AR of 1000 under a gate-bias stress. Stress conditions: $V_D = V_S$ = 0 V; V_G = 30 V.



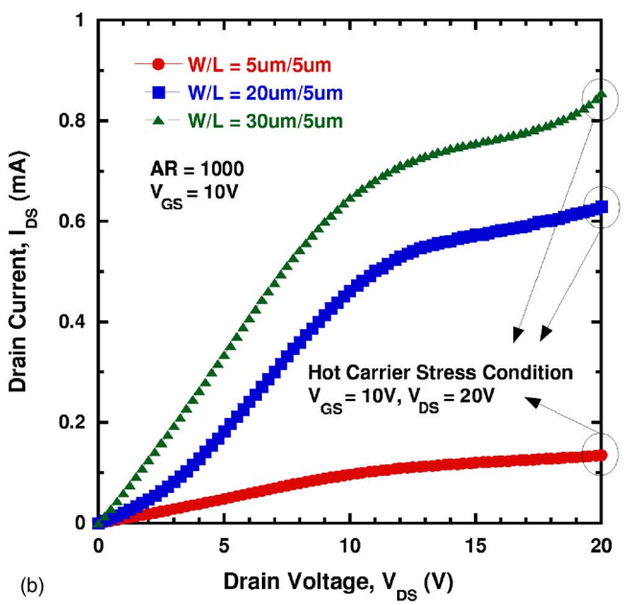
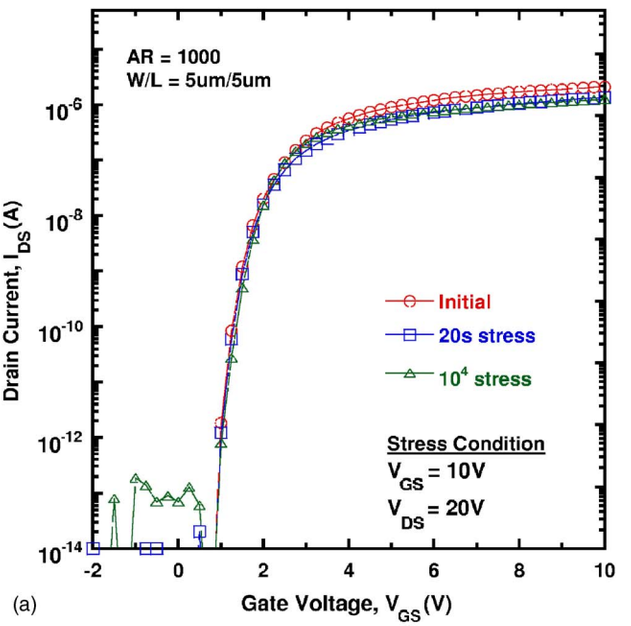


Figure 8. (Color online) (a) Time dependence of the threshold voltage shift for the LTPS TFTs having various channel widths and a fixed AR of 1000 under a hot-carrier stress. (b) Output characteristics of the LTPS TFTs having different channel widths and a fixed AR of 1000 prior to hot-carrier stress. The small circles (O) mark the hot-carrier stress conditions used in this study.



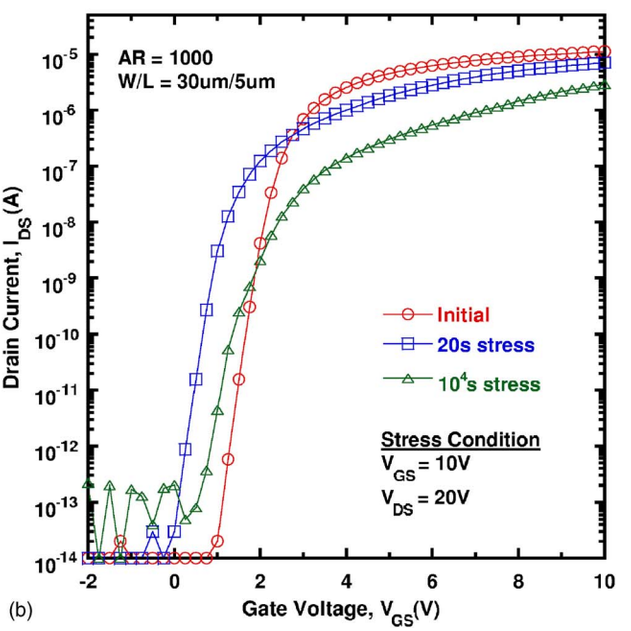


Figure 9. (Color online) Transfer characteristics of the LTPS TFTs having channel widths of (a) 5 and (b) 30 μm and a fixed AR of 1000 at various hot-carrier stress times.

Therefore, a device having a larger channel width exhibits a larger threshold voltage reduction in the first stress regime. As impact ionization continues, hole trapping and the compensation of pretrapped charge effect soon reach saturation.[20] Therefore, hot-electron injection becomes the degrading factor in the second stress regime, leading to positive shifts of the threshold voltage. The kink effects shown in Fig. 8b could be explained from the mechanism proposed by Pretet et al.[21] They have reported that the defects arisen from the mechanical stress shorten the lifetime of carriers along the channel edges and therefore suppress the kink effect for narrow-width devices. The effect can be neglected for the devices having larger channel widths. As a result, in comparing with the devices having larger channel widths, the amount of the impact-ionization-generated holes is relatively reduced for the narrow-width device under our hot-carrier stress condition. Because of the suppressed impact ionization during hot-carrier stress, the 5 μm device has a much smaller current density than the others. Therefore, the device having a 5 μm wide channel has better immunity against hot-carrier degradation.

Figure 9a and b shows the transfer characteristics of the LTPS TFTs having channel widths of 5 and 30 μm, respectively, under hot-carrier stress. The channel length was fixed at 5 μm and the AR was fixed at 1000. For the device having the channel width of 5 μm, the threshold voltage and subthreshold swing changed insignificantly after hot-carrier stress for 10^4 s, as shown in Fig. 9a. For the device having a channel width of 30 μm, however, the device char-

acteristics degraded with increased stress time. The instability of threshold voltage has been explained in the former section. In addition, we found that the subthreshold swing degraded with increased stress time; this phenomenon can be explained by the enhanced impact ionization that generates more interface states during hot-carrier stress. Therefore, we conclude that devices having larger channel widths at a fixed antenna AR are more susceptible to hot-carrier degradation than those having smaller channel widths.

Conclusions

In this study, we investigated the effects of plasma-induced damage on the performance and reliability of LTPS TFTs. Devices having large values of AR exhibited greater instability in their threshold voltage relative to devices having smaller values of AR. This phenomenon is due to the enhanced plasma damage for the large-AR device during the fabrication process. The enhanced damages generates a greater number of trap states in the gate dielectric and degrades the reliability of these devices. For devices having a fixed value of AR of 1000 and various channel widths, we found that the device reliability degraded as the channel width increased. The plasma-induced damage affected both the reliability of the devices and their manufacturing yield. Therefore, for the fabrication of highly reliable devices with improved yield, it is imperative that such antenna structures be designed very carefully.

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