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Formation of Germanium Nanocrystals Embedded in a Silicon-Oxygen-Nitride Layer

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The formation of germanium nanocrystals embedded in silicon-oxygen-nitride with distributed charge storage elements is proposed. A large memory window was observed due to isolated Ge nanocrystals in the SiON gate stack layer. The Ge nanocrystals were nucleated after a high-temperature oxidized SiGeN layer. The Ge nanocrystals embedded in the SiON stack layer exhibited nonvolatile memory characteristics with the obvious threshold voltage shift under a bidirectional voltage sweep. Also, the manufacturing technology using the sequent high-temperature oxidation of the a-Si layer and the direct oxidation of the SiGeN layer is proposed, respectively, for the formation of a blocking oxide layer to enhance the performance of nonvolatile memory devices. The reliability characteristics, including retention time and endurance, are also advisable for the application of nonvolatile memory device.
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In 1967, Kahng and Sze invented the floating-gate (FG) nonvolatile semiconductor memory (or flash memory) at Bell Labs.[1] To date, the flash memory device structure continues to be the most prevailing nonvolatile-memory implementation, and is widely used in both standalone and embedded memories. Because of the low working voltage and nonvolatility, the selection of storage media for most portable electronic devices is the Flash memory which is closely based on the structure of the continuous FG.[2] In a conventional FG memory device, charge is stored in a poly-Si floating gate surrounded by dielectric. The most prominent problem with this is that once there is a charge leakage path (resulting from P/E-cycle degradation) in the gate oxide, all the charges stored in the floating gate will leak away from this one single path because charges are stored in continuous energy level (conduction band) in FG. Therefore, for mass production, there is a trade-off between speed and reliability for the optimal tunnel oxide thickness. Once a leaky path has been created in the tunnel oxide, all the charges stored in the floating gate will be lost. Therefore, several methods are proposed to overcome this oxide quality limit of the conventional FG structure.[2-7] To alleviate the scaling limitation of a conventional FG memory device while preserving the fundamental operating principle of memory, a distributed charge storage approach such as nanocrystal nonvolatile memory was proposed.[5-7] Nanocrystal charge storage offers several advantages, the main one being the potential to use thinner oxide without sacrificing nonvolatility. Unlike the floating gate, stored charges in isolated nodes cannot easily redistribute among themselves and a local leaky path will not cause a fatal loss of information for the nanocrystal nonvolatile memory device. This effectively prevents the leakage of all the stored charges out of the floating gate. Also, the nanocrystal memory device can maintain good retention characteristics and lower power consumption.

Nanocrystals within semiconductor materials have attracted particular attention because of the possibility of integrating nanocrystal with novel or superior properties into existing nanoeletronic and optoelectronic technologies. Si and Ge nanocrystal memories have superior potential for pushing further the scaling limits of conventional nonvolatile memory.[2] In this contribution, the nitride-incorporated silicon germanium (SiGeN) was proposed to be a self-assembling layer of Ge nanocrystals in our previous study.[8] The SiGeN layer was directly deposited using a plasma-enhanced chemical vapor deposition (PECVD) system. After high-temperature thermal oxidation, the Ge nanocrystals were nucleated in the oxidized SiGeN layer. The conditions of thermally oxidized SiGeN layer were also discussed in this study. In addition, the electrical reliability for the proposed metal-oxide-insulator-oxide-silicon (MOIOS) structure is investigated. Also, material analysis such as Fourier transform infrared spectroscopy (FTIR), transmission electron microscopy (TEM), and Auger electron spectroscopy (AES) were utilized to determine the composition and structure of the oxidized SiGeN film. The electrical characteristic analysis, including capacitance-voltage (C-V), current-voltage (I-V), retention time, and endurance, were also performed.

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Experimental

Figure 1 shows the process flow in this work. First, a 5 nm thick thermal oxide was grown as the tunnel oxide on a p-type Si substrate by dry oxidation in an atmospheric-pressure chemical vapor deposition (APCVD) furnace. Subsequently, a 20 nm amorphous silicon germanium nitride layer was deposited by PECVD on the tunnel oxide. The precursors of SiH_4 (20 sccm), GeH_4 (5 sccm), NH_3 (30 sccm), and N_2 (500 sccm) were fed into the PECVD chamber to deposit the SiGeN film at 200°C at a low pressure of 0.6 mTorr with plasma radio-frequency (rf) power of 20 W. The low pressure of 0.6 mTorr during deposition leads the mean free path of electrons to be increased and improves the uniformity of the thin film. Next, the high-temperature SiGeN oxidation was performed in the thermal furnace under oxygen ambient. An oxidation process was then performed to fabricate the oxygen-incorporated SiO_2, acting as a blocking oxide layer. The oxidation temperature was at 900°C for 30, 45, and 60 min, respectively. In this work, we also developed another technology for the blocking oxide formation to enhance memory

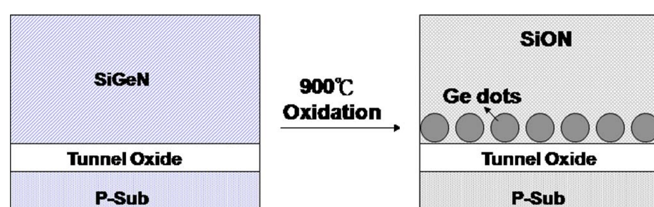

Figure 1. (Color online) The process flow proposed in this work for direct oxidation.

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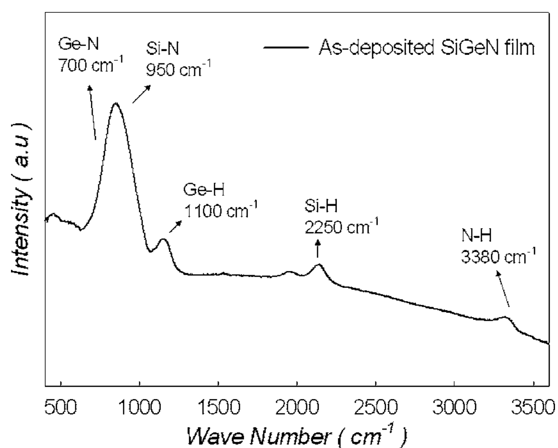

Figure 2. FTIR analysis for the as-deposited SiGeN layer.

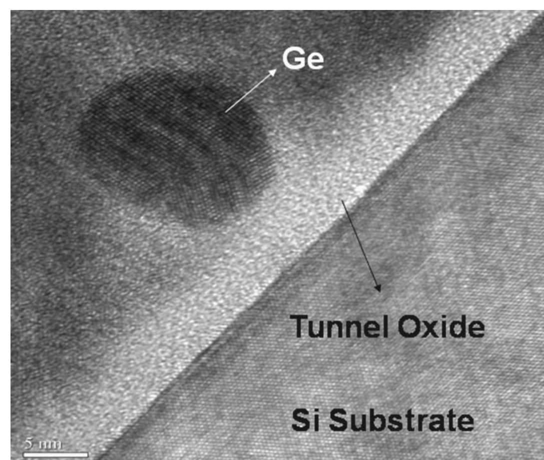

Figure 3. TEM analysis of the MOIOS layer with oxidized SiGeN as the charge trapping layer.

performance, except for the direct oxidation of SiGeN film. In this contribution, an a-Si layer was deposited additionally on SiGeN layer by PECVD at 200°C under a low pressure of 0.6 mTorr with precursors of SiH_4 (20 sccm) and H_2 (980 sccm) and plasma power of 20 W. Then a subsequent high-temperature oxidation process was implemented to transfer the a-Si film into a blocking oxide layer. Finally, the Al gate was deposited and patterned on the blocking oxide layer formed by these two methods to fabricate a MOIOS structure with the charge trapping insulator of SiGeN.

Results and Discussion

Memory device with directly oxidized SiGeN as blocking oxide.— Figure 2 shows the FTIR analysis for the as-deposited SiGeN layer. The initial peak signals of Si–H, Ge–H, and N–H in the as-deposited SiGeN thin film are clearly found in the FTIR spectrum. A thermal furnace process was introduced to form blocking oxide (SiON) and segregate Ge atoms in this study. During the dry oxidation process at 900°C, Si atoms in the SiGeN film more easily combine with O_2 to form a SiON layer than Ge atoms do. Because of the low solid solubility of Ge elements in silicon oxide, the Ge atoms will be segregated downward until they reach the tunnel oxide surface,[9-11] and nucleate to form Ge nanocrystal near the tunnel oxide. Therefore, the SiGeN film will be oxidized to form SiON film as the blocking oxide; meanwhile, the Ge nanocrystals segregated in the SiGeN film and were embedded in SiON dielectric near the tunnel oxide. The TEM analysis and the Raman analysis support the point of view, as shown in Fig. 3 and 4, respectively. It is clearly found that Ge nanocrystals were discretely located at the interface of thermal oxide from the TEM analysis. The signal of Raman spectrum at 300 cm^{-1} represent that the Ge–Ge signal appears due to the Ge nanocrystal formation.

The SiGeN layer of an MOIOS memory device was utilized to capture the injected carriers from the Si channel, which causes a variation in the threshold voltage of the memory device. The C-V measurements were performed by bidirectional voltage sweeping. The three types of thermal process conditions, A, B, and C are listed in Table I. In the dry oxidation conditions A and B (for 30 and 45 min duration), the gate injection phenomena are observed as shown in Fig. 5a and b, respectively. The injected charges cannot be stored in the MOIOS structure, as the oxidation process durations were not longer than 45 min. Hence, the stored charges are leaky to gate electrode, resulting in gate injection. Also, substrate injections are observed in the condition C of 60 min dry oxidation as shown in Fig. 6. The threshold-voltage shift (memory window, ΔV_T) under ±7V C-V sweeping was observed to be about 4 V. When the memory device was programmed, the electrons directly tunneled from the Si substrate through the tunnel oxide, and were trapped in the Ge nanocrystals embedded in SiON layer. For the erase operation, the holes can tunnel from the valence band of the Si substrate and recombine with the electrons trapped in the oxidized SiGeN layer. The stacked structure with Ge nanocrsystals in the dielectric layer was used for the application of memory.[12-14] The charge trap centers are believed to result from the (a) interface states between the silicon substrate, (b) traps inside the dielectric layer, (c) nanocrystal confined state, and (d) interface states between nanocrystals and the surrounding dielectric.[15] The blocking oxide plays a role in preventing the carriers of gate electrode from injecting into the charge-trapping layer by Fowler-Nordheim (F-N) tunneling.

The I-V characteristics for above three conditions are shown in Fig. 7. The leakage current decreased as the dry oxidation duration increased, which indicates that the long duration of thermal oxidation improves the film quality and the film thickness. The dry oxidation under pure oxygen ambient is not effective due to the fact that the oxygen atom with a large volume is difficult to diffuse to the

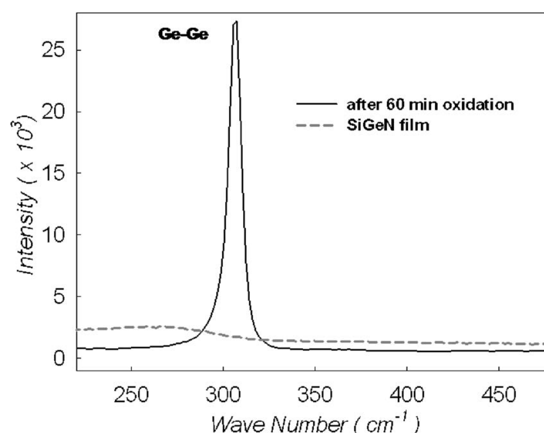

Figure 4. Raman spectra of the as-deposited and oxidized SiGeN layer, respectively.

Table I. Conditions of thermal oxidation for the stacked SiGeN layer.

Condition	900°C O_2 Thermal oxidation (min)
A	30
B	45
C	60

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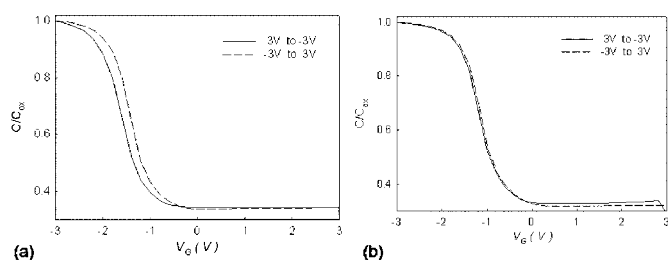

Figure 5. C-V hysteresis of the MOIOS structure for (a) condition A (dry oxidation for 30 min) and (b) condition B (dry oxidation for 45 min).

inner layer. However, the long duration of dry oxidation exhibits more obviously threshold voltage shift under bidirectional voltage sweep.

For the SiO_2 formed by oxidizing SiGeN film, there are dangling bonds and defects exist in the bulk and at the interface between SiGeN and SiO_2 layer. The electrons trapped near the channel will dominate the threshold voltage more significantly than those far from the channel. The proposed SiGeN stack layer with high-temperature oxidized SiGeN layer therefore contributes to the benefits of large memory window and in situ formation of the additional blocking oxide. This is promising for the nonvolatile memory application. The reliability issue of the MOIOS device with Ge nanocrystals embedded in SiON layer (condition C) was also investigated to

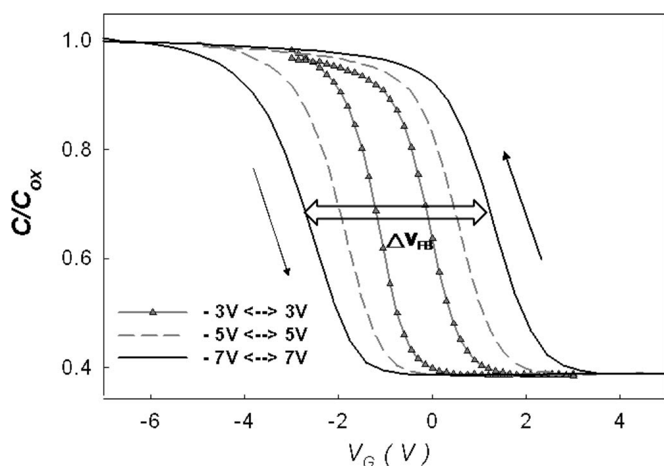

Figure 6. C-V hysteresis of the MOIOS structure for condition C (dry oxidation for 60 min).

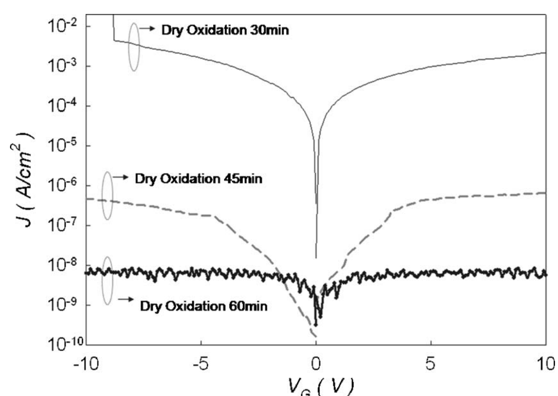

Figure 7. I-V hysteresis of the MOIOS structure for (a) condition A (dry oxidation for 30 min), (b) condition B (dry oxidation for 45 min), and (c) condition C (dry oxidation for 60 min).

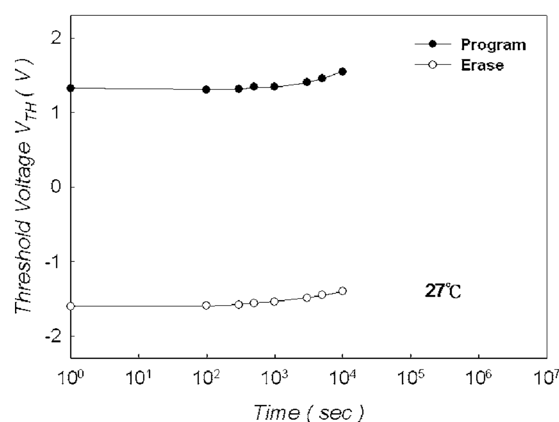

Figure 8. The retention characteristics of the stacked structure with Ge embedded in SiON as the charge trapping layer for condition C (dry oxidation for 60 min).

evaluate its application for a candidate of the distributed charge storage memory device. In Fig. 8, the threshold voltage shift was measured with different time periods at room temperature. It was found that the SiON stack with Ge nanocrystals retained a good retention property without a significant decline of the memory window, which is robust in the Flash nonvolatile memory technology. Figure 9 shows the endurance characteristics, after different write/erase cycles of the Ge nanocrystal embedded SiON layer memory device. The write and erase voltage is 3 and (−3) V, respectively. The memory windows are hardly the same until 10^6 W/E cycles of operation performed. Even after 10^6 cycles of pulse operation, it retains a large memory window of ~3.8 V without catastrophic decline as previous reports on nanocrystal memory devices.[5,7] This certainly demonstrates the rugged nature of the Ge nanocrystal memory device with the suitability for nonvolatile memory devices.

Memory device with oxidized a-Si as blocking oxide.— A thermal furnace process was introduced to form blocking oxide and segregate Ge atoms in this study, as shown in the process flow of Fig. 10. The SiO_2 film originated from the oxidized a-Si film contains dangling bonds or defects in the bulk and at the interface between SiGeN and SiO_2 layer. The electrons trapped near the channel will dominate the threshold voltage significantly more than those far from the channel. In addition, the Si element in the SiGeN film more easily combines with O_2 than Ge to form SiON.

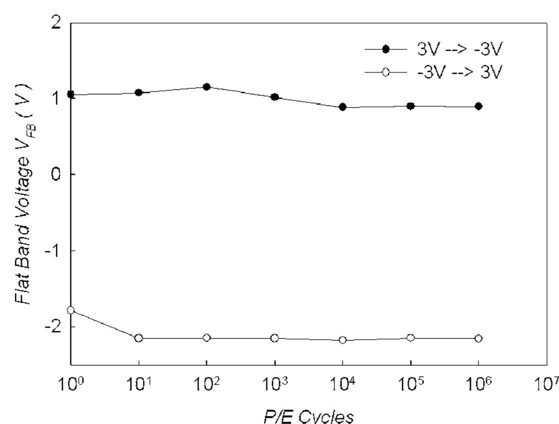

Figure 9. The endurance characteristics of stacked structure with Ge embedded in SiON as the charge trapping layer for condition C (dry oxidation for 60 min).

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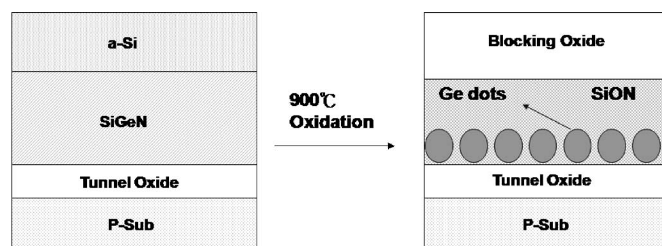

Figure 10. The process flow proposed in this work with oxidized a-Si as the blocking oxide.

In the discussion above it has been found that the low leakage current in the stacked structure is beneficial for exhibiting obvious memory characteristics. Here steam treatment is proposed to reduce the thermal budget of manufacturing processes. Owing to its smaller size and lower activation energy than O_2 molecules, H_2O molecules are more permeable through the blocking oxide and can efficiently passivate dangling bonds in the blocking oxide. Hence, the steam treatment can be an efficient method for the achievement of high-quality blocking oxide. The leakage current characteristics for the stacked structure with or without steam treatment were as shown in Fig. 11. It was clearly found that the leakage current is greatly reduced after steam treatment. The electrical characteristics of C-V hysteresis for stacked structure after 900°C dry oxide oxidation for 30 min and steam treatment for 3 min were as shown in Fig. 12. The memory window is about 2 V under 7 V operation. In addition, the hysteresis effect is counterclockwise, which indicates the charge injection is resulted from substrate. The high-quality blocking oxide avoids the stored charge leaking to gate pad. Hence, the purpose of steam treatment is to strengthen the blocking oxide and improve its quality.

Figure 13 shows the TEM analysis of dry oxidation after 30 min plus steam treatment for 3 min. It exhibits the clearly Ge nanocrystal image at the interface of tunnel oxide after thermal treatment. It is considered that the memory effect as shown in Fig. 12 is contributed by the Ge nanocrystals. The proposed SiGeN stack layer with high-temperature oxidized SiGeN layer, therefore, contributes both larger memory window and the additional blocking oxide deposition for the nonvolatile memory application promisingly.

The reliability characteristics, such as the retention time and endurance, were also discussed. The charge retention time in the MOIOS structure is as shown in Fig. 14. An obvious difference of memory window can be maintained after 10^4 s. However, the little degradation in low-V_{TH} state can be attributed to the effect of hole trap states close to valence band of Ge nanocrystal.[15,16] In addition, the endurance characteristics for program and erase are as shown in Fig. 15. The obvious memory window can be kept after 10^6 program/erase cycles. However, the threshold voltages for program and erase operation both shift to negative voltage, even if the memory window can be distinguished. It is considered that the positive oxide trapped charges causes the negative voltage shift. The AES analysis was investigated to discuss the distribution of Si, Ge, O, and N signals as shown in Fig. 16. It is found that there is a rise in oxygen signal after steam treatment. As a result, the Ge nanocrystals are surrounded by in SiON (partially oxidized as SiO_x). The

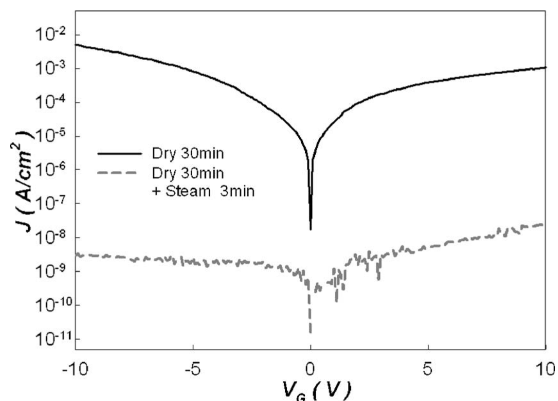

Figure 11. I-V characteristics of the MOIOS structure for dry oxidation for 30 min and dry oxidation for 30 min plus steam treatment for 3 min.

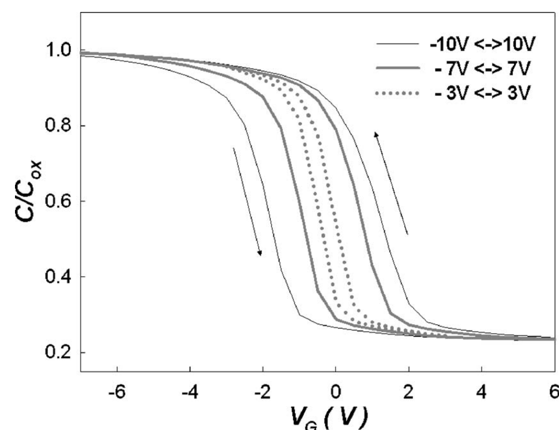

Figure 12. C-V hysteresis of the MOIOS structure for the bidirectional sweep (i) 3 to −3 V, (ii) 7 to −7 V, and (iii) 10 to −10 V.

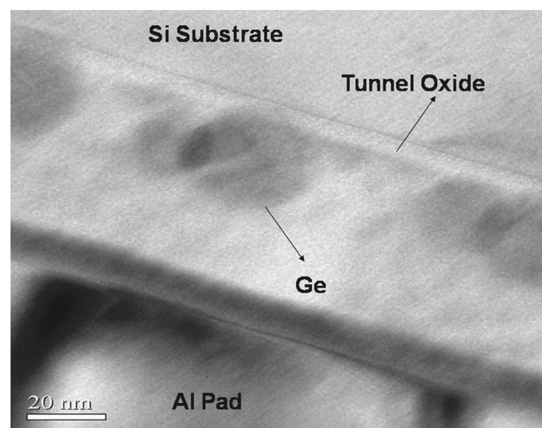

Figure 13. TEM analysis of the MOIOS structure with Ge nanocrystals embedded in the dielectric layer.

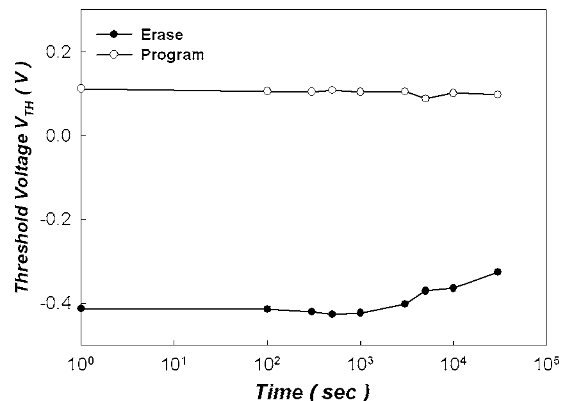

Figure 14. The threshold voltage shift vs different periods of time.

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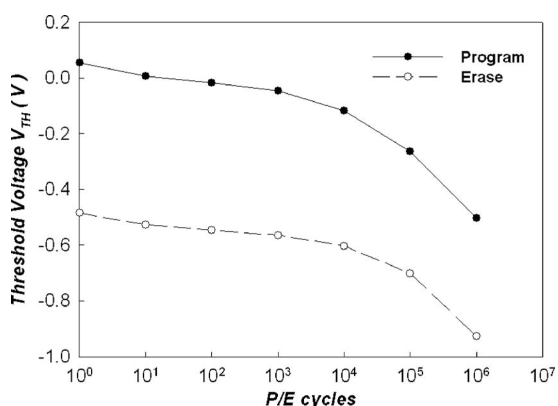

Figure 15. The endurance characteristics after different write/erase cycles of Ge nanocrystals nonvolatile memory.

program and erase curves in Fig. 7 shift to negative voltage at the same time because positive oxide trapped charges are created during the program/erase cycles in both tunnel oxide and the SiO_x.[17] The positive trapped charges in SiO_x will increase with the P/E cycles for the worse quality than tunnel oxide. Therefore, the threshold voltage in the Fig. 15 will shift to negative side. The obvious memory effect and good reliability can be obtained in the MOIOS structure with oxidized SiGeNas charge trapping layer.

In conclusion, the erase technology to form SiGeN stack film with both distributed storage elements and upside blocking oxide has been demonstrated successfully for nonvolatile memory application. The generation of memory windows, after a programming operation, resulted from the storage of charges in germanium nanocrystals embedded in the SiON layer. The dry oxidation causes Ge nanocrystals to segregate to the surface of the tunnel oxide. The completely oxidized SiGeN stacked structure exhibits good electrical retention and endurance characteristics. Furthermore, steam treatment makes for high oxidation efficiency and a better quality of blocking oxide (formed by the oxidation of an a-Si layer). The threshold voltage shifted to negative after numerous program and erase cycles due to the SiON (partially oxidized as SiO_x) after steam treatment. The new material of SiGeN severed as germanium nanocrystal seft-assembling layer was proposed and performed in this study.

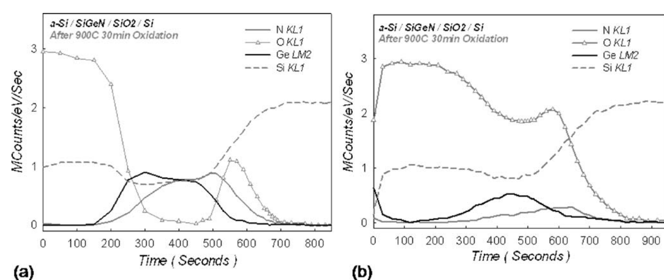

Figure 16. AES of MOIOS structure for (a) dry oxidation and (b) dry oxidation for 30 min plus steam treatment for 3 min.

Acknowledgment

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