



## Nitrogen Effects on the Integrity of Silicon Dioxide Grown on Polycrystalline Silicon

Chao Sung Lai,<sup>a</sup> Chyuan Haur Kao,<sup>a,z</sup> Chung Len Lee,<sup>b</sup> and Tan Fu Lei<sup>b</sup>

<sup>a</sup>Department of Electronics Engineering, Chang Gung University, Tao Yuan, Taiwan

<sup>b</sup>Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan

In this paper, we describe a simple technique to achieve a thin nitrided polyoxide film, only requiring an extra nitrogen implantation to be compatible with the floating gate nonvolatile memory process. The integrity of polyoxides is improved by using the through-silicon-gate nitrogen implantation. Nitridation can be achieved by implanting nitrogen into polysilicon gate followed by a high temperature annealing to drive the nitrogen atoms across the polysilicon, through the polyoxide, and to incorporate nitrogen at the polyoxide/polysilicon interface. The nitrogen-rich layer formed during the driven-in process not only strengthens the polyoxide structure but also improves the polyoxide quality. Improvements of electrical characteristics such as a lower leakage current, a low electron trapping, and a high breakdown field for both positive and negative biases have been observed.  
© 2007 The Electrochemical Society. [DOI: 10.1149/1.2767854] All rights reserved.

Manuscript submitted March 1, 2007; revised manuscript received June 11, 2007. Available electronically August 15, 2007.

In order to obtain good data retention characteristics for nonvolatile memory devices, the interpolysilicon oxides (polyoxides) with low conductivity, high breakdown fields and high charge to breakdown are required.<sup>1-7</sup> The polyoxides grown on polysilicon have a higher leakage current and a lower dielectric strength than those of oxides with comparable thickness grown on single crystal silicon, especially when a positive bias is applied to the top electrode. This is attributed to the rough asperities at the polyoxide/polysilicon interface and nonuniformities in polyoxide film thickness, and enhanced localized electric field due to the enhanced oxidation rate at polysilicon grain boundaries. Also, the integrity of polyoxide mainly depends on growth oxidants or postoxidation annealing.<sup>8,9</sup>

Previous studies showed that the polyoxides grown in N<sub>2</sub>O ambient have good oxide integrity and excellent electrical characteristics. This improvement is largely owing to the incorporation of nitrogen in N<sub>2</sub>O ambient.<sup>10-13</sup> It is also well known that the oxynitride films grown in NO or N<sub>2</sub>O ambient with nitrogen incorporation as gate dielectrics of metal-oxide-semiconductor field effect transistors have been reported to exhibit good electrical and reliability characteristics.<sup>14-17</sup> This is due to the nitrogen incorporation at gate oxide/silicon interface, which can avoid hot-carrier damages, prevent boron penetration and improve interface endurance to Fowler-Nordheim (FN) stress.<sup>18-23</sup> But normal nitridation with NO or N<sub>2</sub>O ambient introduces a small amount of nitrogen at Si/SiO<sub>2</sub> interface, which is insufficient to prevent boron penetration when the oxide is thinner than 3.0 nm. Increasing the temperature or time to increase the nitrogen concentration in oxides will result in a thicker oxide and redistribution of channel doping profile.<sup>24,25</sup> So, the direct implantation of nitrogen into the silicon substrates has been proposed as a nitridation technique for ultrathin gate oxides.<sup>26-30</sup> Some studies have also been reported that gate oxides grown on nitrogen implanted silicon substrates exhibit superior electrical properties, effectively prevent boron penetration and improve the hot-carrier resistance.<sup>31-36</sup>

To achieve a thin nitrided polyoxide film, a simple technique has been described in this study. An extra nitrogen implantation process has been used for the floating gate nonvolatile memory device applications. The integrity of polyoxide films has been improved by nitrogen implantation process. Due to the nitrogen incorporation into polyoxide films, the improved electrical properties such as low leakage current, low electron trapping, and high breakdown field have been observed for both positive and negative bias conditions.

### Experimental

In this study, n<sup>+</sup>-polysilicon/polyoxide/n<sup>+</sup>-polysilicon capacitor structures were fabricated by following process sequence. p-Type Si

wafers were thermally oxidized with a thickness of 100 nm. Then, the polysilicon film (poly-1) with a thickness of 300 nm was deposited by low-pressure chemical vapor deposition at a substrate temperature of 625°C. The poly-1 as a bottom electrode was doped by POCl<sub>3</sub> diffusion process. To activate the dopant, a 1 h drive-in process was performed in N<sub>2</sub> ambient at a temperature of 900°C. The sheet resistance of polysilicon film was ~22 Ω/□.

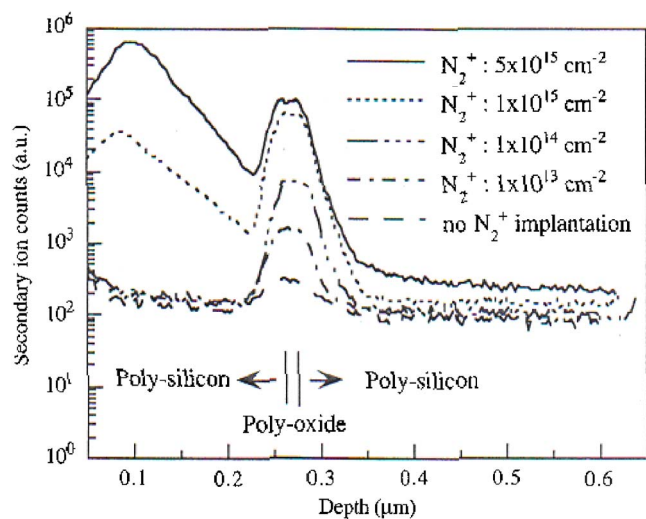
Polyoxides with a thickness of about 13 nm were grown in a pure O<sub>2</sub> ambient at 850°C. Then, the second layer of polysilicon (poly-2) with a thickness of 300 nm for the top electrode was deposited and also doped with POCl<sub>3</sub>. The sheet resistance of poly-2 was ~22 Ω/□. After 15 nm pad oxide was grown in a pure O<sub>2</sub> ambient at 850°C, samples were implanted at 25 keV with nitrogen of various doses from 1 × 10<sup>13</sup>, 1 × 10<sup>14</sup>, 1 × 10<sup>15</sup> to 5 × 10<sup>15</sup> ions/cm<sup>2</sup>, and followed by N<sub>2</sub> ambient annealing for 1 h at 850°C. Then, the poly-2 was defined and on all samples a 100 nm thick oxide was grown via wet oxidation as a passivation layer. Contact holes were opened, and Al was deposited and patterned to form capacitors. Finally, all devices were sintered at 350°C for 40 min in N<sub>2</sub> ambient, which can improve metallurgy between polysilicon and metal film, and it can be further reduced contact resistance.

The thickness of polyoxide film was determined by high-frequency (100 kHz or 1 MHz) capacitance-voltage (C-V) measurement. The current-voltage characteristics of all samples were measured using HP4156 semiconductor parameter analyzer.

### Results and Discussion

The secondary ion mass spectrometry (SIMS) depth profiles of nitrogen for those devices implanted with 0, 1 × 10<sup>13</sup>, 1 × 10<sup>14</sup>, 1 × 10<sup>15</sup>, and 5 × 10<sup>15</sup> ions/cm<sup>2</sup> followed by annealing at 850°C for 1 h in N<sub>2</sub> ambient are shown in Fig. 1. For the highest implanted nitrogen sample (5 × 10<sup>15</sup> ions/cm<sup>2</sup>) in the figure, it can be seen that a highest nitrogen peak is located inside the top polysilicon (poly-2) layer near the as-implanted peak, and nitrogen concentration is gradually lowered down along the polysilicon layer and piled up in the polyoxide/polysilicon interfaces. When the implanted nitrogen dose is reduced, the nitrogen peak located inside the poly-2 film is also lowered, even down to base level as the nonimplanted sample. But it can be found that most of the nitrogen doses of the lighter implanted samples such as 1 × 10<sup>13</sup>, 1 × 10<sup>14</sup> (ions/cm<sup>2</sup>) have been diffused toward the polyoxide/polysilicon interfaces and piled up at the interfaces to incorporate into the polyoxide. For higher nitrogen dose samples, the nitrogen can be incorporated more at the polyoxide/polysilicon interfaces. This is due to the postimplantation high temperature annealing process (850°C for 1 h) to drive and diffuse the implanted nitrogen deeper toward the polysilicon layer and accumulated nitrogen to pile up in the polyoxide/polysilicon interfaces.

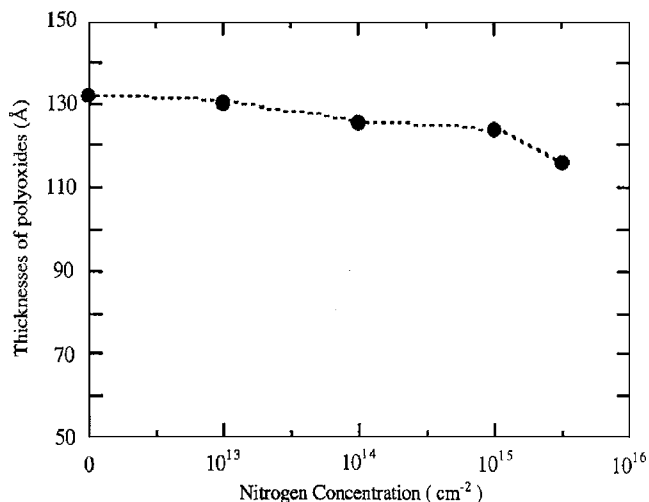
<sup>z</sup> E-mail: chkao@mail.cgu.edu.tw



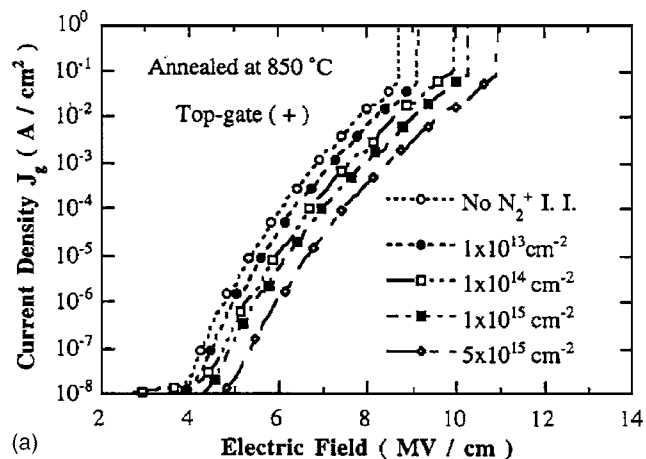
**Figure 1.** The SIMS depth profiles of nitrogen for the devices implanted with  $1 \times 10^{13}$ ,  $1 \times 10^{14}$ ,  $1 \times 10^{15}$  and  $5 \times 10^{15}$  ions/cm<sup>2</sup> and without nitrogen implantation followed by annealing at 850°C in N<sub>2</sub> ambient.

Final thicknesses of all samples determined by *C-V* measurements are shown in Fig. 2. The thickness of nonimplanted sample is about 13.2 nm and the thickness of polyoxide film is gradually decreased with increasing the nitrogen implantation doses. The thickness of highest nitrogen-implanted ( $5 \times 10^{15}$  ions/cm<sup>2</sup>) sample is 15% thinner than that of the nonimplanted sample. It may be due to the nitrogen-rich layer formation. The dielectric constant is increased when nitrogen piled up in the polyoxide/polysilicon interfaces.

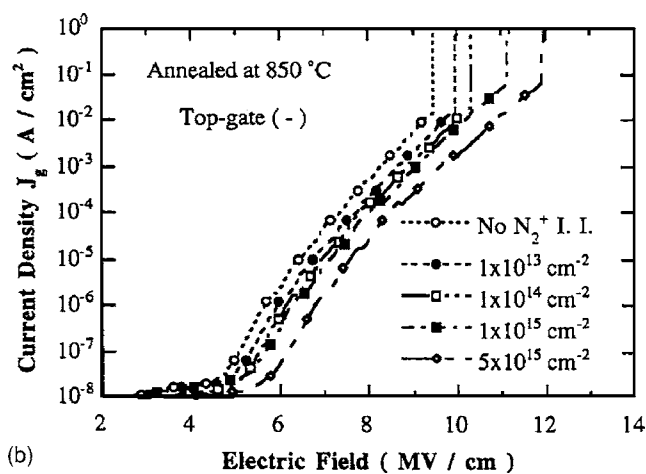
Figure 3a and b shows the *J-E* characteristics of polyoxide films implanted with various doses of nitrogen for positive gate bias (electron injection from the bottom poly-1 electrode) and negative gate bias (electron injection from the top poly-2 electrode), respectively. It can be seen that the nitrogen-implanted polyoxide films exhibit lower leakage currents and higher breakdown electric fields than that of the nonimplanted sample for both positive and negative biases. The improvements of *J-E* characteristics are believed due to the nitrogen implantation in polyoxide films. The nitrogen can passivate the dangling bonds and break the strained Si-O bonds to form more strong Si-N bonds in the polysilicon/polyoxide interfaces. So,



**Figure 2.** The polyoxide thicknesses of the devices implanted with various doses of nitrogen.



(a)

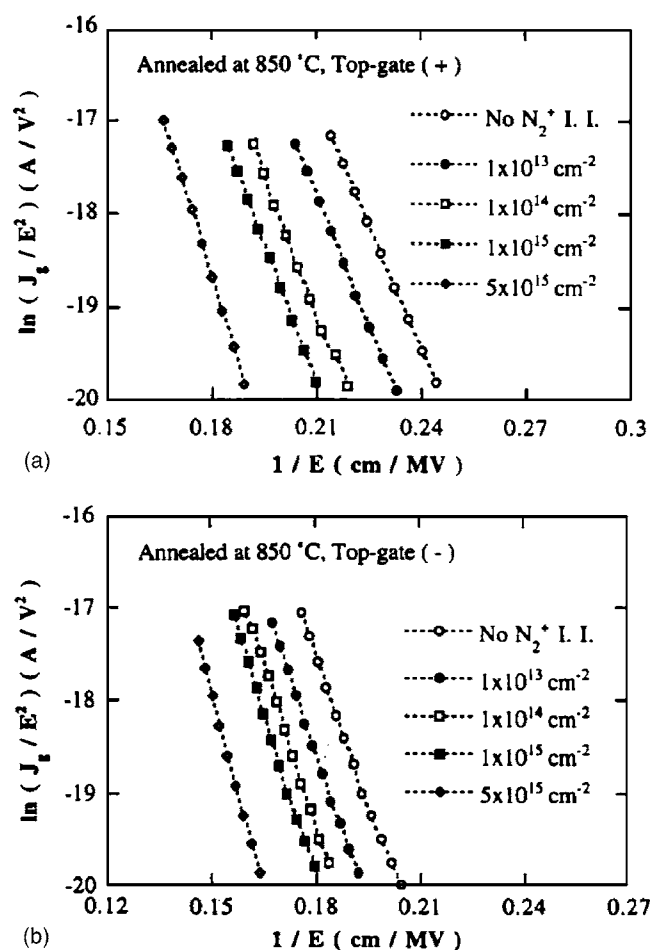


(b)

**Figure 3.** The *J-E* characteristics of polyoxides implanted with various doses of nitrogen for (a) positive gate bias (electron injection from the bottom poly-1 gate), and (b) negative gate bias (electron injection from the top poly-2 gate).

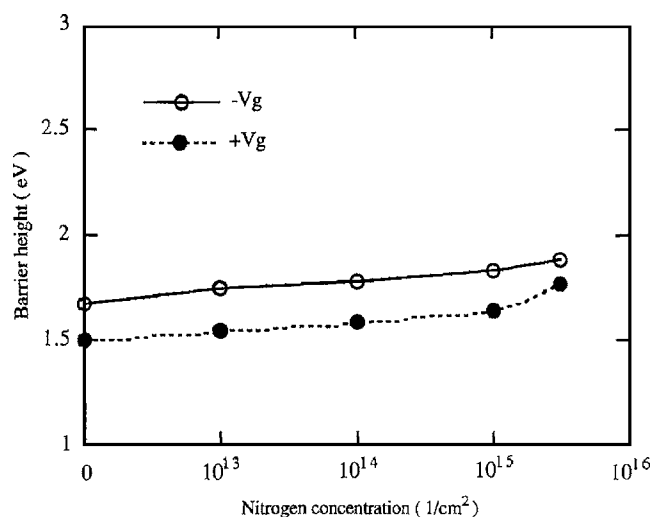
the local stress can be relaxed in the oxide network and made the polysilicon/polyoxide interface morphology smoother. It is indicated that the stress between polyoxide and polysilicon films affects the polyoxide breakdown strength, decreasing the oxide stress increases the breakdown strength.<sup>37</sup> In this experiment, the leakage current and breakdown field for both positive and negative biases are improved with increasing the dose of nitrogen.

It has been reported that the effective barrier height and leakage current of polyoxide were mainly determined by polyoxide/polysilicon interface roughness.<sup>5</sup> The above *J-E* data in the form of FN plot ( $J/E^2$  vs  $1/E$ ) is shown in Fig. 4a and b for the top gate with positive and negative biases, respectively. The effective barrier height extracted from FN plot was shown in Fig. 5. For the positive top-gate bias, the calculated effective barrier heights can be increased from 1.51 eV (for the nonimplanted polyoxide) to 1.76 eV (for the highest nitrogen-implanted polyoxide). For both positive and negative top-gate biases, the effective barrier heights can be gradually increased with increasing the nitrogen implantation doses. The effective barrier height is related to polyoxide/polysilicon interface texture, increasing the barrier height reduces the roughness of the polyoxide/polysilicon interface. This implies that the nitrogen implantation in polyoxide samples can form a nitrogen-rich layer in the polyoxide/polysilicon interfaces after high temperature annealing treatment. It can further improve the polyoxide interface roughness and increase the barrier height. The barrier heights of all samples with negative top-gate bias (electron injection from the top

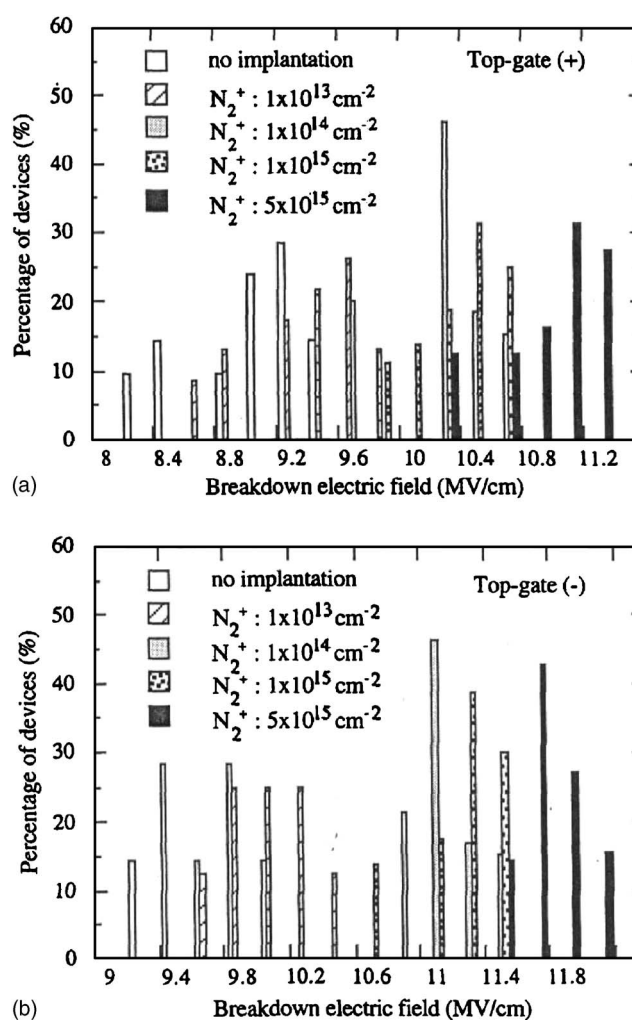


**Figure 4.** Fowler-Nordheim plots ( $J/E^2$  vs  $1/E$ ) for the polyoxides implanted with various doses of nitrogen for (a) positive gate bias and (b) negative gate bias.

poly-2 electrode) are larger as compared with positive top-gate bias (electron injection from the bottom poly-1 electrode). This also im-



**Figure 5.** The effective barrier heights have been extracted from Fowler-Nordheim plot for the polyoxides implanted with various doses of nitrogen under both positive and negative top-gate biases.

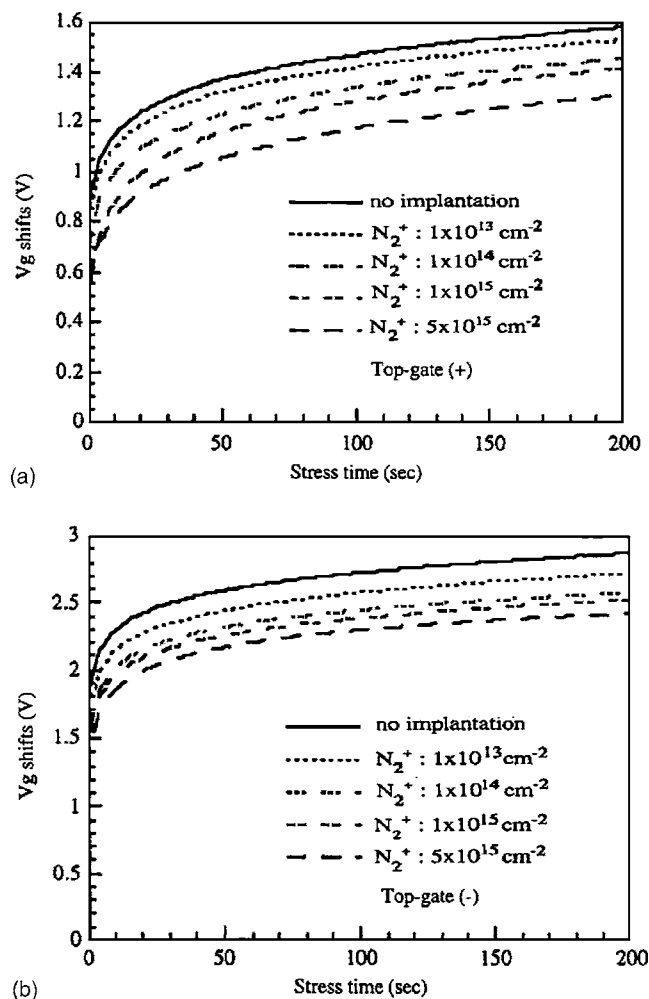


**Figure 6.** The histogram of breakdown electric field for the polyoxide implanted with various doses of nitrogen for (a) positive gate bias and (b) negative gate bias.

plies that the top poly-2/polyoxide interface may be smoother than that of bottom poly-1/polyoxide interface in spite of the sample with or without nitrogen implantation.

The histogram of breakdown electric field for all samples is shown in Fig. 6a and b for positive and negative biases, respectively. It can be seen that the breakdown electric field is increased with increasing nitrogen doses. All samples with positive top-gate bias exhibit a higher conductance and lower dielectric breakdown fields than those of negative top-gate bias. This is due to the enhanced oxidation at the bottom polysilicon grain boundaries, which induces a rougher bottom poly-1/polyoxide interface as compared to the top poly-2/polyoxide interface.<sup>8,9</sup>

The charge trapping characteristics of all nitrogen implanted samples have been investigated. Figure 7a and b shows the gate voltage shift vs time under a constant current stressing of  $100 \mu\text{A}/\text{cm}^2$  for both top-gate positive and negative biases, respectively. The gate voltage increases due to the electron trapping. It is observed that the nitrogen implanted samples show lower electron trapping rates than that of the nonimplanted sample. The electron trapping rates are decreased with increasing the nitrogen implantation for both positive and negative biases. Due to the local high stress in polyoxide films, there are many strained bonds within polyoxides.<sup>2</sup> These strained bonds can easily be broken by high energy electrons, resulting in a dielectric breakdown when a field is applied to the polyoxide films. When nitrogen was implanted into the poly-



**Figure 7.** The gate voltage shifts ( $\Delta V_g$ ) vs time of the polyoxides implanted with various doses of nitrogen under (a)  $+V_g$  and (b)  $-V_g$  constant current ( $100 \mu\text{A}/\text{cm}^2$ ) stressing, respectively.

silicon layer, the nitrogen-rich layer could be formed after the high temperature annealing process. The nitrogen-rich layer not only strengthens polyoxide structure but also improves the polyoxide quality.

### Conclusion

In conclusion, it is found that polyoxide with incorporated nitrogen had a lower leakage current and a higher breakdown field for both positive and negative biases. The implanted nitrogen followed by a high temperature annealing drive the nitrogen across the polysilicon, through the polyoxide, and incorporate nitrogen at the polyoxide/polysilicon interface. These improvements have been observed due to the nitrogen incorporation in the polyoxide films. The nitrogen can passivate the dangling bonds and break the strained Si-O bonds to form strong Si-N bonds in the polysilicon/polyoxide interfaces. Both the strength and quality of polyoxide films can be improved, due to the nitrogen-rich layer formation after high temperature annealing process.

Chang Gung University assisted in meeting the publication costs of this article.

### References

1. T. C. Hamada, Y. Saito, M. Hirayama, H. Aharoni, and T. Ohmi, *IEEE Electron Device Lett.*, **22**, 423 (2001).
2. L. Faraone, R. D. Vibronnek, and J. T. McGinn, *IEEE Trans. Electron Devices*, **ED-32**, 577 (1985).
3. L. Faraone and G. Harbecke, *J. Electrochem. Soc.*, **133**, 1410 (1986).
4. C. Cobianu, O. Popa, and D. Dascalu, *IEEE Electron Device Lett.*, **14**, 213 (1993).
5. J. C. Lee and C. Hu, *IEEE Trans. Electron Devices*, **ED-35**, 1063 (1988).
6. P. Candelier, F. Mondon, B. Guillaumont, G. Reimbold, and F. Martin, *IEEE Electron Device Lett.*, **18**, 306 (1997).
7. T. One, T. Mori, T. Ajioka, and T. Takayashiki, *Tech. Dig. - Int. Electron Devices Meet.*, **1985**, 380.
8. L. Faraone, *IEEE Trans. Electron Devices*, **ED-33**, 1785 (1986).
9. S. L. Wu, T. Y. Lin, C. L. Lee, and T. F. Lei, *IEEE Electron Device Lett.*, **14**, 113 (1994).
10. C. S. Lai, T. F. Lei, and C. L. Lee, *IEEE Trans. Electron Devices*, **43**, 1 (1996).
11. C. H. Kao, C. S. Lai, and C. L. Lee, *IEEE Trans. Electron Devices*, **45**, 1927 (1998).
12. C. H. Kao, C. S. Lai, and C. L. Lee, *IEEE Electron Device Lett.*, **18**, 526 (1997).
13. C. H. Kao, C. S. Lai, and C. L. Lee, *J. Electrochem. Soc.*, **153**, 128 (2006).
14. T. Sasaki, K. Kuwazawa, K. Tanaka, J. Kato, and Dim-Lee Kwong, *IEEE Electron Device Lett.*, **24**, 150 (2003).
15. H. Hwang, W. Ting, D.-L. Kwong, and J. Lee, *IEEE Electron Device Lett.*, **12**, 495 (1991).
16. W.-C. Yang, C.-F. Chen, and K.-M. Chang, *Electron Devices Solid-State Circuits, 2003 IEEE Conference*, p. 349 (2003).
17. Y. Okayama, K. Kasai, T. Yamaguchi, A. Ooishi, M. Takayanagi-Takagi, F. Matsuoka, and M. Kinugawa, *VLSI Technology, Digest of Technical Papers Symposium*, p. 220 (1998).
18. B. S. Doyle and A. Philipossian, *IEEE Electron Device Lett.*, **18**, 267 (1997).
19. V. P. Gopinath, V. Hornback, Y. Le, A. Kamath, L. Duong, J. Lin, M. R. Mirabedini, and W. C. Yeh, *Gate Insulator, 2003.IWGI, Extended Abstracts of International Workshop*, November, p. 50 (2003).
20. Y. Y. Chen, M. Gardner, J. Fulford, D. Wristers, A. B. Joshi, L. Chung, and D. L. Kwong, *VLSI Technology, Systems, and Applications, International Symposium*, p. 86 (1999).
21. Y. Okada, P. J. Tobin, K. G. Reid, R. I. Hegde, B. Maiti, and S. A. Ajuria, *IEEE Trans. Electron Devices*, **41**, 608 (1994).
22. M. Bhat, D. J. Wristers, L.-Kai Han, J. Yan, H. J. Fulford, and D.-L. Kwong, *IEEE Trans. Electron Devices*, **42**, 907 (1995).
23. M.-S. Joo, I.-S. Yeo, C.-H. Lee, H.-J. Cho, S.-A. Jang, and S.-K. Lee, *IEEE Electron Device Lett.*, **20**, 445 (1999).
24. M. Bhat, D. J. Wristers, L.-K. Han, J. Yan, H. J. Fulford, and D.-L. Kwong, *International Electron Devices Meeting*, p. 329 (1994).
25. M. K. Mazumder, A. Teramoto, J. Komori, and Y. Mashiko, *ICMTS Proceedings of Microelectronic Test Structures*, p. 103 (2001).
26. S. Hadda and M. S. Liang, *IEEE Electron Device Lett.*, **8**, 58 (1987).
27. A. J. Bauer, P. Mayer, L. Frey, V. Haublein, and H. Ryssel, *Ion Implantation Technology Proceedings*, **1**, p. 26 (1998).
28. L. K. Han, S. Crowder, M. Hargrove, E. Wu, S. H. Lo, F. Guarin, E. Crabbe, and L. Su, *Tech. Dig. - Int. Electron Devices Meet.*, **1997**, 643.
29. B. Yu, D.-H. Ju, W.-C. Lee, N. Kepler, T.-J. King, and C. Hu, *IEEE Trans. Electron Devices*, **45**, 1253 (1998).
30. A. I. Chou, C. Lin, K. Kumar, P. Chowdhury, M. Gardner, M. Gilmer, J. Fulford, and J. C. Lee, *IEEE International Reliability Physics Symposium, 35th Annual Proceedings*, p. 174 (1997).
31. I.-H. Nam, J. S. Sim, S. I. Hong, B.-G. Park, J. D. Lee, S.-W. Lee, M.-S. Kang, Y.-W. Kim, K.-P. Suh, and W. S. Lee, *IEEE Trans. Electron Devices*, **48**, 2310 (2001).
32. C. T. Liu, Y. Ma, H. Luftman, and S. J. Hillenius, *IEEE Electron Device Lett.*, **18**, 212 (1997).
33. C. T. Liu, Y. Ma, J. Becerro, S. Nakahara, D. J. Eaglesham, and S. J. Hillenius, *IEEE Electron Device Lett.*, **18**, 105 (1997).
34. Y. Y. Chen, D. L. Kwong, M. Gardner, and J. Fulford, *Solid-State Device Research Conference*, p. 292 (1998).
35. C.-C. Chen, H.-C. Lin, C.-Y. Chang, C.-C. Huang, C.-H. Chien, T.-Y. Huang, and M.-S. Liang, *Plasma Process-Induced Damage, 5th International Symposium*, p. 121 (2000).
36. A. J. Bauer, P. Mayer, L. Frey, V. Haublein, and H. Ryssel, *Ion Implantation Technology Proceedings, 1998 International Conference*, Vol. 1, p. 30 (1998).
37. H. N. Chern, C. L. Lee, and T. F. Lei, *IEEE Electron Device Lett.*, **15**, 181 (1994).