DESIGN OF HIGH-VOLTAGE-TOLERANT POWER-RAIL ESD CLAMP CIRCUIT IN LOW-VOLTAGE CMOS PROCESSES

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ABSTRACT

A new high-voltage-tolerant power-rail electrostatic discharge (ESD) clamp circuit with a special ESD detection circuit realized with only 1×VDD devices for 3×VDD-tolerant mixed-voltage I/O interfaces is proposed. The proposed power-rail ESD clamp circuit with excellent ESD protection effectiveness has been verified in a 0.13-μm CMOS process with only 1.2-V devices.

INTRODUCTION

With the scaled-down device dimension in advanced CMOS technology, the power supply voltage is also scaled down to reduce the power consumption and to meet the gate-oxide reliability. With consideration of whole system integration, the I/O buffers must drive or receive high-voltage signals to communicate with other ICs in a microelectronic system. Thus, the I/O buffers should be designed with high-voltage tolerance to prevent overstress voltage on the thinner gate oxide of I/O devices [1]. To achieve a good whole-chip ESD protection scheme for the mixed-voltage I/O applications, it is required to design the power-rail ESD clamp circuit with only low-voltage devices but that can sustain the high power-supply voltage without suffering gate-oxide reliability [2]-[4]. The mixed-voltage I/O buffer to receive 3×VDD input signals by using only 1×VDD low-voltage devices without suffering gate-oxide reliability has been reported [5]. Nevertheless, the ESD protection design for such a 3×VDD-tolerant mixed-voltage I/O buffer was not considered. Therefore, how to design an effective ESD protection circuit with only low-voltage devices without suffering gate-oxide reliability for mixed-voltage I/O buffer with 3×VDD input tolerance is a significant challenge.

In this work, a new high-voltage-tolerant ESD clamp circuit realized with only 1.2-V low-voltage devices for mixed-voltage I/O interfaces with 3×VDD input tolerance is proposed. This new proposed ESD protection design has no gate-oxide reliability issue under normal circuit operating condition. Besides, this design has an efficient ESD detection circuit to trigger on the ESD clamp device during ESD stress event, so that the turn-on efficiency of ESD clamp device can be substantially improved. The proposed ESD protection design has been successfully verified in a 0.13-μm CMOS process with only 1.2-V devices.

3×VDD-TOLERANT POWER-RAIL ESD CLAMP CIRCUIT WITH ONLY 1×VDD DEVICES

The novel 3×VDD-tolerant power-rail ESD clamp circuit, which contains ESD clamp device and ESD detection circuit, is shown in Fig. 1, where the ESD clamp device is realized by a substrate-triggered SCR with two diodes in series. The new proposed power-rail ESD clamp circuit is realized with only 1.2-V low-voltage devices to operate at 3.3-V power supply (3×VDD) without the risk of gate-oxide reliability.

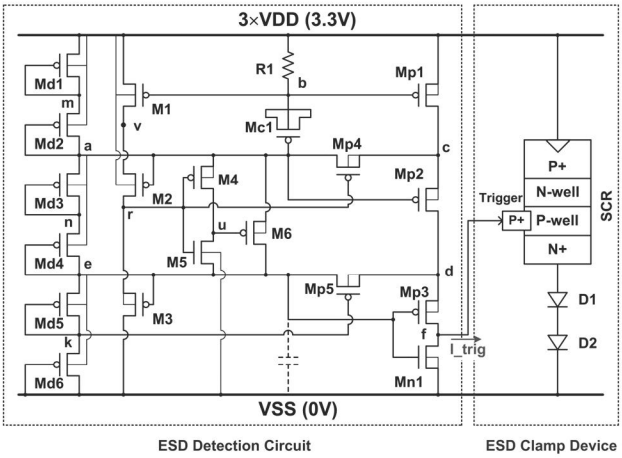

FIGURE 1. THE PROPOSED 3×VDD-TOLERANT ESD CLAMP CIRCUIT REALIZED WITH ONLY 1×VDD DEVICES.

To avoid the damage of mixed-voltage I/O buffers before ESD clamp device is turned on, a turn-on-efficient ESD detection circuit realized with 1×VDD devices to sustain 3×VDD signals is essential in such 1.2/3.3-V mixed-voltage I/O interfaces. The proposed ESD detection circuit that can be operated under 3.3-V voltage bias with only 1.2-V low voltage devices is shown in Fig. 1. During the normal circuit operating condition with 3×VDD line of 3.3V and grounded VSS, the voltage levels at node a and node e in the ESD detection circuit are biased at 2.2V and 1.1V, respectively. The gate voltage (node k) of Mp5 will be biased at 0.6V due to the body effect of Md6, so that Mp5 is turned on and the node d is biased at 1.1V. Therefore, Mp3 is turned off and there is no trigger current generated from the ESD detection circuit into the ESD clamp device. In this situation, all 1.2-V devices are free from gate-oxide reliability issue under normal circuit operating condition with 3×VDD line of 3.3V.

When ESD voltage is conducted to the 3×VDD line with VSS relatively grounded, the RC delay of resistor R1 and capacitor Mc1 in the ESD detection circuit keep node b at a relatively low voltage level for a long time. M1 and Mp1 can be turned on and therefore the voltage levels at node c and node v rise rapidly. The voltage levels at node a and node e are initially floating with a voltage level of ~0V, so that M2 and Mp2 can be turned on, and the voltage levels at node r and node d also rise as the voltage levels at node v and node c. The RC delay of the turn-on resistance of Mp5 and the parasitic capacitance of Mn1 keep the node e in a low voltage level to ensure that Mp3 is in the turned-on state during ESD stress event. Moreover, the gate voltage of M5 is higher than its source voltage so that M5 is turned on to keep the voltage level at node u in a low voltage level as that at node e. Therefore, the gate-to-drain voltage of M6 is nearly zero to keep the voltage level at node a around the voltage level at node e plus a threshold voltage of M6, when the voltage level at node a is one threshold voltage higher than the voltage level at node u. Furthermore, the gate voltage (node r) of Mp4 is as high as its source

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voltage (node c), so that Mp4 is in off state to ensure that the voltage level at node a can be kept in a low voltage level compared with node c. Therefore, the substrate driver of Mp1, Mp2, and Mp3, whose gates are at relatively low voltage levels, can be quickly turned on by ESD energy to generate the substrate-triggered current into the trigger node (node f) of the SCR. Fig. 2 shows the Hspice-simulated voltages of the ESD detection circuit under ESD stress event. A 0-to-6V ESD-like pulse with a rise time of 10ns is applied to the 3×VDD line to simulate the ESD transient voltage. From the simulation results, such low voltage levels at node a, node b, and node e guarantee that Mp1, Mp2, and Mp3 can be turned on during ESD stress event. Therefore, the substrate-triggered current can be generated by the substrate driver into the trigger node of SCR to trigger on the ESD clamp device to discharge ESD current from the 3×VDD line to VSS.

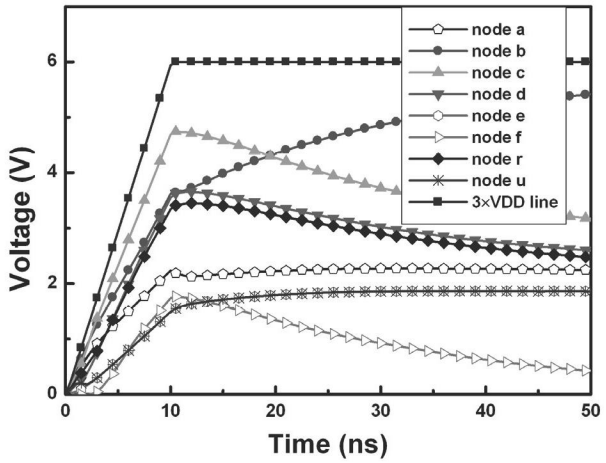

FIGURE 2. HSPICE-SIMULATED VOLTAGES ON NODES OF THE ESD DETECTION CIRCUIT UNDER 0-TO-6V ESD-LIKE TRANSITION WITH A RISE TIME OF 10NS ON THE 3×VDD LINE.

EXPERIMENTAL RESULTS

The proposed ESD protection circuit has been fabricated in a 0.13-μm CMOS process with only 1.2-V devices. To investigate the ESD clamp device behavior with ESD detection circuit during ESD stress event, transmission line pulse (TLP) generator with a pulse width of 100ns and a rise time of ~10ns is used to measured the second breakdown current (It2) of the ESD protection circuit. The TLP-measured I-V characteristics of the ESD clamp device with or without ESD detection circuit under positive ESD stress from 3×VDD line to VSS are shown in Fig. 3, where the width of SCR in ESD clamp device is 60μm. From the measured results, the trigger voltage of ESD clamp device without ESD detection circuit is 12.7V, whereas the trigger voltage of ESD clamp device can be reduced to only 4.6V by ESD detection circuit without involving the junction avalanche breakdown. Therefore, the trigger voltage of ESD clamp device can be significantly reduced by the proposed ESD detection circuit to ensure effective ESD protection.

The human-body-model (HBM) ESD levels and machine-model (MM) ESD levels of the proposed ESD protection circuit with various widths of SCR-based ESD clamp devices are listed in Table I. The HBM ESD levels of ESD protection circuit under SCR widths of 30μm, 45μm, and 60μm are 4kV, 6.2kV, and larger than 8kV, respectively. Besides, the MM ESD levels of ESD protection circuit under SCR widths of 30μm, 45μm, and 60μm are 260V, 380V, and 440V, respectively. The corresponding second breakdown current (It2) measured by TLP is also listed in Table I.

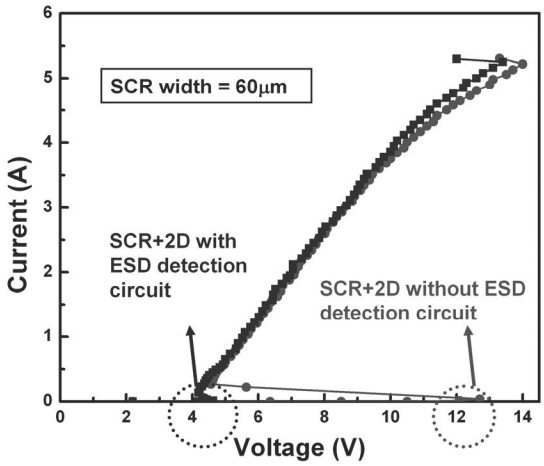

FIGURE 3. THE MEASURED TLP I-V CHARACTERISTICS OF THE ESD CLAMP DEVICE WITH OR WITHOUT ESD DETECTION CIRCUIT UNDER POSITIVE 3×VDD-TO-VSS ESD STRESS.

TABLE 1. ESD ROBUSTNESS OF THE PROPOSED ESD PROTECTION CIRCUIT WITH VARIOUS SCR WIDTHS

ESD clamp device (SCR) width (μm)	HBM ESD Level	MM ESD Level	TLP-measured It2
30	4kV	260V	2.56A
45	6.2kV	380V	3.82A
60	>8kV	440V	5.31A

CONCLUSION

A new high-voltage-tolerant power-rail ESD clamp circuit with ESD detection circuit realized with only 1.2-V low voltage devices for 3×VDD-tolerant mixed-voltage I/O interfaces has been successfully verified in a 0.13-μm CMOS process. The ESD detection circuit can significantly reduce the trigger voltage of ESD clamp device. The proposed power-rail ESD clamp circuit with high ESD robustness and no gate-oxide reliability issue is an excellent ESD protection solution for the mixed-voltage I/O interfaces with high-voltage input/output signals.

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