

FAILURE OF ON-CHIP POWER-RAIL ESD CLAMP CIRCUITS DURING SYSTEM-LEVEL ESD TEST

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ABSTRACT

Four different on-chip power-rail electrostatic discharge (ESD) protection circuits, (1) with typical RC-triggered; (2) with NMOS+PMOS feedback; (3) with PMOS feedback; and (4) with cascaded PMOS feedback, have been designed and fabricated in a 0.18- μm CMOS technology to investigate their susceptibility to system-level ESD test. During the system-level ESD test, where the ICs in a system have been powered up, the feedback loop used in the power-rail ESD clamp circuit provides the lock function to keep the main ESD device in a “latch-on” state. The latch-on ESD device, which is often designed with a larger device dimension to sustain high ESD level, conducts a huge current between the power lines to perform a latchup-like failure after the system-level ESD test. From the experimental results, two kinds of on-chip power-rail ESD clamp circuits with feedback structures are highly sensitive to transient-induced latchup-like failure than others.

INTRODUCTION

Electrostatic discharge (ESD) protection has been one of the most important reliability issues in CMOS IC products. In order to obtain high ESD robustness, a CMOS IC must be designed with on-chip ESD protection circuits at the input/output (I/O) pins and across the power lines. When the input (or output) pin is zapped under the positive-to- V_{SS} (PS-mode) or negative-to- V_{DD} (ND-mode) ESD stresses, the power-rail ESD clamp circuit can provide a low impedance path between the V_{DD} and V_{SS} power lines to efficiently discharge the ESD current. To enhance the triggering efficiency of the power-rail ESD clamp circuit, some advanced designs had been reported in [1]-[4].

Recently, system-level ESD reliability has attracted more attentions than before in microelectronics products. During the system-level ESD test, some of ESD-induced overshooting/undershooting pulses may couple into the microelectronics products to cause damage or malfunction in CMOS ICs. Some CMOS ICs are very susceptible to system-level ESD stress, even though they have passed the component-level ESD specifications.

In this work, the wrong triggering behavior among different on-chip power-rail ESD clamp circuits under system-level ESD test are investigated and first reported in the literature. Some feedback loop in the power-rail ESD clamp circuits will continually keep the ESD-clamping NMOS in the latch-on state after the system-level ESD test. The latch-on ESD-clamping NMOS between V_{DD} and V_{SS} power lines in the powered-up microelectronics system causes a serious latchup-like failure in CMOS ICs.

POWER-RAIL ESD CLAMP CIRCUITS

To provide effective on-chip ESD protection, four different power-rail ESD clamp circuits had been reported [1]-[4], which are re-drawn in Figs. 1(a)-1(d) with the names of (1) typical RC-based power-rail ESD clamp, (2) power-rail ESD clamp with NMOS+PMOS feedback, (3) power-rail ESD clamp with PMOS feedback, and (4) power-rail ESD clamp with cascaded PMOS feedback.

The typical RC-based power-rail ESD clamp circuit is illustrated in Fig. 1(a) with a three-stage buffer between the RC circuit and the ESD-clamping NMOS [1]. The RC time constant in the RC-based ESD-transient detection circuit has been typically designed about 0.1 ~ 1 μs to detect the ESD pulses with the rise time of ~10ns and to keep off the power-rail ESD clamp circuit under normal power-on transition with the rise time of ~1ms.

In the advanced CMOS technology with thinner gate oxide, the large MOS capacitance could suffer large gate oxide leakage current [6]. It was reported that the power-rail ESD clamp circuit incorporated with a regenerative feedback network can be used to reduce the RC time constant [2], as illustrated in Fig. 1(b). When a fast positive going ESD transient across the power rails, the MNFB can further pull the potential of INV2OUT node towards ground to latch the ESD-clamping NMOS in the conducting state until the voltage on V_{DD} drops below the threshold voltage of ESD-clamping NMOS.

The power-rail ESD clamp circuit incorporated with PMOS feedback [3], as shown in Fig. 1(c), can be used to mitigate false triggering during a fast power-up transition (rise time < 10 μs). The transistor MPFB can help to keep the gate voltage of ESD-clamping NMOS below the threshold voltage and further reduce the current drawn during the power-up transition.

Another power-rail ESD clamp circuit with cascaded PMOS feedback has been proposed to reduce the RC time constant and to solve false trigger issue during fast power-up transition [4], as shown in Fig. 1(d). During the ESD-stress condition, the transistor MPFB is turned off and the voltage on the INV2OUT node can be remained in a low state. If the power-rail ESD clamp circuit is mis-triggered by fast transient, the voltage on the INV2OUT node can be charged up toward V_{DD} by the subthreshold current of MPFB.

SYSTEM-LEVEL ESD TEST

In the standard of IEC 61000-4-2 [5], the measurement setup of the system-level ESD test with indirect contact-discharge test mode has been specified, which is used to verify the susceptibility of the fabricated power-rail ESD clamp circuits to system-level ESD stresses. When the latchup-like failure occurs after ESD zapping, the I_{DD} will significantly increase and the voltage level on V_{DD} node will be pulled down to a much lower level due to the latch-on state of ESD-clamping NMOS in the power-rail ESD clamp circuits.

As shown in Fig. 2, after the system-level ESD test with ESD voltage of -200V, latchup-like failure can be founded in the power-rail ESD clamp circuit with NMOS+PMOS feedback structure, because I_{DD} significantly increases and V_{DD} is pulled down. All the PMOS and NMOS devices in the ESD-transient detection circuits are surrounded with double guard rings to guarantee no latchup issue in this part. This implies that the feedback loop in the ESD-transient detection circuit is locking after system-level ESD test and to continually keep the ESD-clamping NMOS in its latch-on state. The continued latchup-like state will result in malfunction or even damage in CMOS ICs due to the pulled-down V_{DD} voltage level and so huge I_{DD} current.

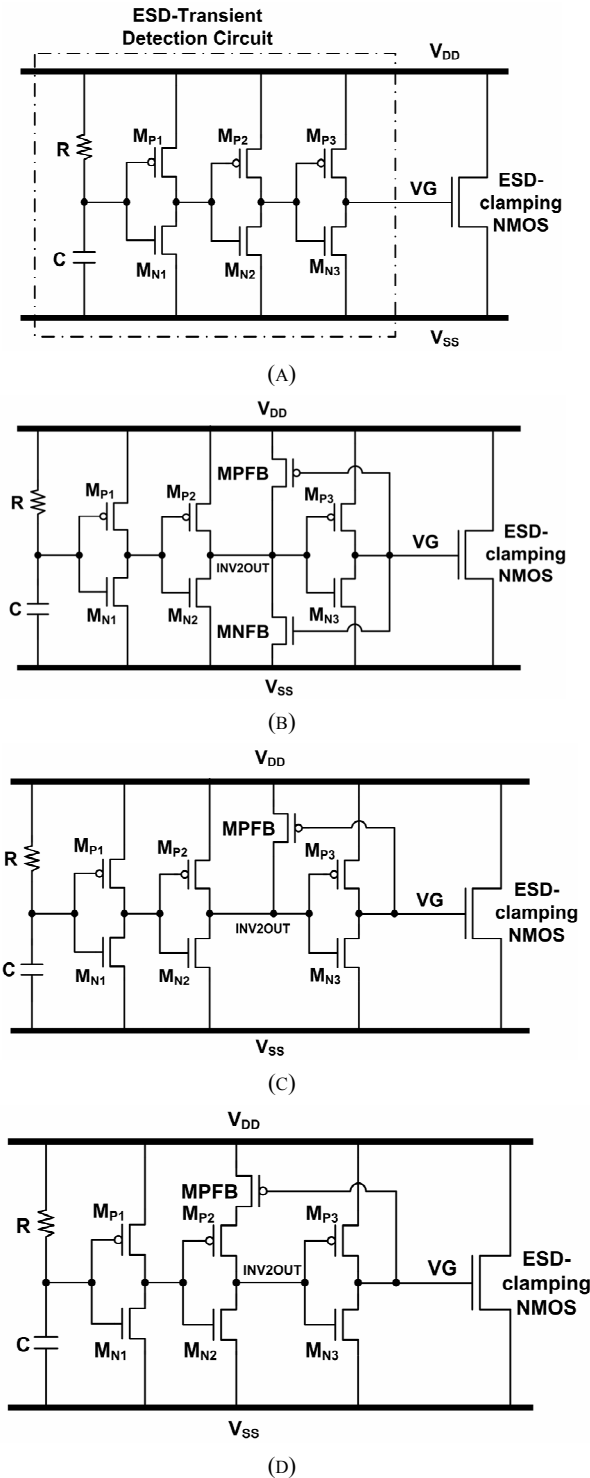


FIGURE 1. FOUR DIFFERENT POWER-RAIL ESD CLAMP CIRCUITS DESIGNED WITH (A) TYPICAL RC-BASED DETECTION, (B) NMOS+PMOS FEEDBACK, (C) PMOS FEEDBACK, AND (D) CASCADED PMOS FEEDBACK.

The susceptibility among the aforementioned four different power-rail ESD clamp circuits against system-level ESD test are listed in Table I. The power-rail ESD clamp circuits with NMOS+PMOS feedback or with cascaded PMOS feedback have lower susceptibility to system-level ESD test. Modified design on such power-rail ESD clamp circuits with feedback loop should be developed to overcome such latchup-like failure.

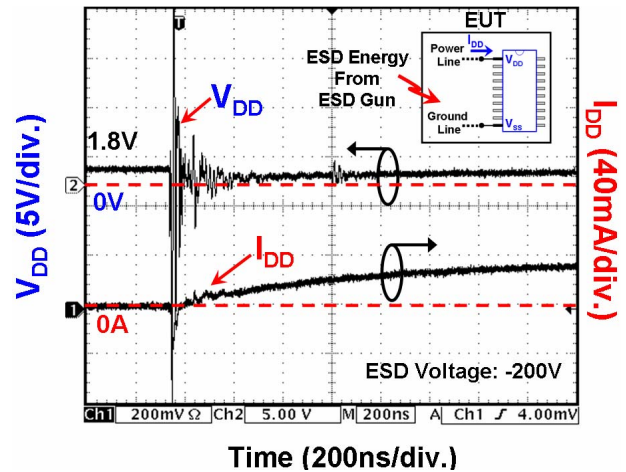


FIGURE 2. MEASURED V_{DD} AND I_{DD} WAVEFORMS ON THE POWER-RAIL ESD CLAMP CIRCUIT WITH NMOS+PMOS FEEDBACK UNDER SYSTEM-LEVEL ESD TEST WITH ESD VOLTAGE OF -200V.

TABLE I. COMPARISON ON THE SUSCEPTIBILITY AMONG FOUR DIFFERENT POWER-RAIL ESD CLAMP CIRCUITS UNDER SYSTEM-LEVEL ESD TEST.

Power-Rail ESD Clamp Circuits	Positive ESD Stress	Negative ESD Stress
Typical RC-Based Detection	over +10kV	over -10kV
With PMOS Feedback	over +10kV	over -10kV
With NMOS+PMOS Feedback	+2.5kV	-0.2kV
With Cascaded PMOS Feedback	over +10kV	-1kV

CONCLUSION

Some of advanced on-chip power-rail ESD clamp circuits designed with feedback loop in their ESD-transient detection circuits have been found to suffer the latchup-like failure after the system-level test. The latch-on state of the ESD-clamping NMOS is kept by the feedback loop in the ESD-transient detection circuit during and after system-level ESD stress. The huge I_{DD} current due to continued latchup-like state will result in malfunction or even damage in CMOS ICs.

ACKNOWLEDGMENT

The authors would like to thank Himax Technologies, Inc., Taiwan, for the project support on this reliability topic.

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